Siliconix incorporated

DG506A/507A

16-Channel and Dual 8-Channel CMOS Analog Multiplexers

T-51-11

FEATURES

- TTL & CMOS Direct Control Over Military Temperature Range
- Low Power (30 mW typ.)
- Break-Before-Make Switching
- 44 V Power Supply Rating

BENEFITS

- Easily Interfaced
- Reduced Power Consumption
- Reduced System Cross-Talk
- Environmentally Rugged

APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing

DESCRIPTION

DG506A and DG507A are 16- and dual 8-channel analog multiplexers, respectively, designed for selecting 1 of 16 (or 8) analog input signals and connecting it to a common output or, conversely, routing an analog signal to 1 of 16 (or 8) output loads. Break-before-make switching action protects against momentary shorting of the input signals.

The DG506A, an 16-channel single-ended analog multiplexer, is designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address (A_0, A_1, A_2, A_3). DG507A, a dual 8-channel analog multiplexer, is designed to connect 1 of 8 dual inputs to a common dual output as determined by its 3 bit binary address (A_0, A_1, A_2) logic.

A channel in the ON state conducts current equally well in both directions (bidirectional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

Designed in the Siliconix PLUS-40 process, the absolute maximum voltage rating is extended to 44 Volts, allowing increased operating headroom for standard ±15 V signal swings and operation with ±20 V supplies. An epitaxial layer prevents latch up.

Both DG506A and DG507A are available in dual-in-line ceramic and plastic packages, and are specified for operation over the military, A suffix (–55 to 125°C), industrial, D suffix (–40 to 85°C), and commercial, C suffix (0 to 70°C), temperature ranges.

For applications requiring address data latching, the DG528/DG529 is recommended. For wideband/ video routing and multiplexing applications, the DG536 is recommended.

For more information, refer to Siliconix Application Note AN75-1 and AN73-2.

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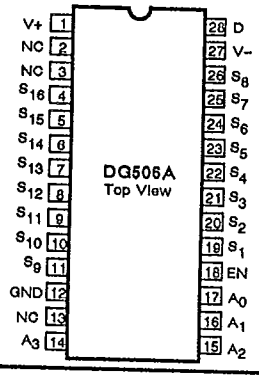
PIN CONFIGURATION

Dual-In-Line Package



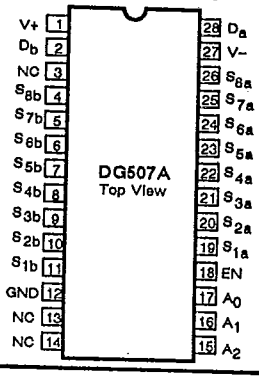
Order Numbers:

Side Braze: DG506AAR, DG506ABR, DG506ACR

CerDIP: DG506AAK, DG506ABK, DG506ACK

Plastic: DG506ACJ

Dual-In-Line Package



Order Numbers:

Side Braze: DG507AAR, DG507ABR, DG507ACR

CerDIP: DG507AAK, DG507ABK, DG507ACK

Plastic: DG507ACJ

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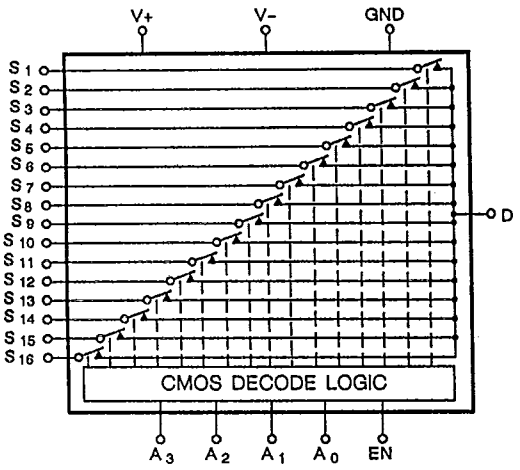
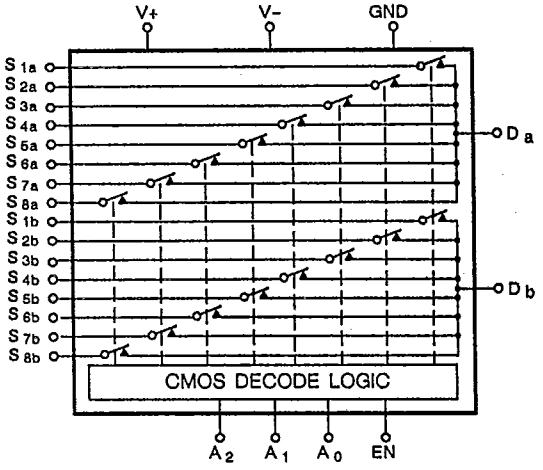
FUNCTIONAL BLOCK DIAGRAM



DG506A
16-Channel Single Ended Multiplexer



DG507A
Differential 8-Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs, V_S, V_D[h] ..... (V-) -2 V to (V+) +2 V or ..... 20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak CURRENT, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Storage Temperature (A & B Suffix) .....-65 to 150°C
(C Suffix) .....-65 to 125°C

Operating Temperature (A Suffix) .....-55 to 125°C
(D Suffix) .....-40 to 85°C
(C Suffix) .....0 to 70°C

Power Dissipation (Package)*
28-Pin Ceramic DIP** ..... 1200 mW
28-Pin Plastic DIP*** ..... 625 mW

* All leads soldered or welded to PC board.
** Derate 16 mW/°C above 75°C.
*** Derate 8.3 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		B, C SUFFIX		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH									
Analog Signal Range[c]	V_{ANALOG}		1,2,3		-15	15	-15	15	V
Drain-Source[e] ON Resistance	$r_{DS(ON)}$	$V_D = \pm 10$ V, $V_{AL} = 0.8$ V $I_S = -200$ µA, $V_{AH} = 2.4$ V	1,3 2			400 500		450 550	Ω
Greatest Change in $r_{DS(ON)}$ Between Channels[f]	$\Delta r_{DS(ON)}$	-10 V < V_S < 10 V	1	6					%

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ELECTRICAL CHARACTERISTICS [a]

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PARAMETER		SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0		LIMITS 1=25°C 2=125,85°C 3=−55,−40°C TEMP	TYP[d]	A SUFFIX −55 to 125°C MIN[b]	A SUFFIX −55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
SWITCH (Cont'd)											
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V, V_D = ∓10 V	1		−1	1	−5	5	nA
					2		−50	50	−50	50	
Drain OFF Leakage Current	DG506A	$I_{D(OFF)}$		V_D = ±10 V, V_S = ∓10 V	1		−10	10	−20	20	
					2		−300	300	−300	300	
	DG507A			V_D = ±10 V, V_S = ∓10 V	1		−5	5	−10	10	
					2		−200	200	−200	200	
Drain ON[e,g] Leakage Current	DG506A	$I_{D(ON)}$	V_S = V_D = ±10 V, V_{AL} = 0.8 V, V_{AH} = 2.4 V		1		−10	10	−20	20	
					2		−300	300	−300	300	
	DG507A				1		−5	5	−10	10	
					2		−200	200	−200	200	
INPUT											
Logic Input Current Input Voltage High		I_{AH}	V_A = 2.4 V		1		−10		−10		µA
					2		−30		−30		
			V_A = 15 V		1			10		10	
					2			30		30	
Logic Input Current Input Voltage Low		I_{AL}	V_{EN} = 0, 2.4 V, V_A = 0 V		1		−10		−10		
					2		−30		−30		
DYNAMIC											
Switching Time of Multiplexer		t_{TRANS}	See Figure 1		1	0.6		1			µs
Break-Before-Make Interval		t_{OPEN}	See Figure 3		1	0.2					ns
Enable Turn ON Time		$t_{ON(EN)}$	See Figure 2		1	1					µs
Enable Turn OFF Time		$t_{OFF(ON)}$	See Figure 2		1	0.4					
Charge Injection		Q			1	20					pC
OFF Isolation[i]			V_{EN} = 0, R_L = 1 kΩ, C_L = 15 pF, V_S = 7 V_{RMS}, f = 500 kHz		1	68					dB
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0, f = 140 kHz	V_S = 0	1	6					pF
Drain OFF Capacitance	DG506A	$C_{D(OFF)}$		V_D = 0	1	45					
	DG507A				1	23					

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ELECTRICAL CHARACTERISTICS [a]

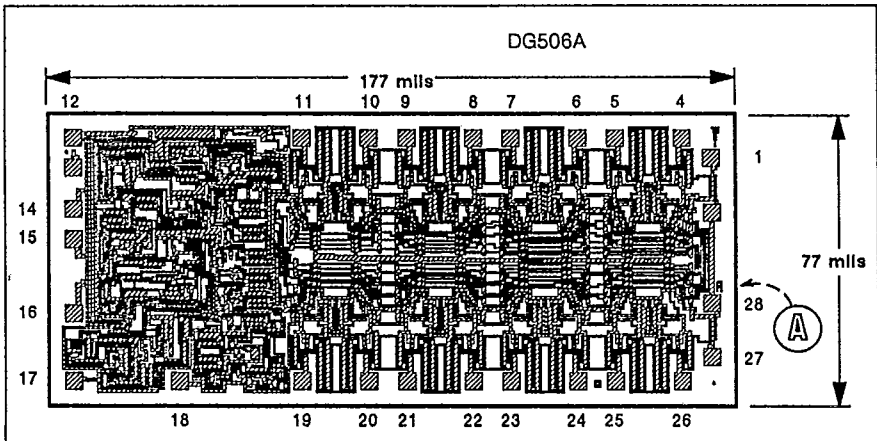
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0	1=25°C 2=125,85°C 3=-55,-40°C TEMP	TYP[d]	LIMITS A SUFFIX -55 to 125°C MIN[b]	MAX[b]	B, C SUFFIX MIN[b]	MAX[b]	UNIT
SUPPLY									
Positive Supply Current	I+	V_{EN} = 0, V_A = 0	1	1.3		2.4		2.4	mA
Negative Supply Current	I-		1	-0.7	-1.5		-1.5		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.

f. $\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)}\ MAX - r_{DS(ON)}\ MIN}{r_{DS(ON)}\ AVE} \right)$

g. $I_{D(ON)}$ is leakage from driver into "ON" switch.
h. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. OFF isolation = 20 log $\frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.

DIE TOPOGRAPHY



ICMHA-I
5 Capacitors
152 P Channel enhancement MOSFETs
8 Resistors
169 N Channel enhancement MOSFETs

Pad No.	Function
1	V+(Substrate)
4	Source 16
5	Source 15
6	Source 14
7	Source 13
8	Source 12
9	Source 11
10	Source 10
11	Source 9
12	Ground
14	Address 3
15	Address 2
16	Address 1
17	Address 0
18	Enable
19	Source 1
20	Source 2
21	Source 3
22	Source 4
23	Source 5
24	Source 6
25	Source 7
26	Source 8
27	V-
28	Drain

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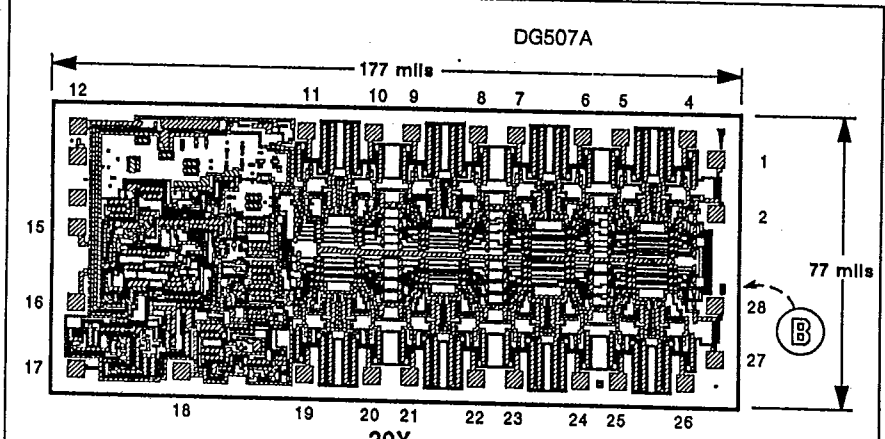
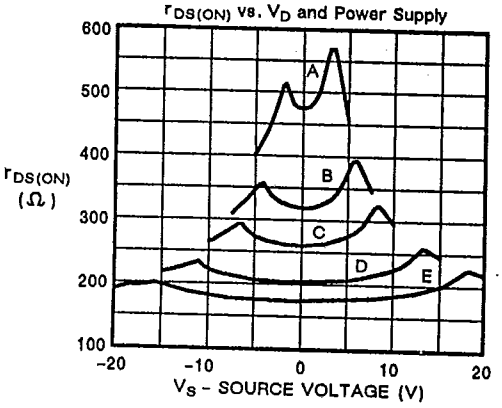
DIE TOPOGRAPHY (Cont'd)

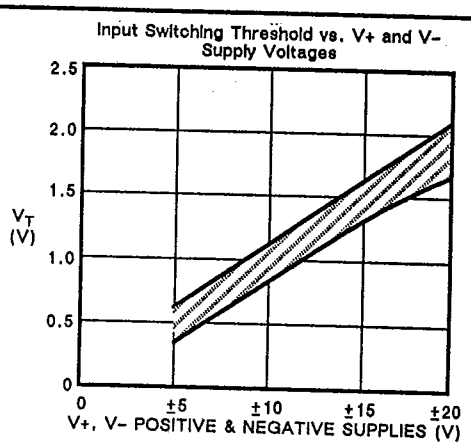


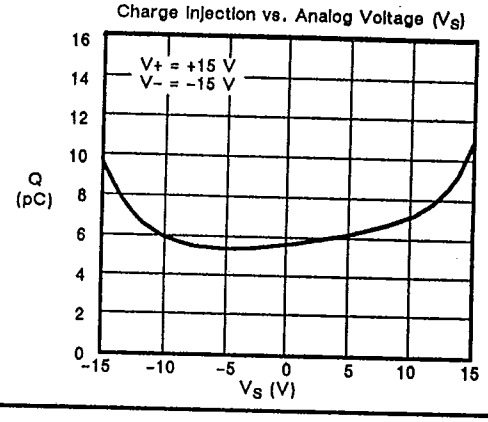
ICMHB-I
4 Capacitors
141 P Channel enhancement MOSFETs
7 Resistors
160 N Channel enhancement MOSFETs

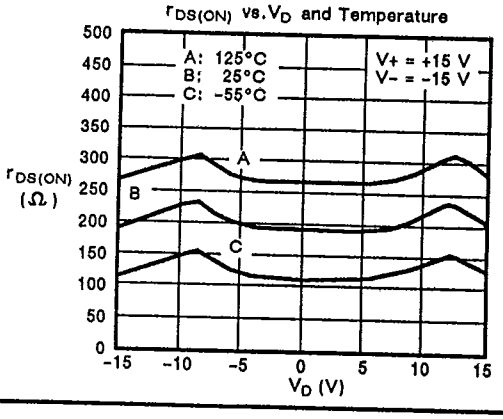
Pad No.	Function
1	V+(Substrate)
2	Drain b
4	Source 8b
5	Source 7b
6	Source 6b
7	Source 5b
8	Source 4b
9	Source 3b
10	Source 2b
11	Source 1b
12	Ground
15	Address 2
16	Address 1
17	Address 0
18	Enable
19	Source 1a
20	Source 2a
21	Source 3a
22	Source 4a
23	Source 5a
24	Source 6a
25	Source 7a
26	Source 8a
27	V-
28	Drain a

TYPICAL CHARACTERSITICS









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TYPICAL CHARACTERSITICS (Cont'd)

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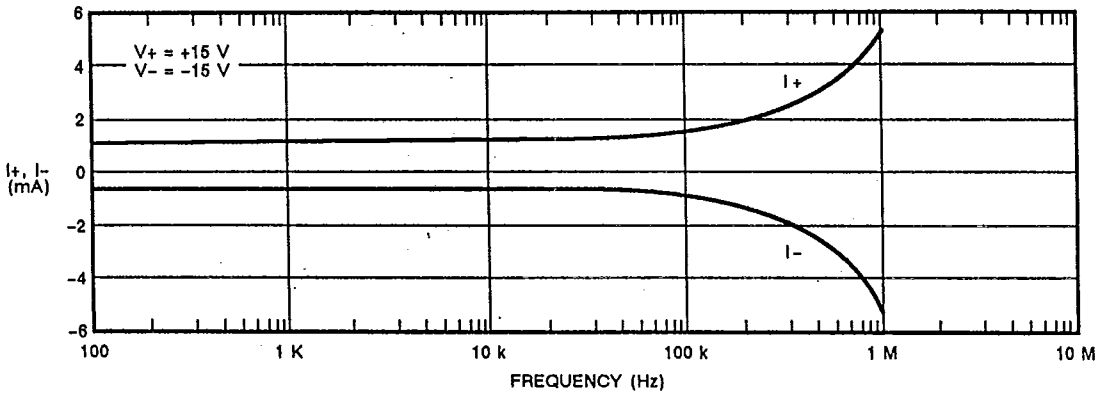
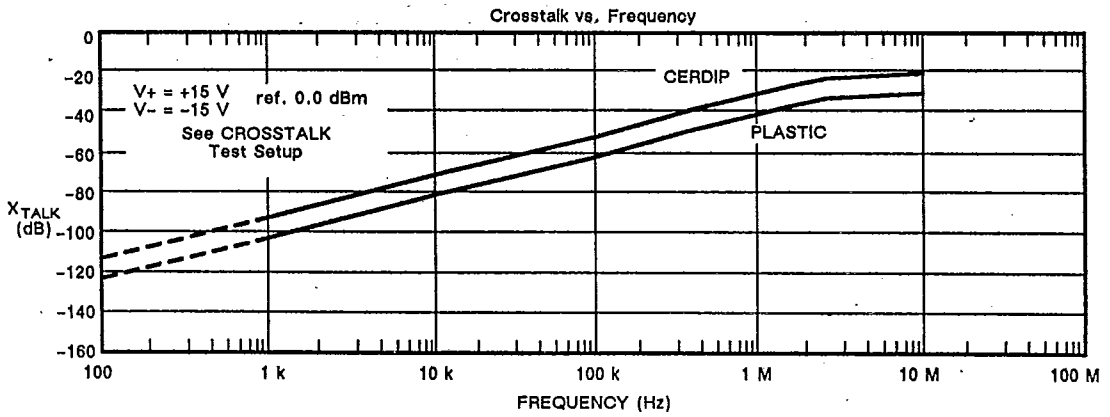
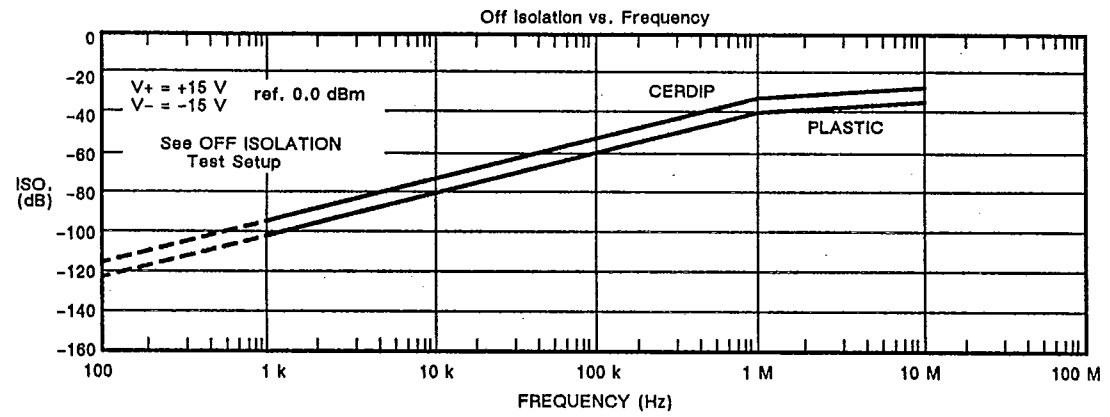
Supply Current vs. Switching Frequency



Crosstalk vs. Frequency



Off Isolation vs. Frequency



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TYPICAL CHARACTERSITICS (Cont'd)

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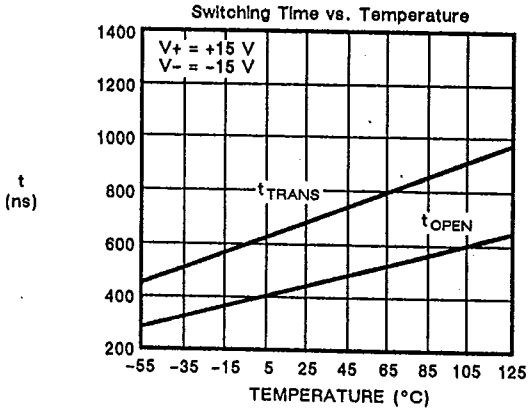
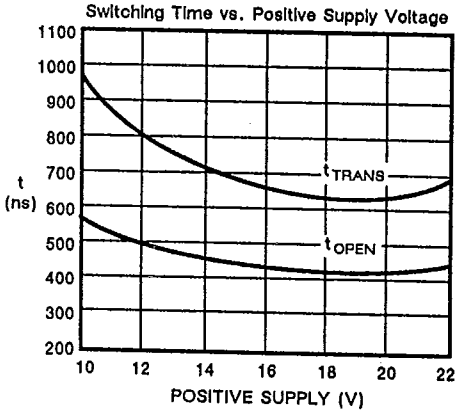
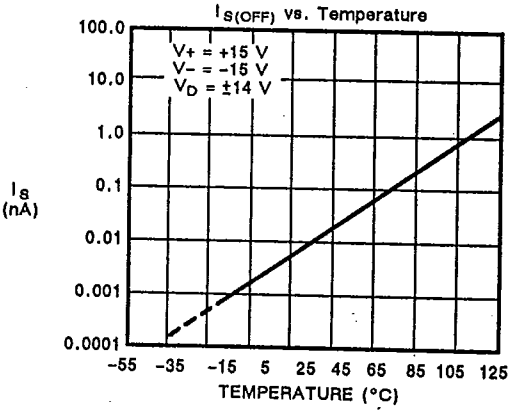
Switching Time vs. Temperature



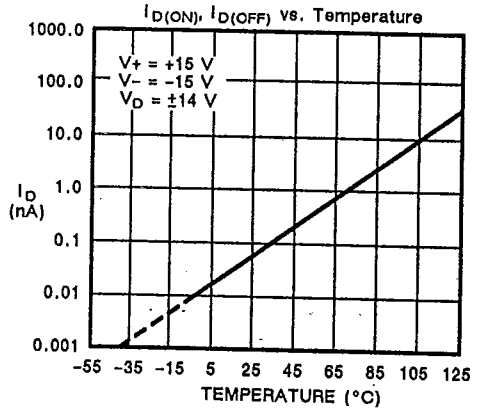
Switching Time vs. Positive Supply Voltage



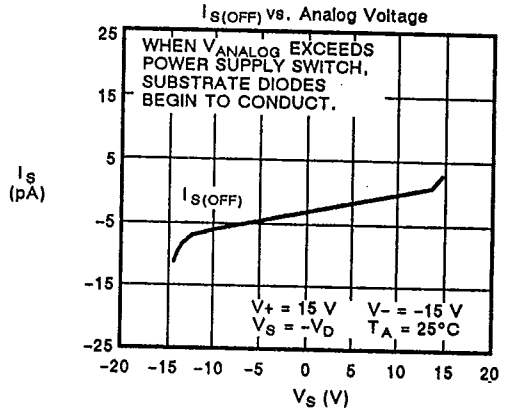
$I_{S(OFF)}$ vs. Temperature



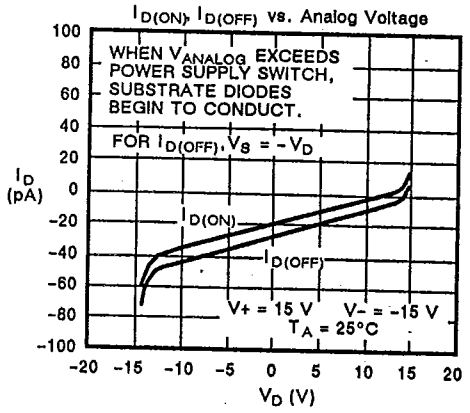
$I_{D(ON)}$, $I_{D(OFF)}$ vs. Temperature



$I_{S(OFF)}$ vs. Analog Voltage



$I_{D(ON)}$, $I_{D(OFF)}$ vs. Analog Voltage



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TRUTH TABLES

DG506A

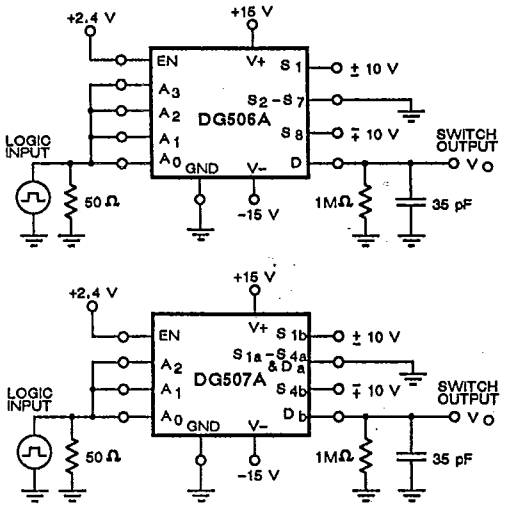
A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{AL} < 0.8 V, LOGIC "1" = V_{AH} > 2.4 V

$t_{TRANSITION}$ TIME TEST CIRCUIT



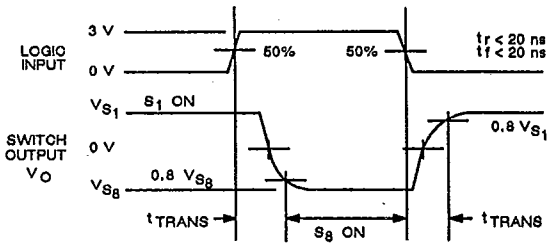


Figure 1

$t_{ON(EN)}$ AND $t_{OFF(EN)}$ TIME TEST CIRCUIT

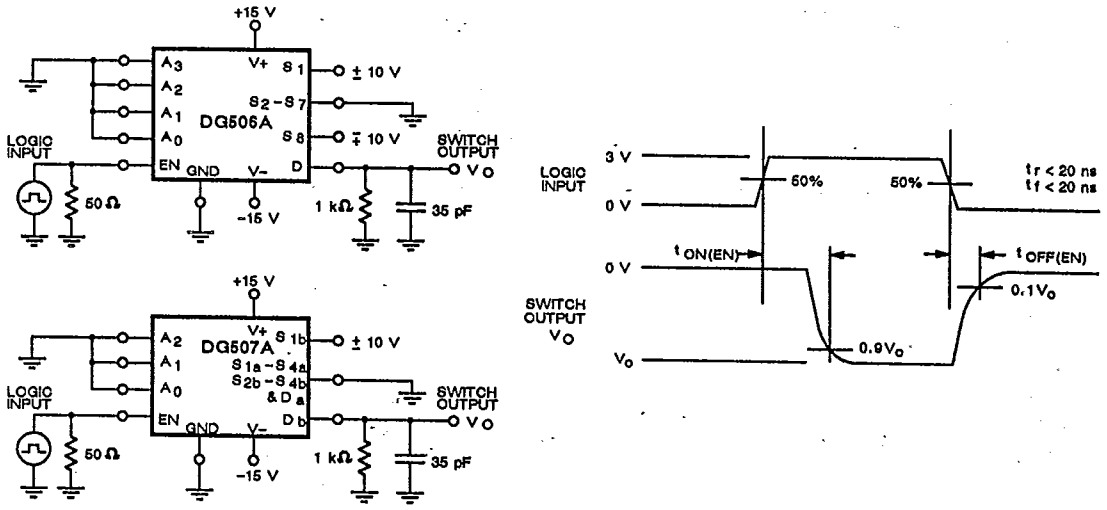


Figure 2

t_{OPEN} TIME TEST CIRCUIT

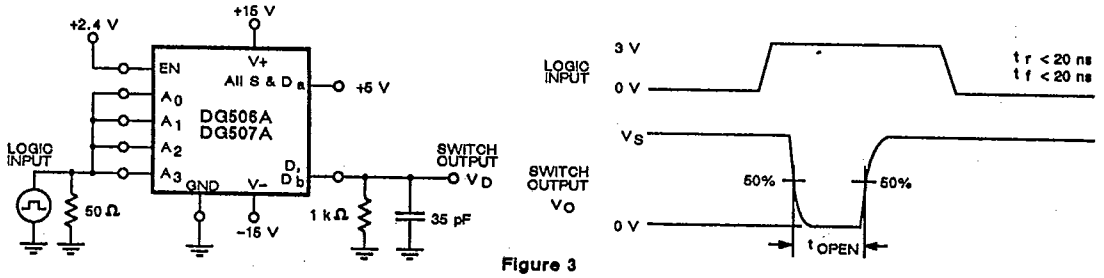
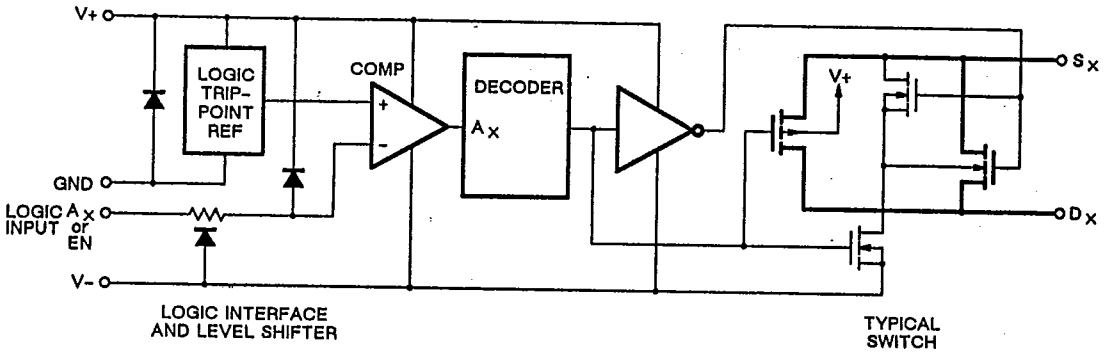


Figure 3

SCHEMATIC DIAGRAM



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APPLICATION HINTS*

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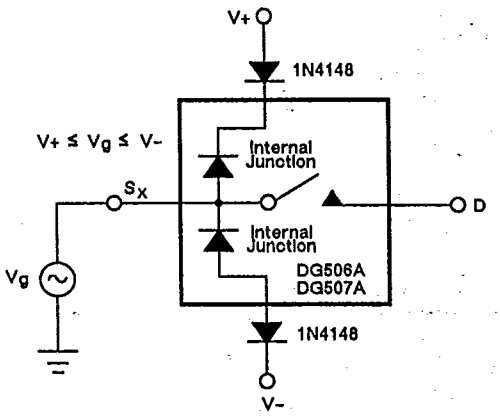
V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15 **	−15	2.4/0.8	−15 to 15
12	−12	2.4/0.6	−12 to 12
10	−10	2.4/0.5	−10 to 10
8 ***	−8	2.4/0.3	−8 to 8

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Electrical Characteristics chart based on V+ = +15 V, V− = −15 V.
*** Operation below ±8 V is not recommended due to the shift in $V_{INL(MAX)}$.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V− value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference Vs − (V−) doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V−, but it preserves the low channel resistance and low leakage characteristics.



Overvoltage Protection Using Blocking Diodes

Siliconix incorporated

DG506A/507A

APPLICATIONS

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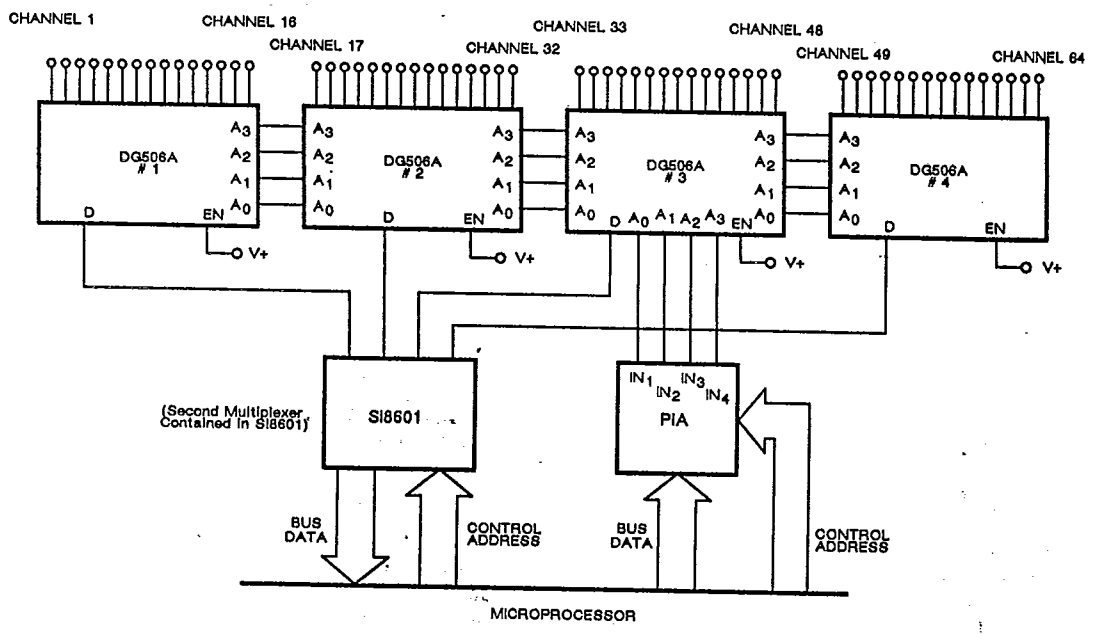

64-Channel 2-Level Multiplex System

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