8-Ch/Dual 4-Ch High-Performance CMOS Analog Multiplexers

DESCRIPTION

The DG408 is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409 is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408, DG409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see Technical Article TA201.

FEATURES

- Low on-resistance - $R_{DS(on)}$: 100 Ω
- Low charge injection - Q: 20 pC
- Fast transition time - t_{TRANS}: 160 ns
- Low power - I_{SUPPLY}: 10 µA
- Single supply capability
- 44 V supply max. rating
- TTL compatible logic

BENEFITS

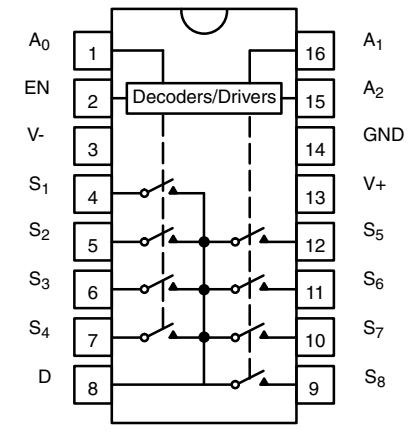
- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges (± 5 V to ± 20 V)

APPLICATIONS

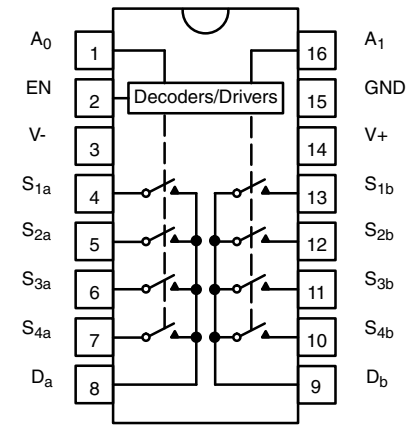
- Data acquisition systems
- Audio signal routing
- ATE systems
- Battery powered systems
- High rel systems
- Single supply systems
- Medical instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

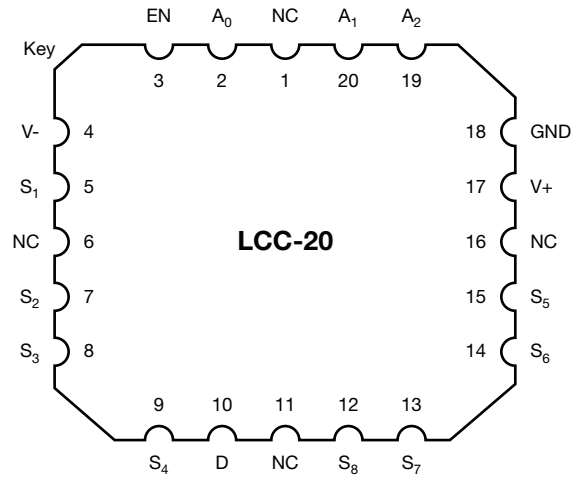
DG408 **CerDIP**
Top View



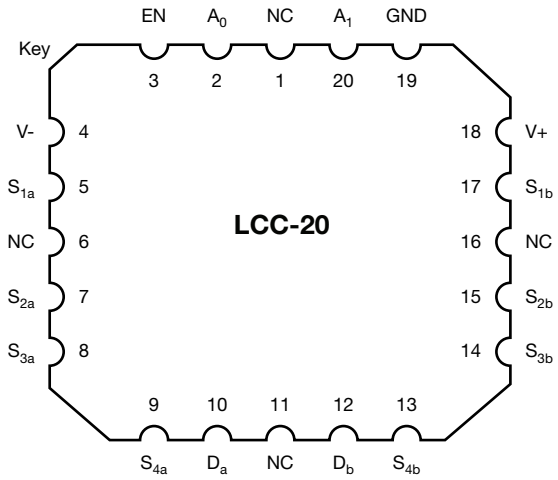
DG409 **CerDIP**
Top View



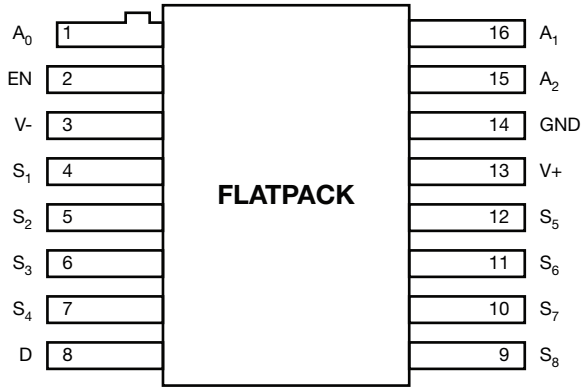
DG408 Top View



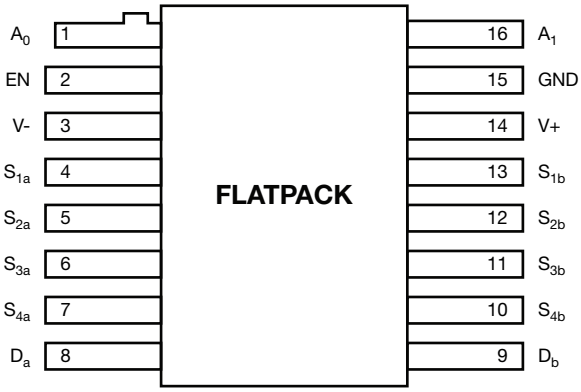
DG409 Top View



DG408 Top View



DG409 Top View



TRUTH TABLE (DG408)				
A_2	**A_1**	**A_0**	**EN**	**ON SWITCH**
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE (DG409)			
A_1	**A_0**	**EN**	**ON SWITCH**
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Notes

- Logic “0” = $V_{AL} \leq 0.8$ V
- Logic “1” = $V_{AH} \geq 2.4$ V
- X = Do not care

ORDERING INFORMATION (Hi-Rel)						
PART	CONFIGURATION	TEMP. RANGE	PACKAGE	ORDERING PART	GENERIC	DSCC NUMBER
DG408	8:1 x 1	- 55 °C to 125 °C	16-pin CerDIP	DG408AK	DG408AK	-
				DG408AK-E3	DG408AK-E3	-
				9204201EA	DG408AK/883	5962-9204201MEA
			LCC-20	92042012A	DG408AZ/883	5962-9204201M2A
				92042012C		5962-9204201M2C
			Flat-pack 16	9204201XA	DG408AL/883	5962-9204201MXA
				9204201XC		5962-9204201MXC
DG409	4:1 x 2	- 55 °C to 125 °C	16-pin CerDIP	DG409AK	DG409AK	-
				DG409AK-E3	DG409AK-E3	-
				9204202EA	DG409AK/883	5962-9204202MEA
			LCC-20	92042022A	DG409AZ/883	5962-9204202M2A
				92042022C		5962-9204202M2C
			Flat-pack 16	9204202XA	DG409AL/883	5962-9204202MXA
				9204202XC		5962-9204202MXC

Note

- Block diagram and pin configuration for Flat-pack 16 not shown.

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (any terminal)		30	mA
Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(A suffix)	- 65 to 150	°C
Power Dissipation (Package)[b]	16-pin CerDIP[c]	900	mW
	LCC-20[d]	750	

Notes

a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 12 mW/°C above 75 °C.
d. Derate 10 mW/°C above 75 °C.

SPECIFICATIONS[a]								
PARAMETER		SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = - 15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]	TEMP.[b]	TYP.[c]	A SUFFIX - 55 °C to 125 °C MIN.[d]	 MAX.[d]	UNIT
Analog Switch								
Analog Signal Range[e]		V_{ANALOG}		Full	-	- 15	15	V
Drain-Source On-Resistance		$R_{DS(on)}$	V_D = ± 10 V, I_S = - 10 mA	Room	40	-	100	Ω
				Full	-	-	125	
$R_{DS(on)}$ Matching Between Channels[g]		$\Delta R_{DS(on)}$	V_D = ± 10 V	Room	-	-	15	
Source Off Leakage Current		$I_{S(off)}$	V_S = ± 10 V, V_D = ± 10 V, V_{EN} = 0 V	Room	-	- 0.5	0.5	nA
				Full	-	- 50	50	
Drain Off Leakage Current	DG408	$I_{D(off)}$	V_D = ± 10 V, V_S = ± 10 V, V_{EN} = 0 V	Room	-	- 1	1	
	DG408			Full	-	- 100	100	
	DG409			Room	-	- 1	1	
	DG409			Full	-	- 50	50	
Drain On Leakage Current	DG408	$I_{D(on)}$	V_S = V_D = ± 10 V sequence each switch on	Room	-	- 1	1	
	DG408			Full	-	- 100	100	
	DG409			Room	-	- 1	1	
	DG409			Full	-	- 50	50	
Digital Control								
Logic High Input Voltage		V_{INH}		Full	-	2.4	-	V
Logic Low Input Voltage		V_{INL}		Full	-	-	0.8	
Logic High Input Current		I_{AH}	V_A = 2.4 V, 15 V	Full	-	- 10	10	µA
Logic Low Input Current		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V	Full	-	- 10	10	
Logic Input Capacitance		C_{in}	f = 1 MHz	Room	8	-	-	pF
Dynamic Characteristics								
Transition Time		t_{TRANS}	see figure 2	Full	160	-	250	ns
Break-Before-Make Interval		t_{OPEN}	see figure 4	Room	-	10	-	
Enable Turn-On Time		$t_{ON(EN)}$	see figure 3	Room	115	-	150	
				Full	-	-	225	
Enable Turn-Off Time		$t_{OFF(EN)}$		Room	105	-	150	
Charge Injection		Q	C_L = 10 nF, V_S = 0 V	Room	20	-	-	pC
Off Isolation[h]		OIRR	V_{EN} = 0 V, R_L = 1 kΩ, f = 1 MHz	Room	- 75	-	-	pF
Source Off Capacitance		$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz	Room	3	-	-	
Drain Off Capacitance	DG408	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V, f = 1 MHz	Room	26	-	-	
	DG409			Room	14	-	-	
Drain On Capacitance	DG408	$C_{D(on)}$		Room	37	-	-	
	DG409			Room	25	-	-	
Power Supplies								
Positive Supply Current		I+	V_{EN} = V_A = 0 V or 5 V	Full	10	-	75	µA
Negative Supply Current		I-		Full	1	- 75	-	
Positive Supply Current		I+	V_{EN} = V_A = 0 V or 5 V	Room	0.2	-	0.5	mA
				Full	-	-	2	
Negative Supply Current		I-		Full	-	- 500	-	µA

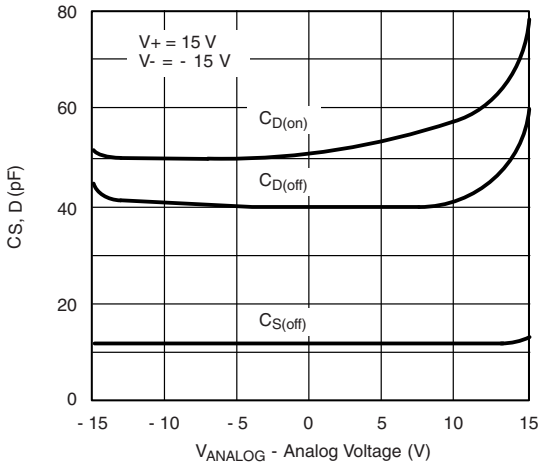
SPECIFICATIONS[a] (Single Supply)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** **V+ = 12 V, V- = 0 V** **V_{AL} = 0.8 V, V_{AH} = 2.4 V[F]**	**TEMP.[b]**	**TYP.[c]**	**A SUFFIX - 55 °C to 125 °C**		**UNIT**
					MIN.[d]	**MAX.[d]**	
Analog Switch							
Drain-Source On-Resistance[e, f]	$R_{DS(on)}$	V_D = 3 V, 10 V, I_S = - 1 mA	Room	90	-	-	Ω
Dynamic Characteristics							
Switching Time of Multiplexer[e]	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V	Room	180	-	-	ns
Enable Turn-On Time[e]	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V, V_{S1} = 5 V	Room	180	-	-	
Enable Turn-Off Time[e]	$t_{OFF(EN)}$		Room	120	-	-	
Charge Injection[e]	Q	C_L = 1 nF, V_S = 0 V, R_S = 0	Room	5	-	-	pC

Notes

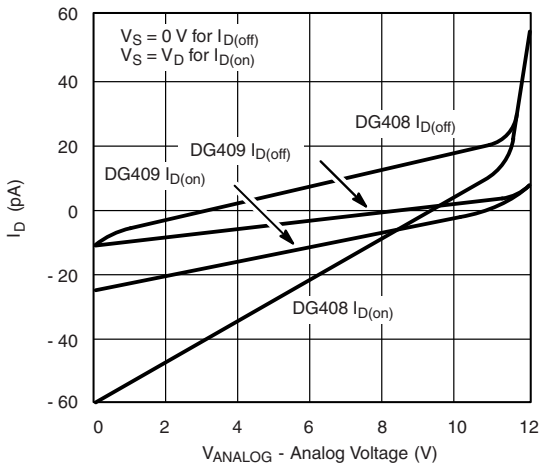
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 due to proximity to the drain pin.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

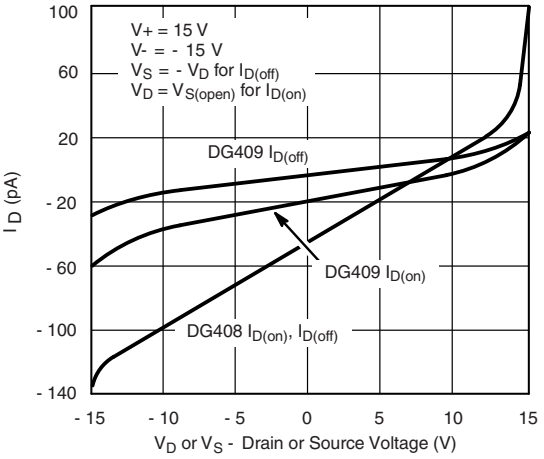
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



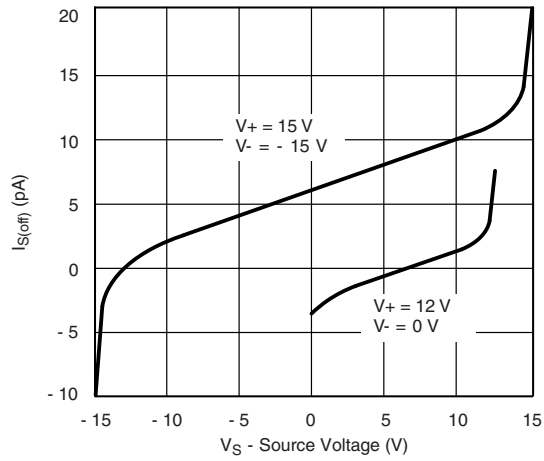
Source/Drain Capacitance vs. Analog Voltage



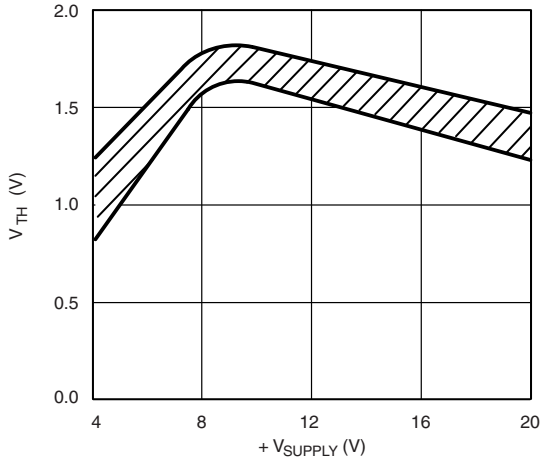
Drain Leakage Current vs. Source/Drain Voltage (Single 12 V Supply)



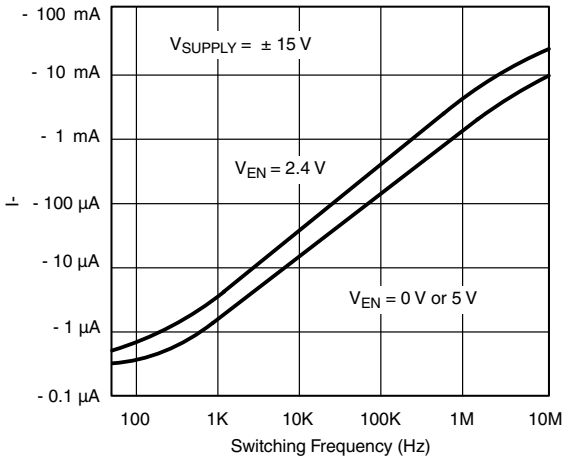
Drain Leakage Current vs. Source/Drain Voltage



Source Leakage Current vs. Source Voltage

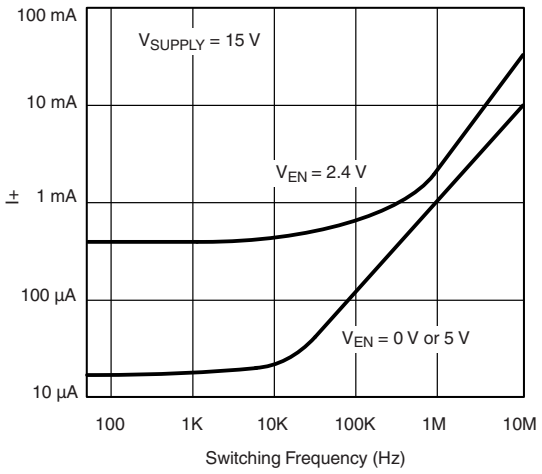


Input Switching Threshold vs. Supply Voltage

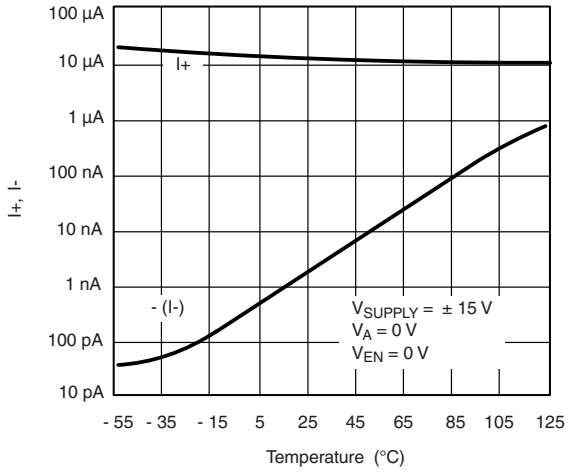


Negative Supply Current vs. Switching Frequency

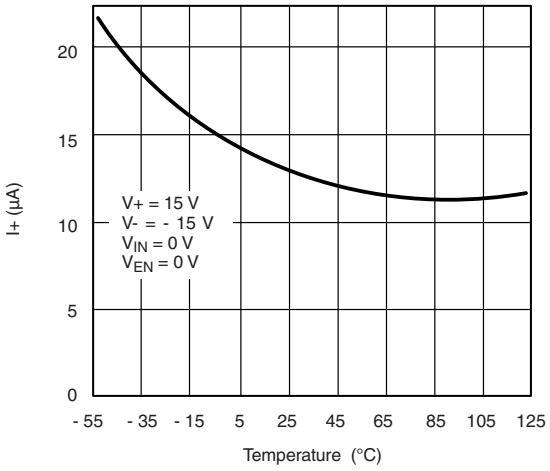
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



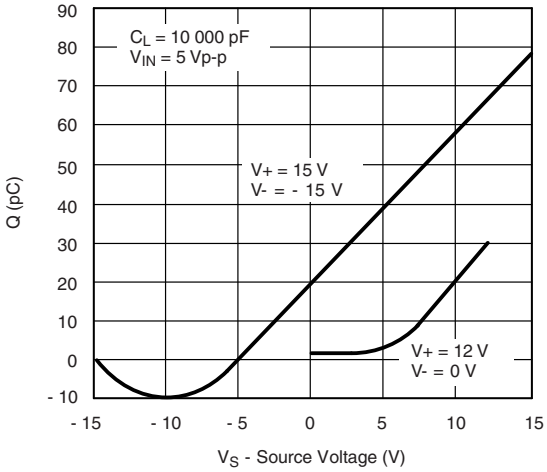
Positive Supply Current vs. Switching Frequency



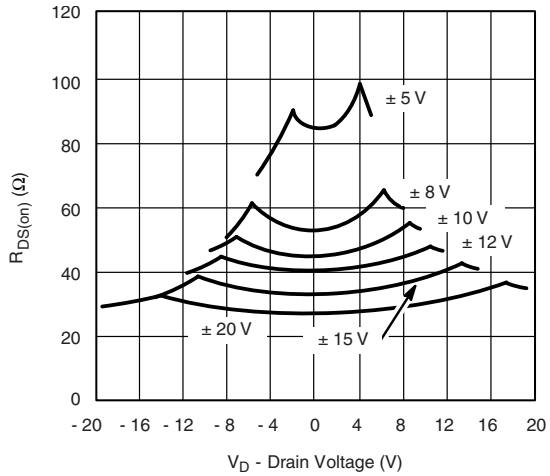
I_{SUPPLY} vs. Temperature



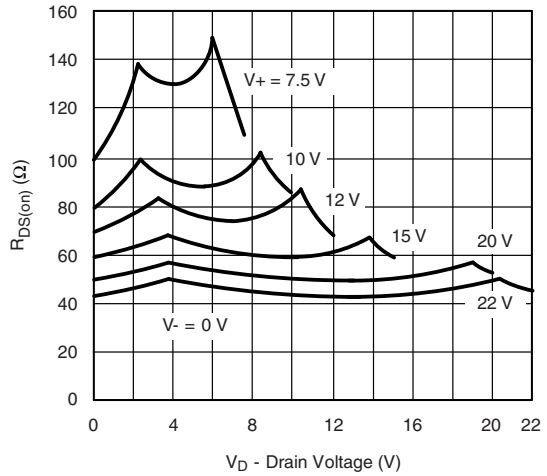
Positive Supply Current vs. Temperature (DG408)



Charge Injection vs. Analog Voltage

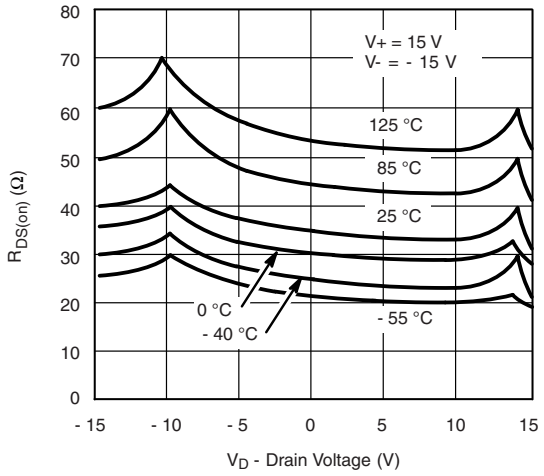


$R_{DS(on)}$ vs. V_D and Supply

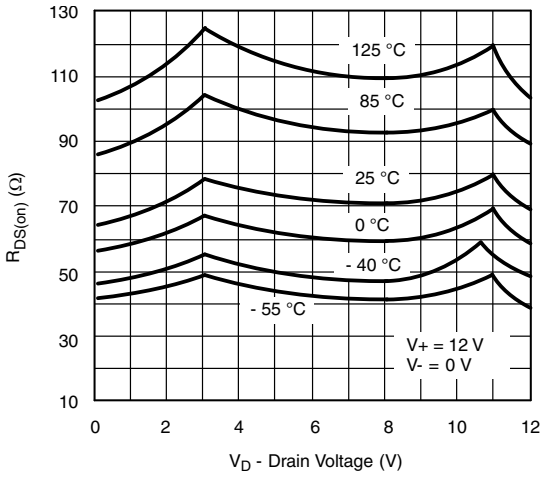


$R_{DS(on)}$ vs. V_D and Supply (Single Supply)

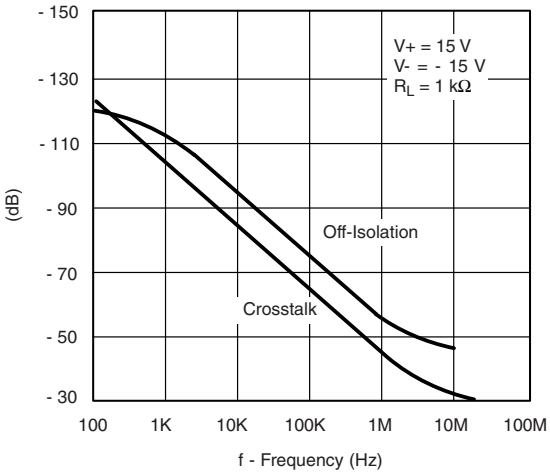
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



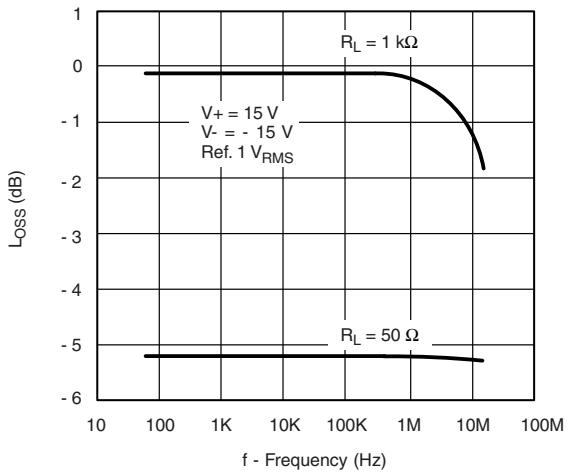
$R_{DS(on)}$ vs. V_D and Temperature



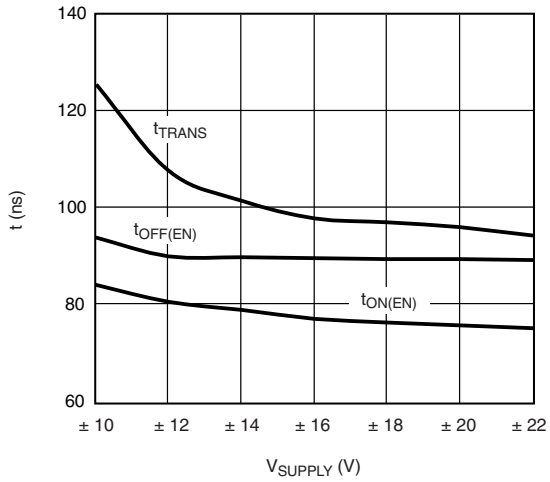
$R_{DS(on)}$ vs. V_D and Temperature (Single Supply)



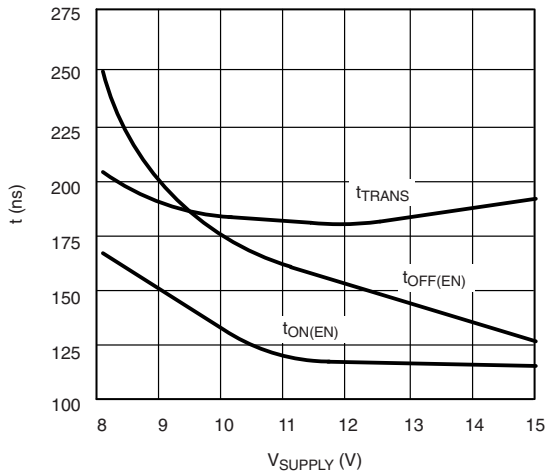
Off Isolation and Crosstalk vs. Frequency



Insertion Loss vs. Frequency



Switching Time vs. Bipolar Supply



Switching Time vs. Single Supply

SCHEMATIC DIAGRAM (Typical Channel)

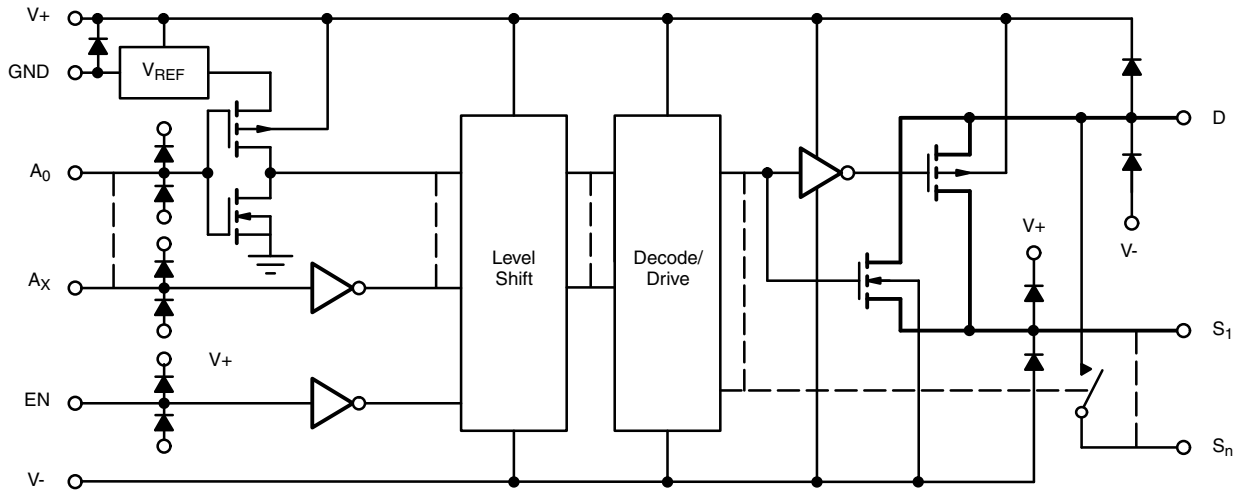
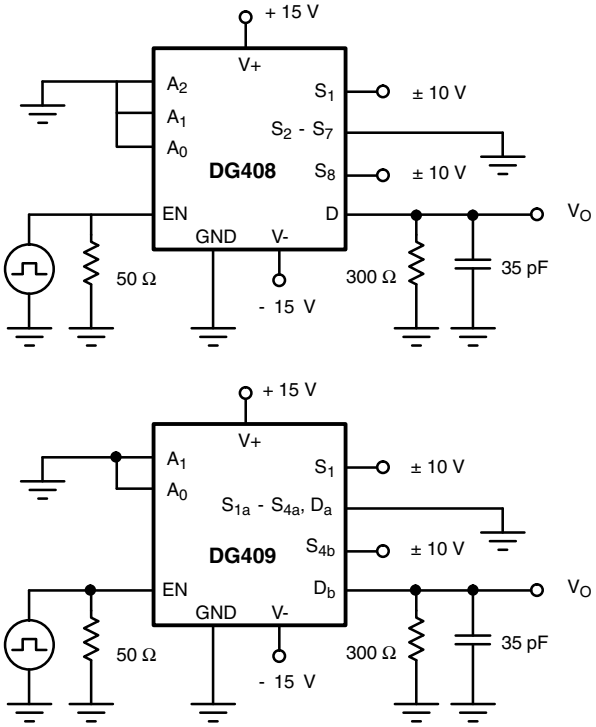


Fig. 1

TEST CIRCUITS



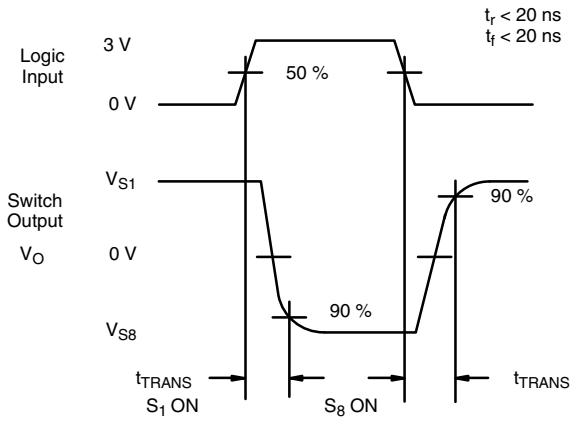


Fig. 2 - Transition Time

TEST CIRCUITS

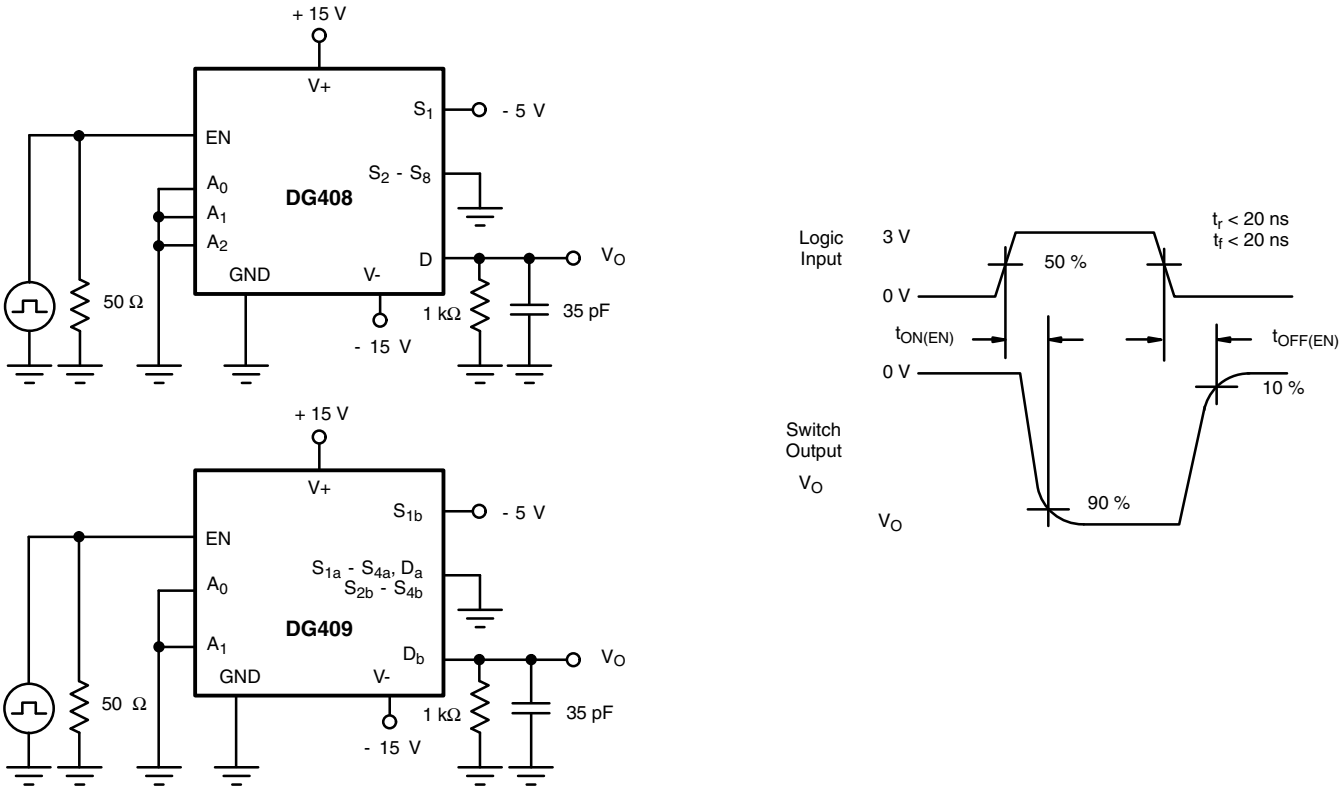


Fig. 3 - Enable Switching Time

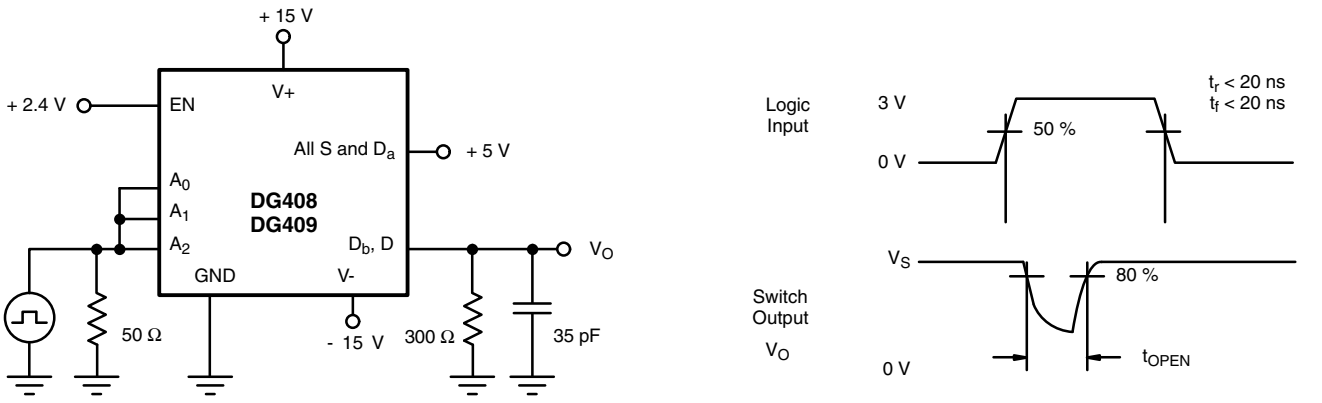


Fig. 4 - Break-Before-Make Interval

TEST CIRCUITS

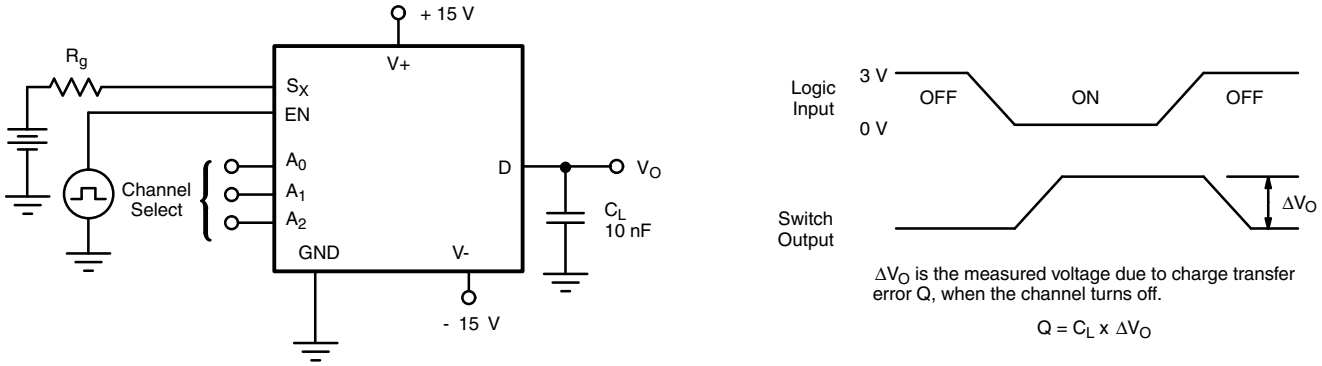


Fig. 5 - Charge Injection

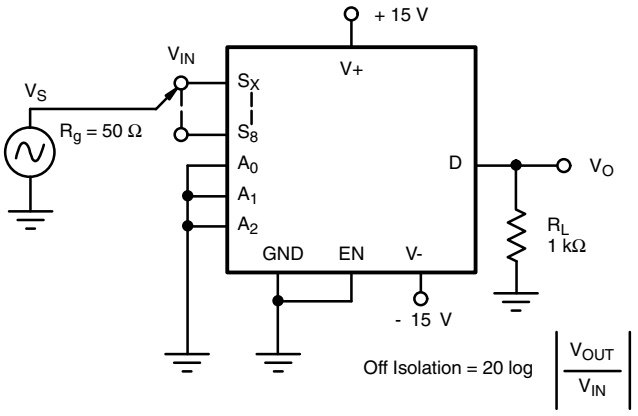


Fig. 6 - Off Isolation

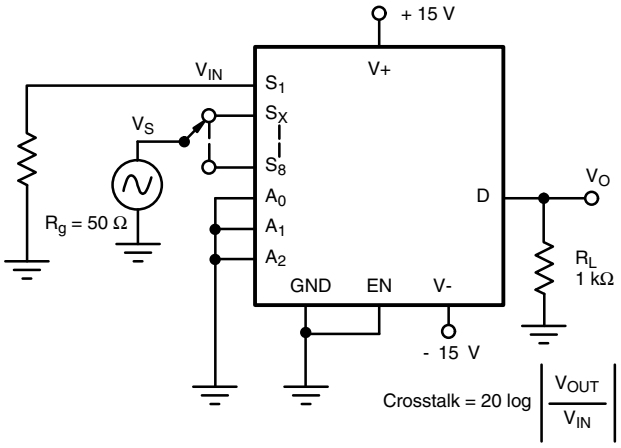


Fig. 7 - Crosstalk

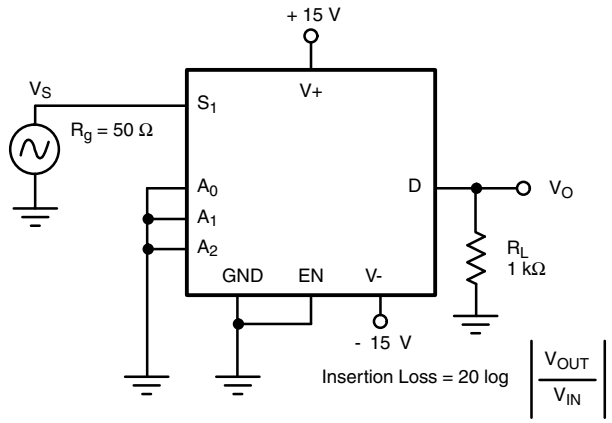


Fig. 8 - Insertion Loss

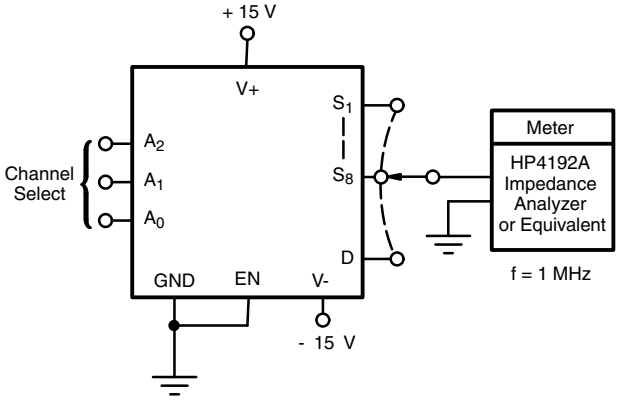


Fig. 9 - Source Drain Capacitance

APPLICATION HINTS

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference VS - (V-) does not exceed + 44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

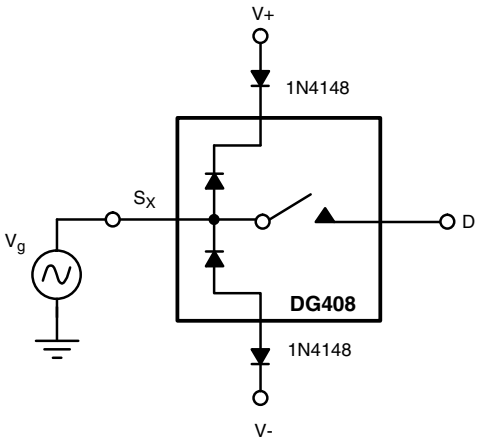
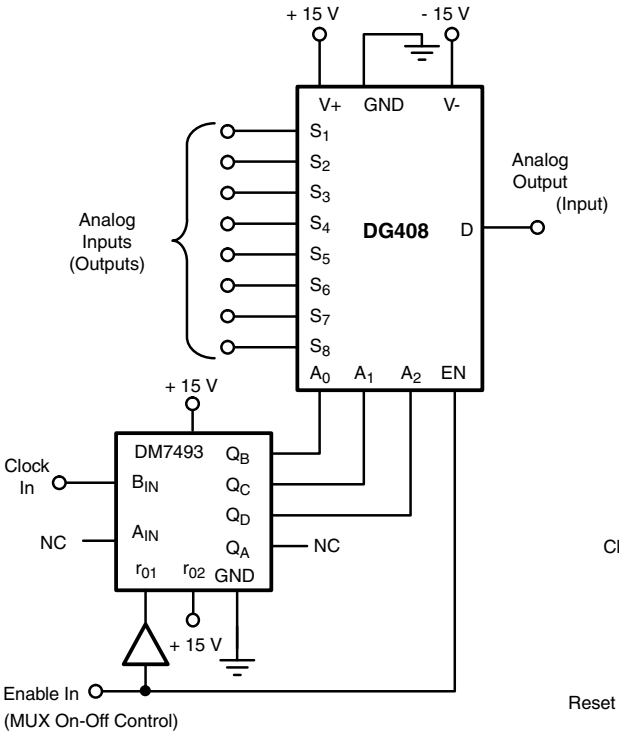


Fig. 10 - Overvoltage Protection Using Blocking Diodes

8-Channel Sequential Multiplexer/Demultiplexer



Differential 4-Channel Sequential Multiplexer/Demultiplexer

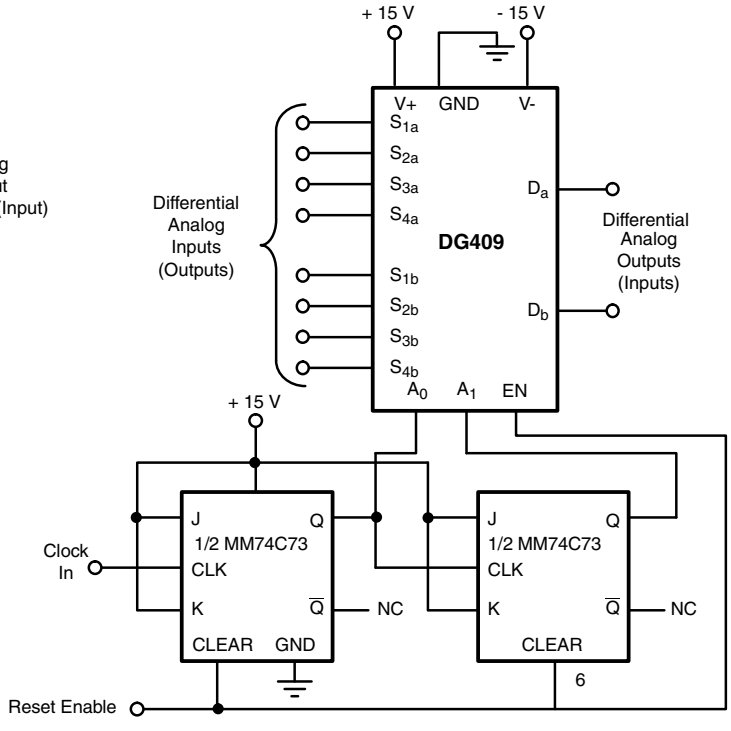
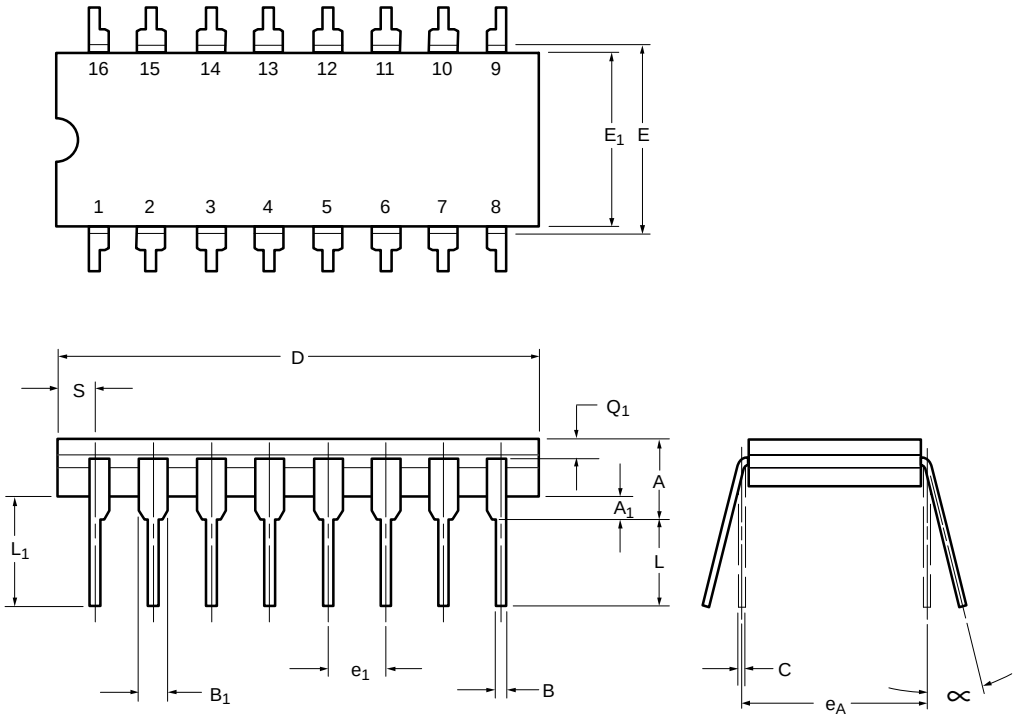


Fig. 11

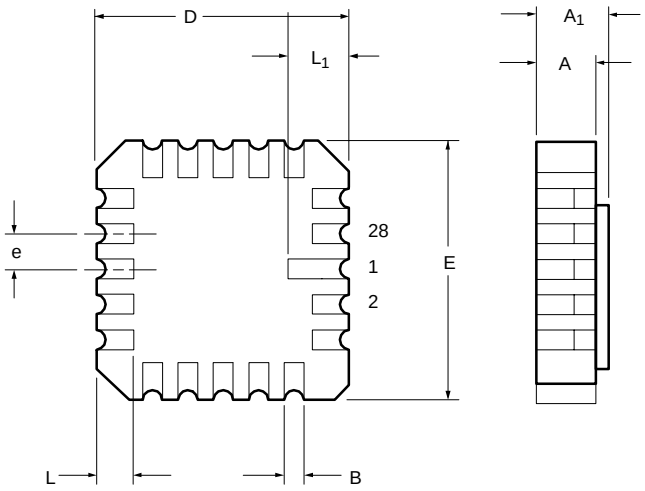
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70062.

CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∝	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5403				

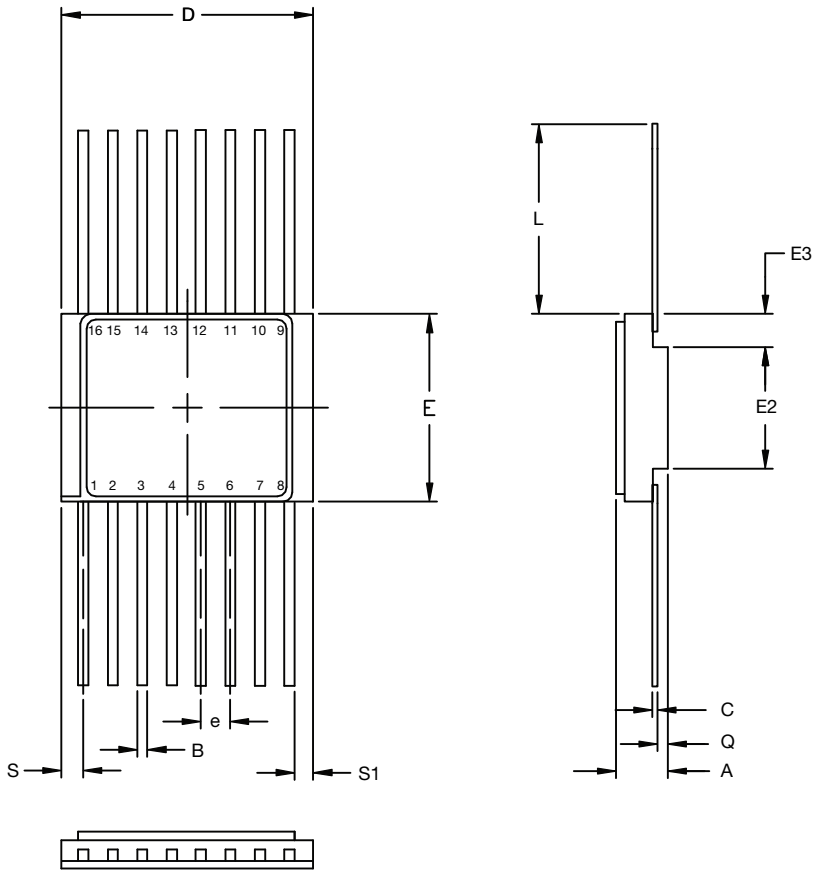
20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A_1	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L_1	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

Flat Pack: 16 Leads



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.52	2.54	0.060	0.100
B	0.38	0.48	0.015	0.019
C	0.10	0.15	0.004	0.006
D	9.91	10.41	0.390	0.410
E	6.60	7.11	0.260	0.280
E2	4.45	4.95	0.175	0.195
E3	0.76	1.27	0.030	0.050
e	1.27 BSC		0.050 BSC	
L	7.62	8.89	0.300	0.350
Q	0.66	1.14	0.026	0.045
S	-	1.14	-	0.045
S1	0.013	-	0.005	-
ECN: S15-1674-Rev. D, 27-Jul-15 DWG: 5343				

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