# 16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

## DESCRIPTION

The DG406B is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407B selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address ($A_x$) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406B, DG407B include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V, allowing operation with ± 20 V supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

## FEATURES

- Low on-resistance - $R_{DS(on)}$: 45 Ω
- Low charge injection - Q: 11 pC
- Fast transition time - $t_{TRANS}$: 115 ns
- Low power: 0.2 mW
- Single supply capability
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available

RoHS* Available

**Note**

* This datasheet provides information about parts that are RoHS-compliant and/or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information/tables in this datasheet for details.

## BENEFITS

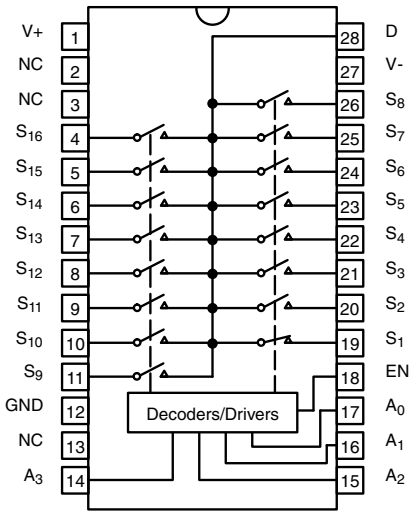
- Higher accuracy
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges: ± 5 V to ± 20 V

## APPLICATIONS

- Data acquisition systems
- Audio signal routing
- Medical instrumentation
- ATE systems
- Battery powered systems
- High-rel systems
- Single supply systems

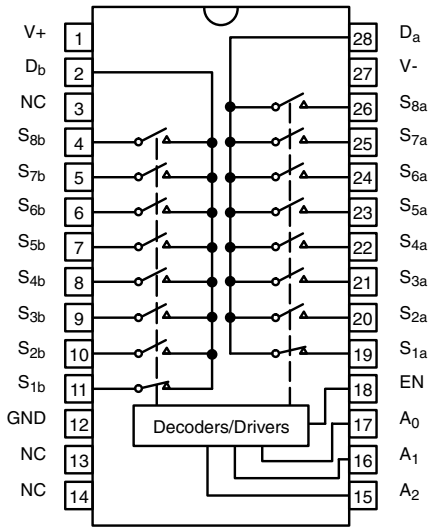
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG406B** Dual-In-Line and SOIC Wide-Body




Top View

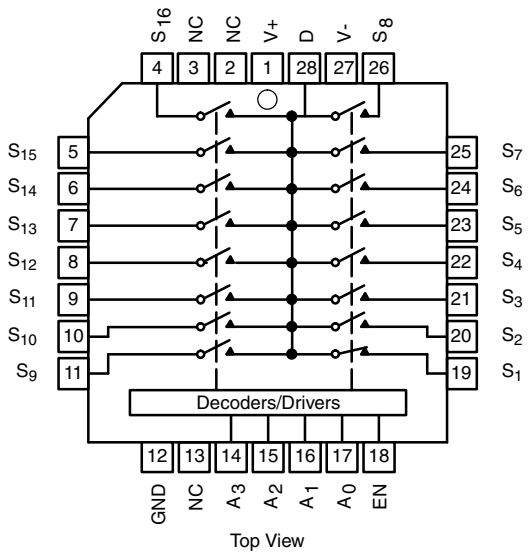
**DG407B** Dual-In-Line and SOIC Wide-Body




Top View

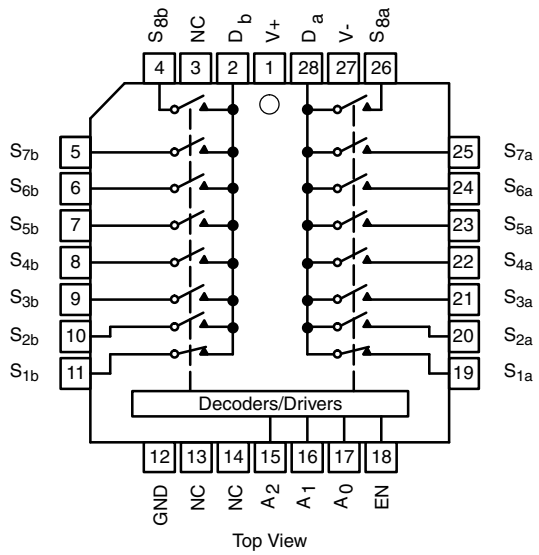
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406B PLCC and LCC




Top View

DG407B PLCC and LCC




Top View

**TRUTH TABLE** (DG406B)

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH |
|---|---|---|---|---|---|
| X | X | X | X | 0 | None |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 2 |
| 0 | 0 | 1 | 0 | 1 | 3 |
| 0 | 0 | 1 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 1 | 9 |
| 1 | 0 | 0 | 1 | 1 | 10 |
| 1 | 0 | 1 | 0 | 1 | 11 |
| 1 | 0 | 1 | 1 | 1 | 12 |
| 1 | 1 | 0 | 0 | 1 | 13 |
| 1 | 1 | 0 | 1 | 1 | 14 |
| 1 | 1 | 1 | 0 | 1 | 15 |
| 1 | 1 | 1 | 1 | 1 | 16 |

**TRUTH TABLE** (DG407B)

| $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH |
|---|---|---|---|---|
| X | X | X | 0 | None |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

**Notes**

- Logic “0” = $V_{AL} \leq 0.8$ V
- Logic “1” = $V_{AH} \geq 2.4$ V
- X = Do not care

**ORDERING INFORMATION** (DG406B)

| TEMP. RANGE | PACKAGE | PART NUMBER |
|---|---|---|
| -40 °C to 85 °C | 28-Pin Plastic DIP | DG406BDJ, DG406BDJ-E3 |
| | 28-Pin PLCC | DG406BDN, DG406BDN-T1-E3 |
| | 28-Pin Widebody SOIC | DG406BDW, DG406BDW-E3, DG406BDW-T1-E3 |

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**Note**

- -T1 indicates Tape and Reel, -E3 indicates Lead-Free and RoHS Compliant, NO -E3 indicates standard Tin/Lead finish.

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | LIMIT | UNIT |
|---|---|---|---|
| Voltages Referenced to V- | V+ to V-[g] | 44 | V |
| | GND to V- | -25 | |
| Digital Inputs[a], $V_S$, $V_D$ | | (V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first | |
| Current (any terminal) | | 30 | mA |
| Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle max.) | | 100 | |
| Storage Temperature | | -65 to 150 | °C |
| Power Dissipation (Package)[b] | 28-Pin Plastic DIP[c] | 625 | mW |
| | 28-Pin Plastic PLCC[c] | 450 | mW |
| | 28-Pin Widebody SOIC[f] | 450 | mW |

**Notes**

a. Signals on $S_X$, $D_X$ or $IN_X$ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 8.3 mW/°C above 75 °C.
d. Derate 16 mW/°C above 75 °C.
e. Derate 18 mW/°C above 75 °C.
f. Derate 6 mW/°C above 75 °C.
g. Also applies when V- = GND.

## SPECIFICATIONS

| PARAMETER | | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V $V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V[f] | TEMP.[b] | TYP.[c] | D SUFFIX -40 °C to 85 °C MIN.[d] | D SUFFIX -40 °C to 85 °C MAX.[d] | UNIT |
|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | |
| Analog Signal Range[e] | | $V_{ANALOG}$ | | Full | - | -15 | 15 | V |
| Drain-Source On-Resistance | | $R_{DS(on)}$ | $V_D$ = ± 10 V, $I_S$ = -10 mA sequence each switch on | Room | 45 | - | 60 | Ω |
| | | | | Full | 45 | - | 74 | |
| $R_{DS(on)}$ Matching Between Channels[g] | | $\Delta R_{DS(on)}$ | $V_D$ = ± 10 V | Room | 5 | - | - | % |
| Source Off Leakage Current | | $I_{S(off)}$ | $V_S$ = ± 10 V, $V_D$ = ± 10 V, $V_{EN}$ = 0 V | Room | - | -0.5 | 0.5 | nA |
| | | | | Full | - | -5 | 5 | |
| Drain Off Leakage Current | DG406B | $I_{D(off)}$ | $V_D$ = ± 10 V, $V_S$ = ± 10 V, $V_{EN}$ = 0 V | Room | - | -1 | 1 | |
| | | | | Full | - | -40 | 40 | |
| | DG407B | | | Room | - | -1 | 1 | |
| | | | | Full | - | -20 | 20 | |
| Drain On Leakage Current | DG406B | $I_{D(on)}$ | $V_S$ = $V_D$ = ± 10 V sequence each switch on | Room | - | -1 | 1 | |
| | | | | Full | - | -40 | 40 | |
| | DG407B | | | Room | - | -1 | 1 | |
| | | | | Full | - | -20 | 20 | |
| **Digital Control** | | | | | | | | |
| Logic High Input Voltage | | $V_{INH}$ | | Full | - | 2.4 | - | V |
| Logic Low Input Voltage | | $V_{INL}$ | | Full | - | - | 0.8 | |
| Logic High Input Current | | $I_{AH}$ | $V_A$ = 2.4 V, 15 V | Full | - | -1 | 1 | µA |
| Logic Low Input Current | | $I_{AL}$ | $V_{EN}$ = 0 V, 2.4 V, $V_A$ = 0 V | Full | - | -1 | 1 | |
| Logic Input Capacitance | | $C_{in}$ | f = 1 MHz | Room | 6 | - | - | pF |

## SPECIFICATIONS

| PARAMETER | | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED<br>V+ = 15 V, V- = -15 V<br>$V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V[f] | TEMP.[b] | TYP.[c] | D SUFFIX -40 °C to 85 °C<br>MIN.[d] | <br>MAX.[d] | UNIT |
|---|---|---|---|---|---|---|---|---|
| **Dynamic Characteristics** | | | | | | | | |
| Transition Time | | $t_{TRANS}$ | see figure 2 | Room | 115 | - | 148 | ns |
| | | | | Full | - | - | 161 | |
| Break-Before-Make Interval | | $t_{OPEN}$ | see figure 4 | Room | 39 | 10 | - | |
| | | | | Full | - | 21 | - | |
| Enable Turn-On Time | | $t_{ON(EN)}$ | see figure 3 | Room | 75 | - | 107 | |
| | | | | Full | - | - | 123 | |
| Enable Turn-Off Time | | $t_{OFF(EN)}$ | | Room | 50 | - | 88 | |
| | | | | Full | - | - | 94 | |
| Charge Injection | | Q | $C_L$ = 1 nF, $V_S$ = 0 V<br>$R_S$ = 0 Ω | Room | 11 | - | - | pC |
| Off Isolation[h] | | OIRR | $V_{EN}$ = 0 V, $R_L$ = 50 Ω,<br>f = 1 MHz | Room | -86 | - | - | dB |
| Source Off Capacitance | | $C_{S(off)}$ | $V_{EN}$ = 0 V, $V_S$ = 0 V,<br>f = 1 MHz | Room | 6 | - | - | pF |
| Drain Off Capacitance | | $C_{D(off)}$ | $V_{EN}$ = 0 V,<br>$V_D$ = 0 V,<br>f = 1 MHz | Room | 108 | - | - | |
| | DG407B | | | Room | 54 | - | - | |
| Drain On Capacitance | DG406B | $C_{D(on)}$ | | Room | 114 | - | - | |
| | DG407B | | | Room | 57 | - | - | |
| **Power Supplies** | | | | | | | | |
| Positive Supply Current | | I+ | $V_{EN}$ = $V_A$ = 0 V or 5 V | Room | 23 | - | 30 | µA |
| | | | | Full | - | - | 75 | |
| Negative Supply Current | | I- | | Room | -0.02 | -1 | - | |
| | | | | Full | - | -10 | - | |
| Positive Supply Current | | I+ | $V_{EN}$ = 2.4 V, $V_A$ = 0 V | Room | 28 | - | 500 | |
| | | | | Full | - | - | 700 | |
| Negative Supply Current | | I- | | Room | -0.01 | -20 | - | |
| | | | | Full | - | -20 | - | |

**Notes**

a. Guaranteed by ± 15 V leakage test, not production tested.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 due to proximity to the drain pin.

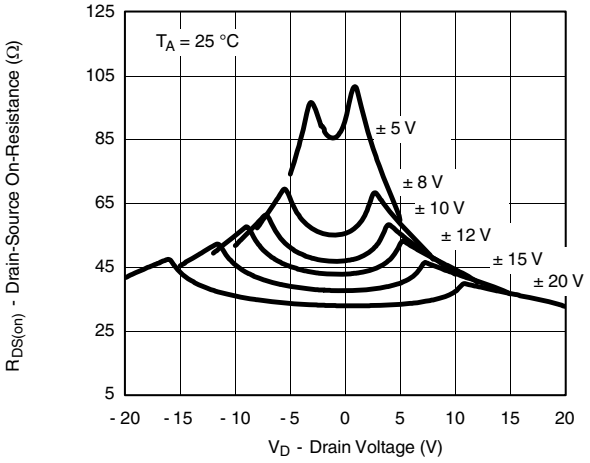
| SPECIFICATIONS FOR SINGLE SUPPLY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED<br>V+ = 15 V, V- = -15 V<br>$V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V[f] | TEMP.[b] | TYP.[c] | D SUFFIX -40 °C to 85 °C<br>MIN.[d] | <br>MAX.[d] | UNIT |
| **Analog Switch** | | | | | | | | |
| Analog Signal Range[e] | | $V_{ANALOG}$ | | Full | - | 0 | 12 | V |
| Drain-Source On-Resistance | | $R_{DS(on)}$ | $V_D$ = 3 V, $I_S$ = -1 mA sequence each switch on | Room | 78 | - | 100 | Ω |
| $R_{DS(on)}$ Matching Between Channels[g] | | $\Delta R_{DS(on)}$ | | Room | 5 | - | - | % |
| Source Off Leakage Current[a] | | $I_{S(off)}$ | $V_D$ = 10 V or 0.5 V, $V_S$ = 0.5 V or 10 V, $V_{EN}$ = 0 V | Room | - | -0.5 | 0.5 | nA |
| Drain Off Leakage Current | DG406B | $I_{D(off)}$ | | Room | - | -1 | 1 | |
| | DG407B | | | Room | - | -1 | 1 | |
| Drain On Leakage Current | DG406B | $I_{D(on)}$ | $V_S$ = $V_D$ = ± 10 V sequence each switch on | Room | - | -1 | 1 | |
| | DG407B | | | Room | - | -1 | 1 | |
| **Dynamic Characteristics** | | | | | | | | |
| Transition Time | | $t_{TRANS}$ | $V_{S1}$ = 8 V, $V_{S8}$ = 0 V, $V_{IN}$ = 2.4 V | Room | 130 | - | 163 | ns |
| Enable Turn-On Time | | $t_{ON(EN)}$ | $V_{INH}$ = 2.4 V, $V_{INL}$ = 0 V, $V_{IN}$ = 5 V | Room | 93 | - | 125 | |
| Enable Turn-Off Time | | $t_{OFF(EN)}$ | | Room | 63 | - | 94 | |
| Charge Injection | | Q | $C_L$ = 1 nF, $V_S$ = 6 V $R_S$ = 0 Ω | Room | 9 | - | - | pC |
| **Power Supplies** | | | | | | | | |
| Positive Supply Current | | I+ | $V_{EN}$ = 0 V or 5 V $V_A$ = 0 V or 5 V | Room | 13 | - | 30 | µA |
| | | | | Full | - | - | 75 | |
| Positive Supply Current | | I+ | | Room | -0.01 | -20 | - | |
| | | | | Full | - | -20 | - | |

**Notes**

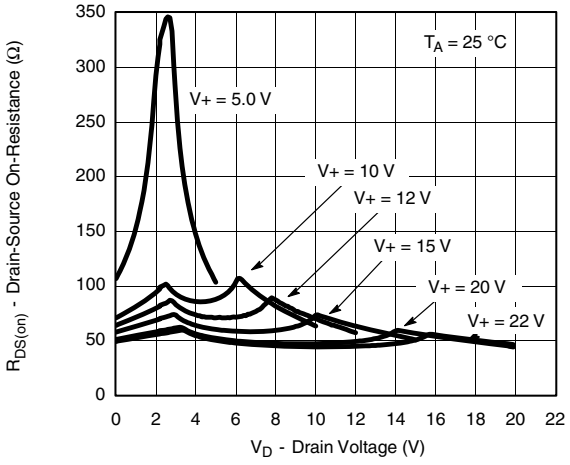
a. Guaranteed by ± 15 V leakage test, not production tested.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 due to proximity to the drain pin.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

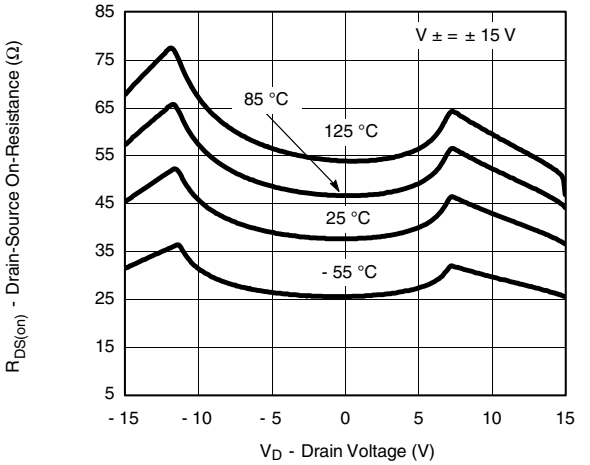
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



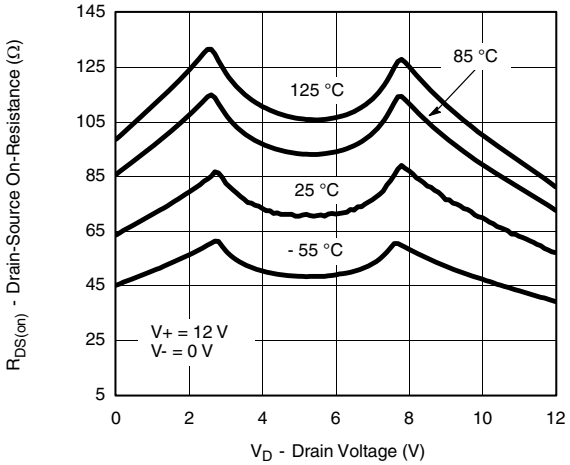

On-Resistance vs. $V_D$ and Dual Supply Voltage



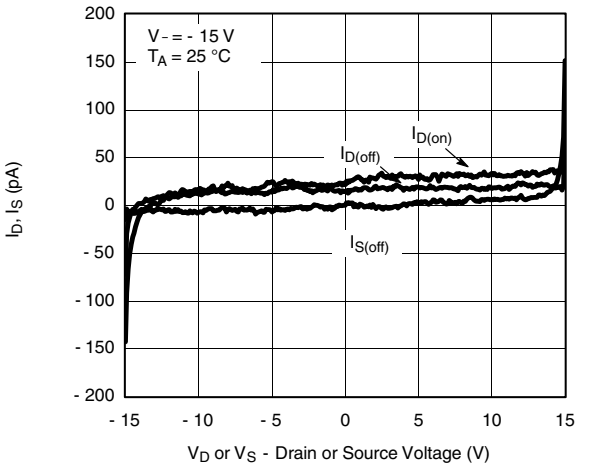

On-Resistance vs. $V_D$ and Unipolar Supply Voltage



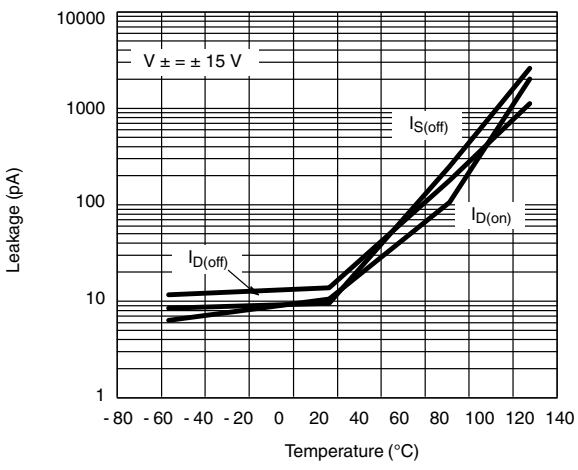

On-Resistance vs. $V_D$ and Temperature




On-Resistance vs. $V_D$ and Temperature

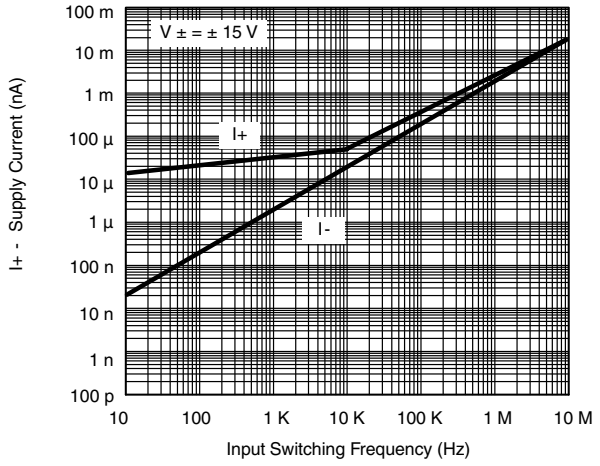



Leakage vs. Analog Voltage

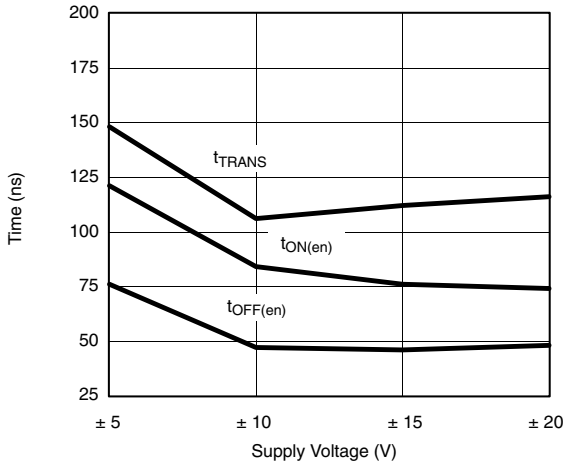



Leakage vs. Current

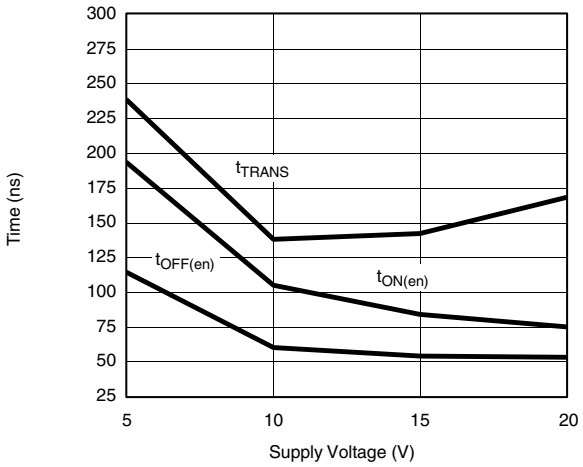
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



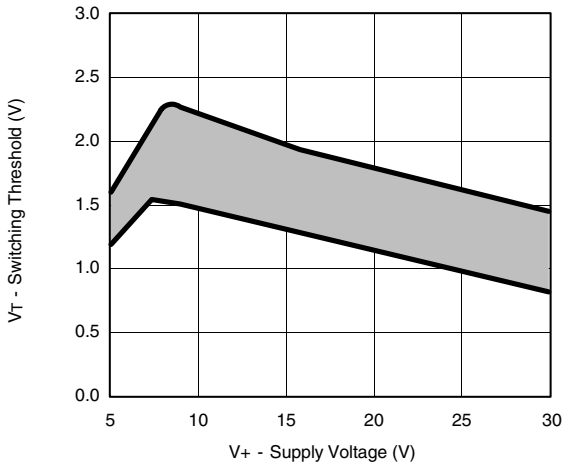

Supply Current vs. Input Switching Frequency



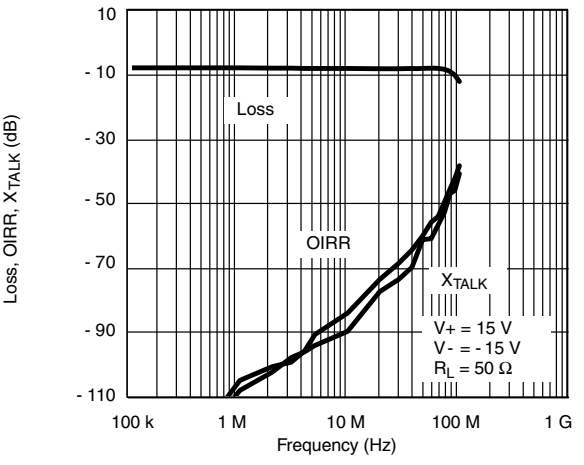

Switching Time vs. Bipolar Supplies



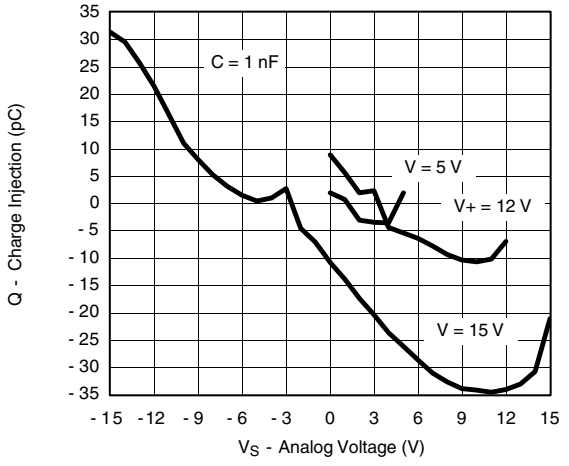

Switching Time vs. Single Supplies




Switching Threshold vs. Supply Voltage

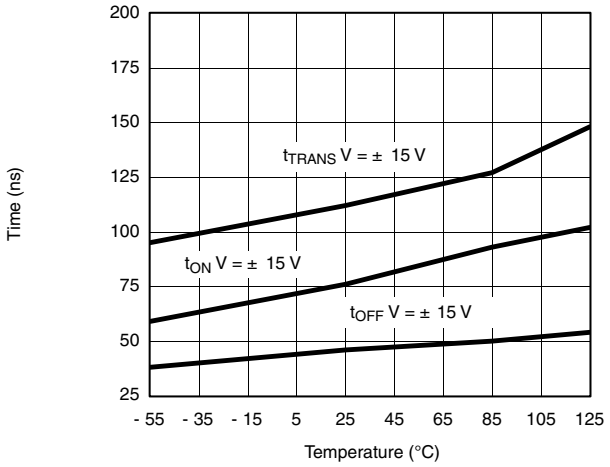



Insertion Loss, Off -Isolation Crosstalk vs. Frequency




Charge Injection vs. Analog Voltage

## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)




Switching Time vs. Temperature

## SCHEMATIC DIAGRAM (Typical Channel)

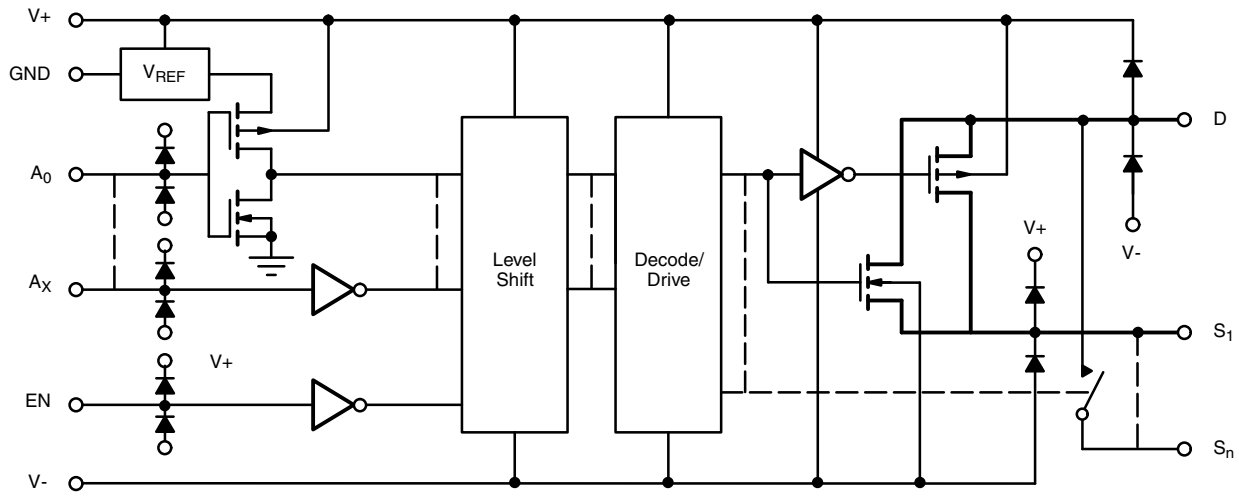



Fig. 1

## TEST CIRCUITS

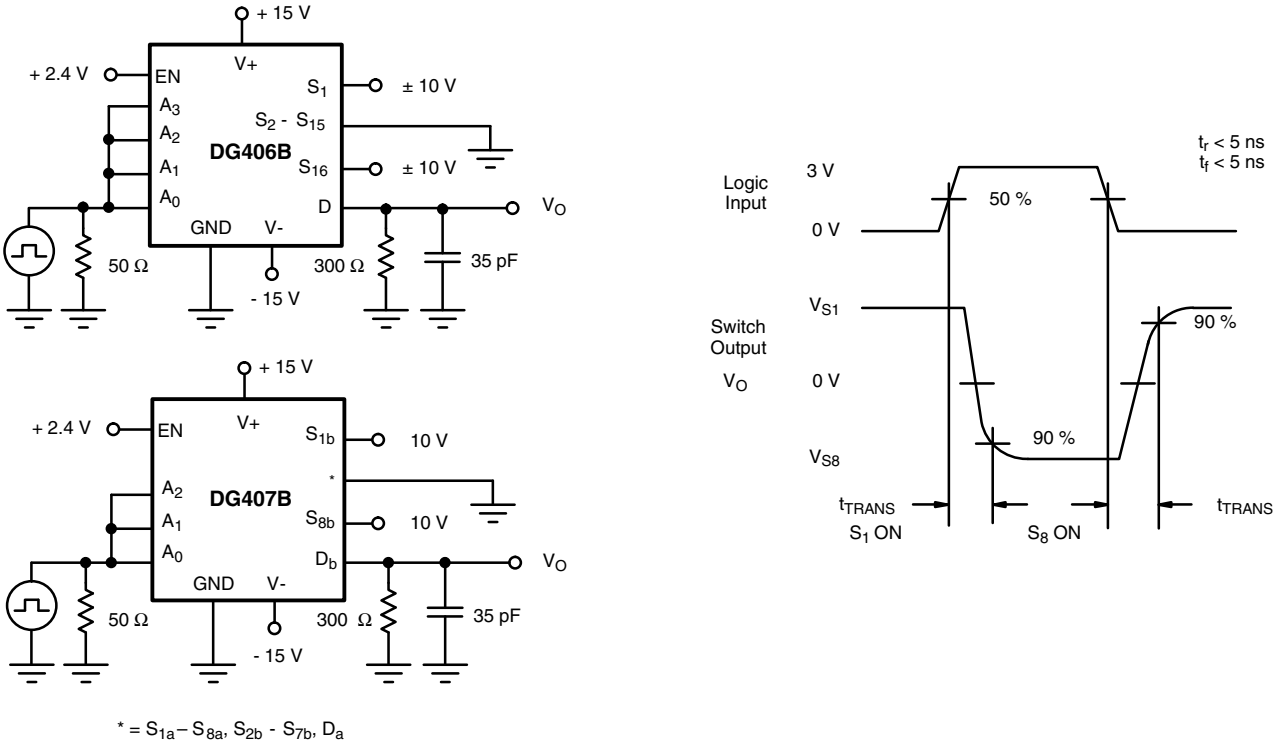



Fig. 2 - Transition Time

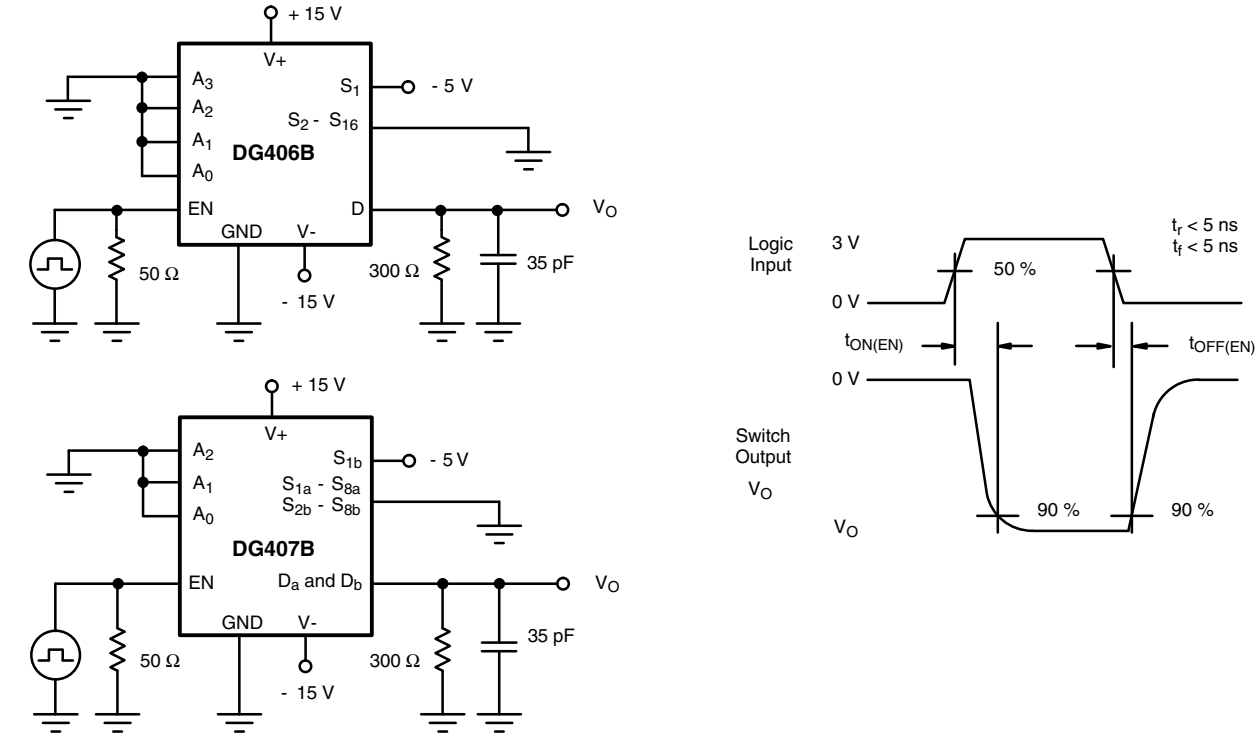



Fig. 3 - Enable Switching Time

## TEST CIRCUITS

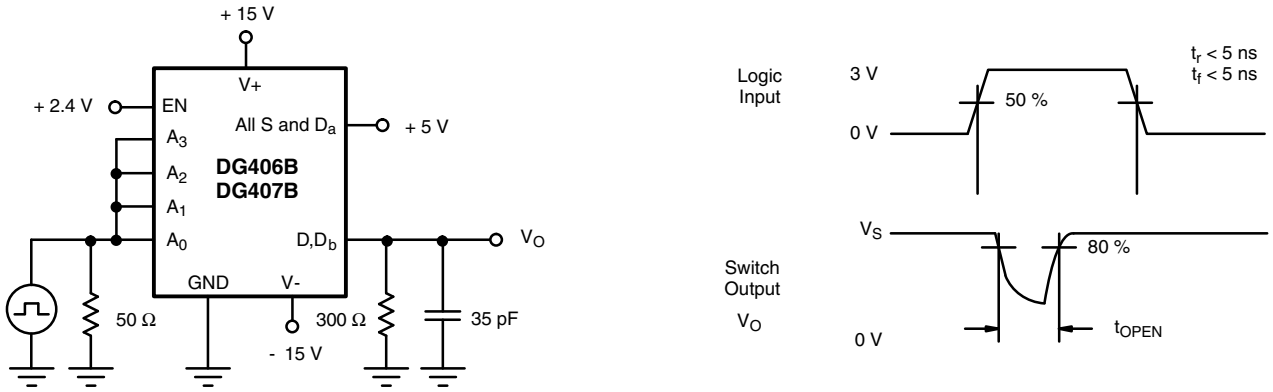
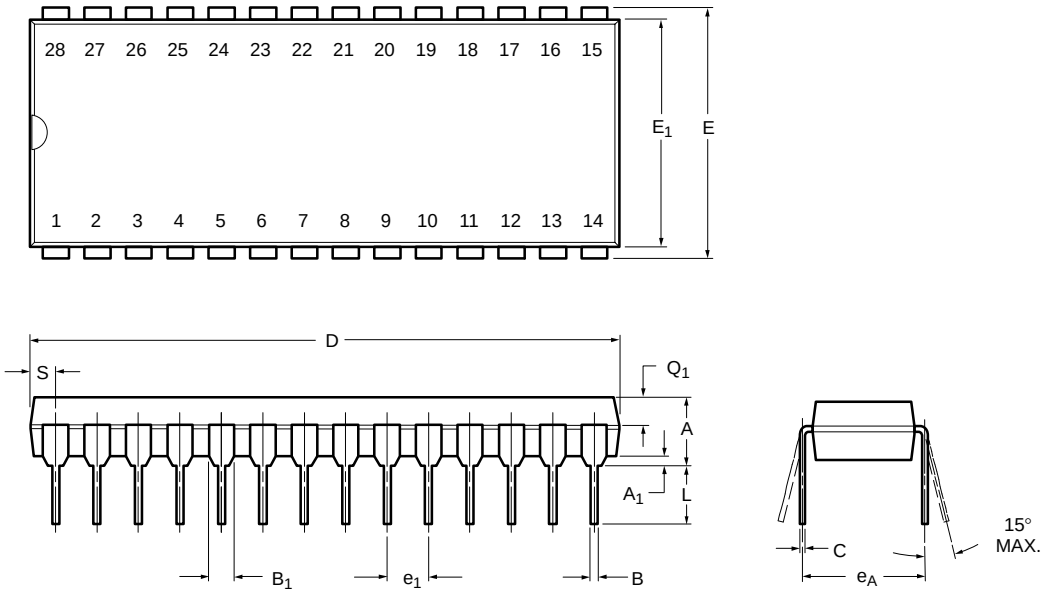



Fig. 4 - Break-Before-Make Interval

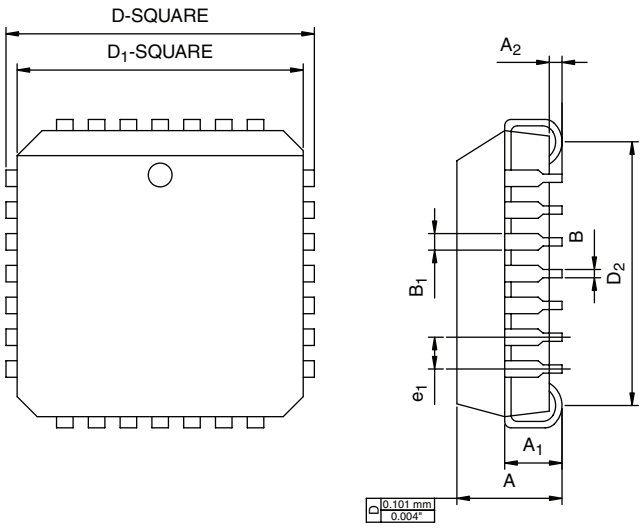
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72552.*

## PDIP: 28-LEAD




| Dim | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| **A** | 2.29 | 5.08 | 0.090 | 0.200 |
| **$A_1$** | 0.39 | 1.77 | 0.015 | 0.070 |
| **B** | 0.38 | 0.56 | 0.015 | 0.022 |
| **$B_1$** | 0.89 | 1.65 | 0.035 | 0.065 |
| **C** | 0.204 | 0.30 | 0.008 | 0.012 |
| **D** | 35.10 | 39.70 | 1.380 | 1.565 |
| **E** | 15.24 | 15.88 | 0.600 | 0.625 |
| **$E_1$** | 13.21 | 14.73 | 0.520 | 0.580 |
| **$e_1$** | 2.29 | 2.79 | 0.090 | 0.110 |
| **$e_A$** | 14.99 | 15.49 | 0.590 | 0.610 |
| **L** | 2.60 | 5.08 | 0.100 | 0.200 |
| **$Q_1$** | 0.95 | 2.345 | 0.0375 | 0.0925 |
| **S** | 0.995 | 2.665 | 0.0375 | 0.105 |
| ECN: S-03946—Rev. F, 09-Jul-01<br>DWG: 5488 | | | | |

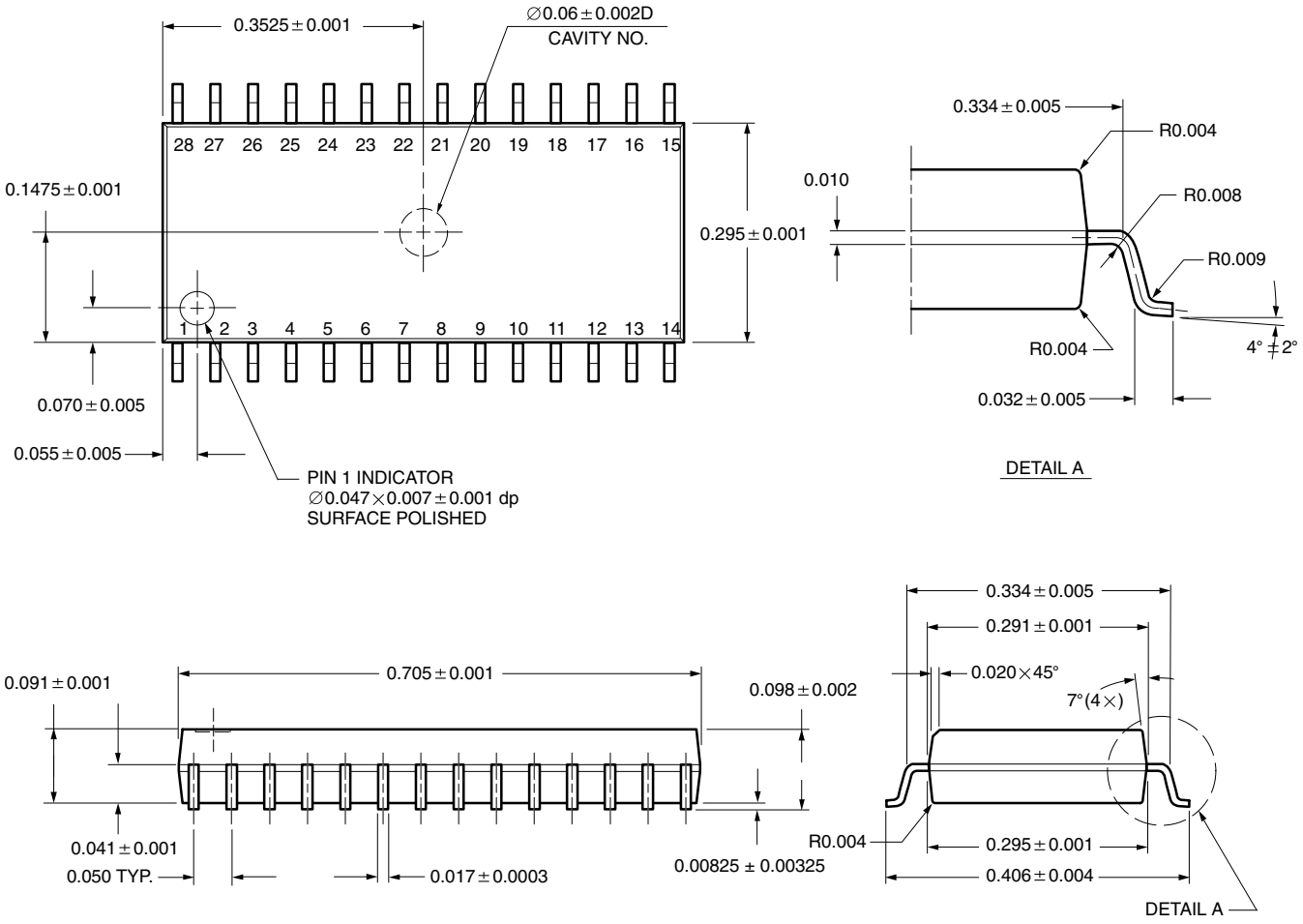
## PLCC: 28-LEAD




| DIM. | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.20 | 4.57 | 0.165 | 0.180 |
| $A_1$ | 2.29 | 3.04 | 0.090 | 0.120 |
| $A_2$ | 0.51 | - | 0.020 | - |
| B | 0.331 | 0.553 | 0.013 | 0.021 |
| $B_1$ | 0.661 | 0.812 | 0.026 | 0.032 |
| D | 12.32 | 12.57 | 0.485 | 0.495 |
| $D_1$ | 11.430 | 11.582 | 0.450 | 0.456 |
| $D_2$ | 9.91 | 10.92 | 0.390 | 0.430 |
| $e_1$ | 1.27 BSC | | 0.050 BSC | |

ECN: T09-0766-Rev. D, 28-Sep-09
DWG: 5491

## SOIC (WIDE-BODY): 28-LEADS




All Dimensions In Inches

ECN: E11-2209-Rev. D, 01-Aug-11
DWG: 5850

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