# 2.5 Ω, High Bandwidth, Dual SPDT Analog Switch

## DESCRIPTION

The DG2517E is low-voltage dual single-pole / double-throw monolithic CMOS analog switches. Designed to operate from 1.8 V to 5.5 V power supply, the DG2517E achieves a bandwidth of 221 MHz while providing low on-resistance (2.5 Ω), excellent on-resistance matching (0.3 Ω) and flatness (1 Ω) over the entire signal range.

The DG2517E offers the advantage of high linearity that reduces signal distortion, making ideal for audio, video, and USB signal routing applications.

Built on Vishay Siliconix's proprietary sub-micron high-density process, the DG2517E brings low power consumption at the same time as reduces PCB spacing with the MSOP10 and DFN10 packages.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. The DFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-GE4" suffix. The MSOP package uses 100 % matte Tin device termination and is represented by the lead (Pb)- free "-GE3" suffix. Both the matte Tin and nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL ratings.

## FEATURES

- 1.8 V to 5.5 V single supply operation
- Low $R_{ON}$: 2.5 Ω at 4.5 V
- 221 MHz, -3 dB bandwidth
- Low off-isolation, -58 dB at 1 MHz
- +1.6 V logic compatible
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

## BENEFITS

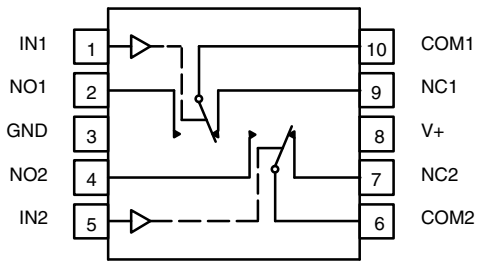
- High linearity
- Low power consumption
- High bandwidth
- Full rail signal swing range

## APPLICATIONS

- USB / UART signal switching
- Audio / video switching
- Cellular phone
- Media players
- Modems
- Hard drives
- PCMCIA

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2517E




Top View

**TRUTH TABLE**

| LOGIC | NC1 AND NC2 | NO1 AND NO2 |
|---|---|---|
| 0 | ON | OFF |
| 1 | OFF | ON |

**ORDERING INFORMATION**

| TEMP. RANGE | PACKAGE | PART NUMBER |
|---|---|---|
| -40 °C to 85 °C | MSOP-10 | DG2517EDQ-T1-GE3 |
| | DFN-10 | DG2517EDN-T1-GE4 |

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER | | LIMIT | UNIT |
|---|---|---|---|
| **Reference to GND** | | | |
| V+ | | -0.3 to +6 | V |
| IN, COM, NC, NO [a] | | -0.3 to (V+ + 0.3) | |
| Continuous current (any terminal) | | ± 50 | mA |
| Peak current (pulsed at 1 ms, 10 % duty cycle) | | ± 200 | |
| Storage temperature (D suffix) | | -65 to +150 | °C |
| Power dissipation (packages) [b] | MSOP-10 [c] | 320 | mW |
| | DFN-10 [d] | 1191 | |
| ESD / HBM | EIA / JESD22-A114-A | 7.5k | V |
| ESD / CDM | EIA / JESD22-C101-A | 1.5k | |
| Latch up | JESD78 | 300 | mA |

**Notes**

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 4 mW/°C above 70 °C
d. Derate 14.9 mW/°C above 70 °C

## SPECIFICATIONS (V+ = 3 V)

| PARAMETER | SYMBOL | TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 3 V, ± 10 %, $V_{INL}$ = 0.4 V, $V_{INH}$ = 1.5 V [e] | TEMP. [a] | LIMITS -40 °C to +85 °C MIN. [c] | TYP. [b] | MAX. [c] | UNIT |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog signal range [d] | $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| Drain-source on-resistance | $R_{DS(on)}$ | V+ = 1.8 V, $V_{NC/NO}$ = 0.4 V / V+, $I_{NC/NO}$ = 8 mA | Room | - | 7 | 11 | Ω |
| | | | Full | - | - | 13 | |
| | | V+ = 2.7 V, $V_{COM}$ = 0.8 V / 1.8 V, $I_{COM}$ = 10 mA | Room | - | 4.6 | 5.5 | |
| | | | Full | - | - | 6.5 | |
| On-resistance matching | $\Delta R_{DS(on)}$ | V+ = 2.7 V, $V_{COM}$ = 0.8 V / 1.4 V / 1.8 V, $I_{COM}$ = 10 mA | Room | - | 0.02 | 0.3 | |
| | | | Full | - | - | 0.6 | |
| On-resistance flatness [d, f] | $R_{flat(on)}$ | | Room | - | 0.62 | 1 | |
| | | | Full | - | - | 1.5 | |
| Off leakage current [g] | $I_{NC/NO(off)}$ | V+ = 3.6 V, $V_{NC/NO}$ = 1 V / 3.2 V, $V_{COM}$ = 3.2 V / 1 V | Room | -1 | 0.01 | 1 | nA |
| | | | Full | -5 | - | 5 | |
| Channel-on leakage current [g] | $I_{COM(on)}$ | V+ = 3.6 V, $V_{COM}$ = $V_{NC/NO}$ = 1 V / 3.2 V | Room | -1 | 0.01 | 1 | |
| | | | Full | -5 | - | 5 | |
| **Digital Control** | | | | | | | |
| Input current [d] | $I_{INL}$ or $I_{INH}$ | | Full | -1 | - | 1 | µA |
| Input high voltage [d] | $V_{INH}$ | | Full | 1.5 | - | - | V |
| Input low voltage [d] | $V_{INL}$ | | Full | - | - | 0.4 | |
| Digital input capacitance [d] | $C_{IN}$ | | Room | - | 3 | - | pF |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{NC/NO}$ = 3 V, $C_L$ = 35 pf, $R_L$ = 300 Ω | Room | - | 19 | 45 | ns |
| | | | Full | - | - | 50 | |
| Turn-off time | $t_{OFF}$ | | Room | - | 9 | 35 | |
| | | | Full | - | - | 45 | |
| Break-before-make time [d] | $t_{BBM}$ | | Room | 4 | 11 | - | |
| | | | Full | 3 | - | - | |
| Charge injection [d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{gen}$= 1.5 V, $R_{gen}$= 0 Ω | Room | - | -9 | - | pC |
| Bandwidth [d] | BW | $C_L$ = 5 pF (set up capacitance) | Room | - | 226 | - | MHz |
| Off-isolation [d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -55 | - | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz | Room | - | -42 | - | |
| Channel-to-channel crosstalk [d] | $X_{TALK}$ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -61 | - | |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz | Room | - | -44 | - | |
| NO, NC off capacitance [d] | $C_{NO(off)}$ | V+ = 2.7 V, f = 1 MHz | Room | - | 7 | - | pF |
| | $C_{NC(off)}$ | | Room | - | 7 | - | |
| Channel-on capacitance [d] | $C_{NO(on)}$ | | Room | - | 23 | - | |
| | $C_{NC(on)}$ | | Room | - | 23 | - | |
| **Power Supply** | | | | | | | |
| Power supply range | V+ | | | 2.7 | - | 3.3 | V |
| Power supply current [d] | I+ | V+ = 2.7 V, $V_{IN}$ = 0 V or 2.7 V | Full | - | - | 1 | µA |

**Notes**

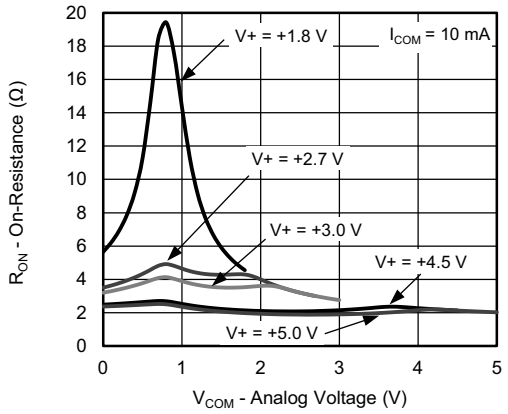
a. Room = 25 °C, Full = as determined by the operating suffix
b. Typical values are for design aid only, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guarantee by design, not subjected to production test
e. $V_{IN}$ = V+ voltage to perform proper function
f. Crosstalk measured between channels
g. Guarantee by 5 V testing

| **SPECIFICATIONS** (V+ = 5 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 5 V, ± 10 %, $V_{INL}$ = 0.5 V, $V_{INH}$ = 2 V [e]** | **TEMP. [a]** | **LIMITS -40 °C to +85 °C** | | | **UNIT** |
| | | | | **MIN. [c]** | **TYP. [b]** | **MAX. [c]** | |
| **Analog Switch** | | | | | | | |
| Analog signal ranged | $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| Drain-source on-resistance | $R_{DS(on)}$ | V+ = 4.5 V, $V_{COM}$ = 0.8 V / 3.5 V; $I_{COM}$ = 10 mA | Room | - | 2.5 | 3.1 | Ω |
| | | | Full | - | - | 4 | |
| On-resistance matching | $\Delta R_{DS(on)}$ | V+ = 4.5 V, $V_{COM}$ = 0.8 V / 2.5 V / 3.5 V, $I_{COM}$ = 10 mA | Room | - | 0.01 | 0.4 | |
| | | | Full | - | - | 0.6 | |
| On-resistance flatness [d, f] | $R_{flat(on)}$ | | Room | - | 0.61 | 1 | |
| | | | Full | - | - | 1.5 | |
| Off leakage current [g] | $I_{NC/NO(off)}$ | V+ = 5.5 V, $V_{NC/NO}$ = 1 V / 4.5 V, $V_{COM}$ = 4.5 V / 1 V | Room | -2 | 0.15 | 2 | nA |
| | | | Full | -10 | - | 10 | |
| Channel-on leakage current [g] | $I_{COM(on)}$ | V+ = 5.5 V, $V_{COM}$ = $V_{NC/NO}$ = 1 V / 4.5 V | Room | -2 | 0.20 | 2 | |
| | | | Full | -10 | - | 10 | |
| Power down leakage [d] | $I_{PD}$ | V+ = 0 V, $V_{COM}$ = 5.5 V, NC/NO open | Full | - | 0.01 | 5 | µA |
| | | V+ = 0 V, $V_{NC/NO}$ = 5.5 V, COM, open | Full | - | 0.01 | 3 | mA |
| **Digital Control** | | | | | | | |
| Input current [d] | $I_{INL}$ or $I_{INH}$ | | Full | -1 | - | 1 | µA |
| Input high voltage [d] | $V_{INH}$ | | Full | 2 | - | - | V |
| Input low voltage [d] | $V_{INL}$ | | Full | - | - | 0.5 | |
| Digital input capacitance [d] | $C_{IN}$ | | Room | - | 3 | - | pF |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{NC/NO}$ = 3 V, $C_L$ = 35 pf, $R_L$ = 300 Ω | Room | - | 13 | 40 | ns |
| | | | Full | - | - | 43 | |
| Turn-off time | $t_{OFF}$ | | Room | - | 7 | 33 | |
| | | | Full | - | - | 35 | |
| Break-before-make time [d] | $t_{BBM}$ | | Room | 3 | 6 | - | |
| | | | Full | 2 | - | - | |
| Propagation delay [d] | tpd | V+ = 5 V, no $R_L$ | Room | - | 380 | - | ps |
| Charge injection [d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{gen}$ = 2.5 V, $R_{gen}$ = 0 Ω | Room | - | -19.4 | - | pC |
| Bandwidth [d] | BW | $C_L$ = 5 pF (set up capacitance) | Room | - | 221 | - | MHz |
| Off-isolation [d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -58 | - | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz | Room | - | -43 | - | |
| Channel-to-channel crosstalk [d] | $X_{TALK}$ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -62 | - | |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz | Room | - | -47 | - | |
| NO, NC off capacitance [d] | $C_{NO(off)}$ | V+ = 5 V, f = 1 MHz | Room | - | 7 | - | pF |
| | $C_{NC(off)}$ | | Room | - | 7 | - | |
| Channel-on capacitance [d] | $C_{NO(on)}$ | | Room | - | 23 | - | |
| | $C_{NC(on)}$ | | Room | - | 23 | - | |
| **Power Supply** | | | | | | | |
| Power supply range | V+ | | | 4.5 | - | 5.5 | V |
| Power supply current [d] | I+ | V+ = 5.5 V, $V_{IN}$ = 0 or 5.5 V | Full | - | - | 1 | µA |

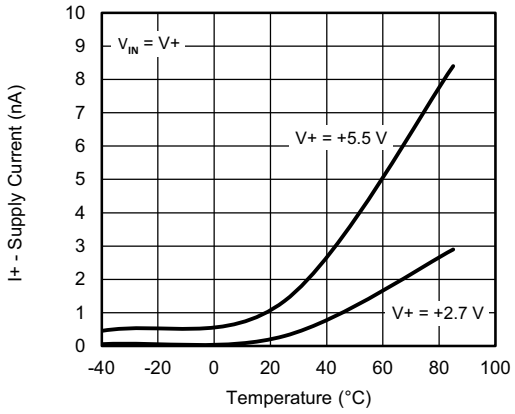
**Notes**
a. Room = 25 °C, Full = as determined by the operating suffix
b. Typical values are for design aid only, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guarantee by design, not subjected to production test
e. $V_{IN}$ = input voltage to perform proper function
f. Difference of min and max values
g. Guaranteed by 5 V testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

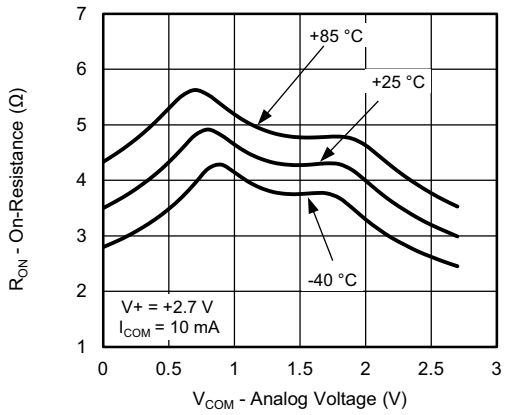
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



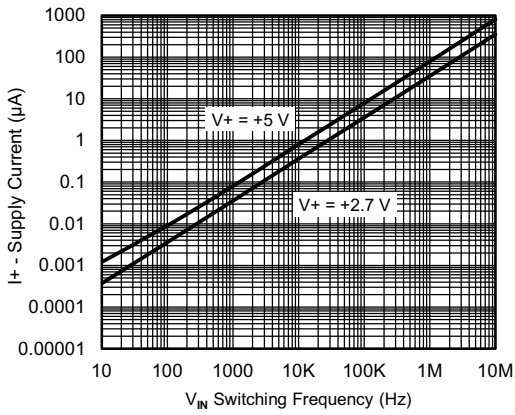

**$R_{ON}$ vs. $V_{COM}$ and Single Supply Voltage**



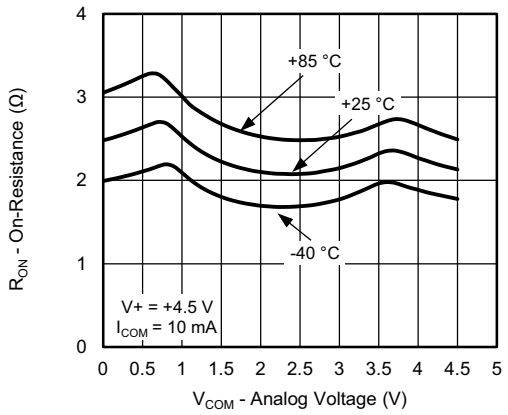

**Supply Current vs. Temperature**



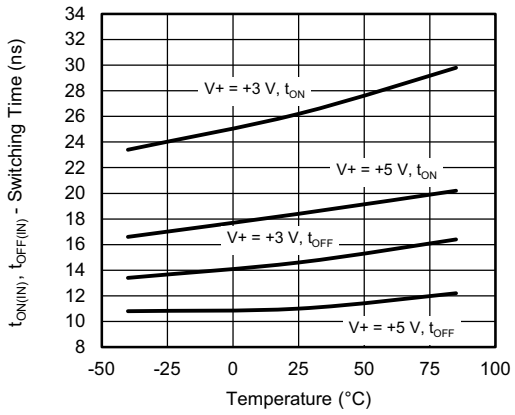

**$R_{ON}$ vs. Analog Voltage and Temperature**




**Positive Supply Current vs. Switching Frequency**

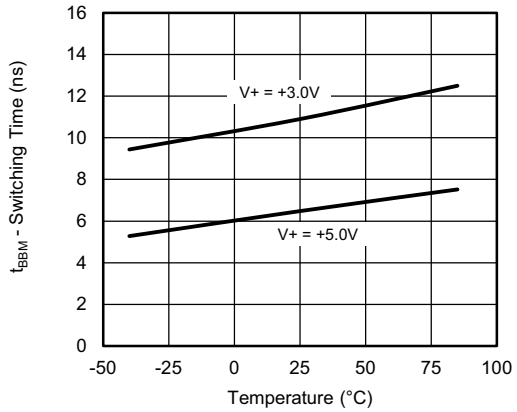



**$R_{ON}$ vs. Analog Voltage and Temperature**

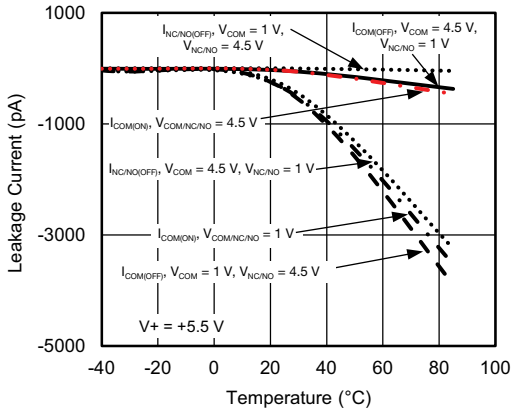



**Switching Time vs. Temperature**

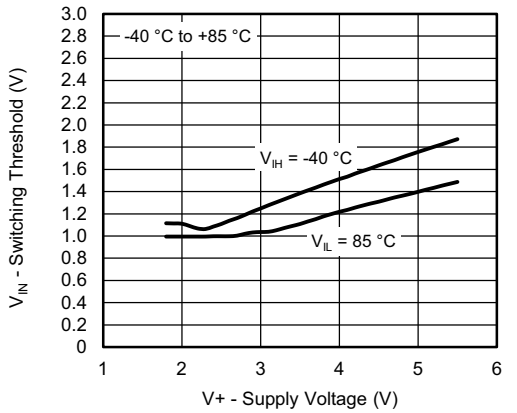
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



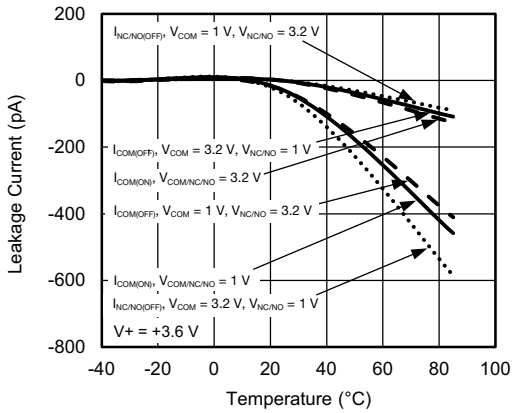

**Switching Time vs. Temperature**



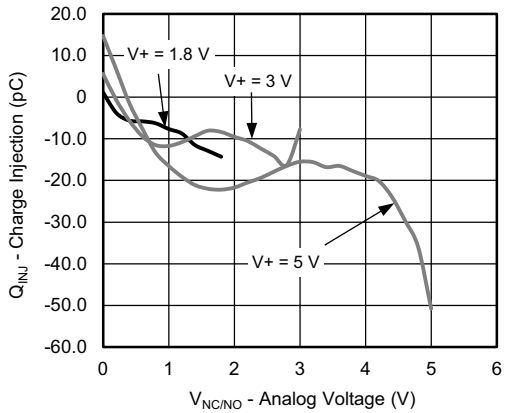

**Leakage Current vs. Temperature**



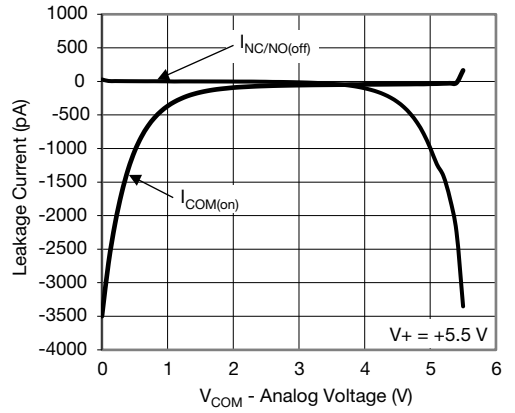

**Switching Threshold vs. Supply Voltage**




**Leakage Current vs. Temperature**

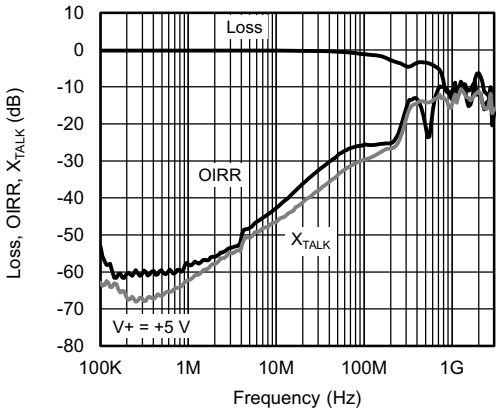



**Charge Injection vs. Source Voltage**



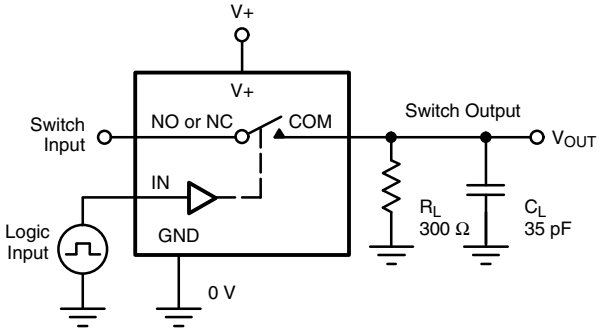

**Leakage Current vs. Analog Voltage**

## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



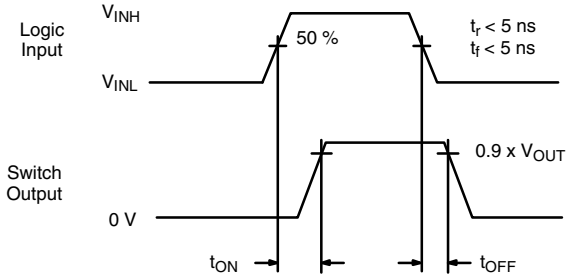

**Loss, OIRR, $X_{TALK}$ vs. Frequency**

## TEST CIRCUITS



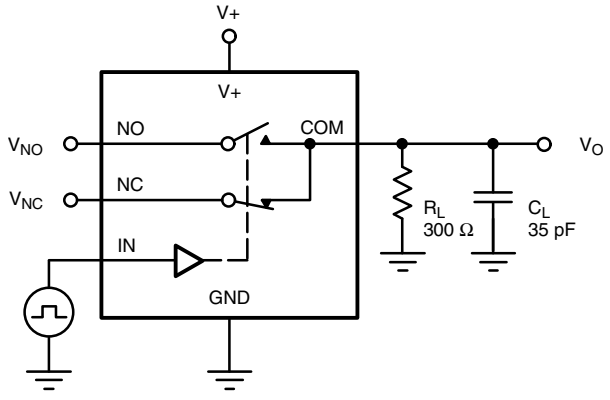

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Fig. 1 - Switching Time**




$C_L$ (includes fixture and stray capacitance)

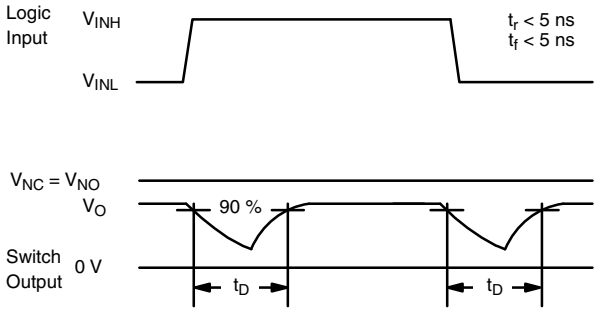



**Fig. 2 - Break-Before-Make Interval**

## TEST CIRCUITS

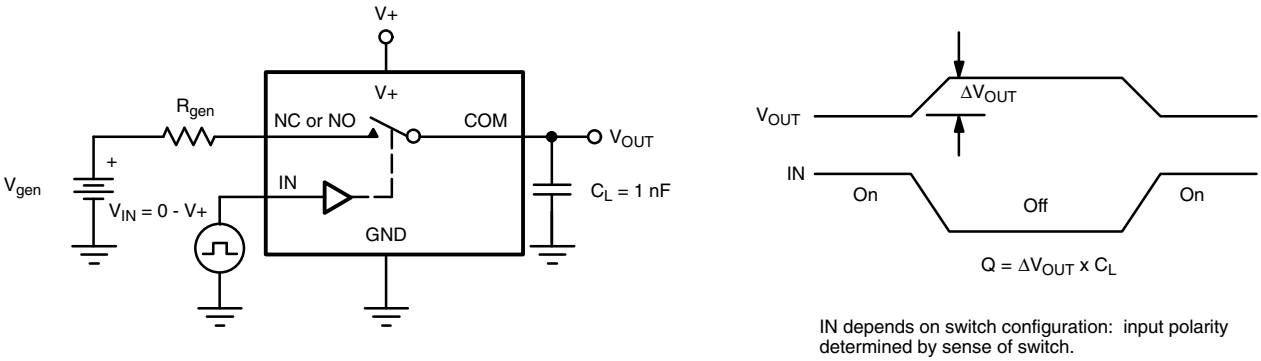



**Fig. 3 - Charge Injection**

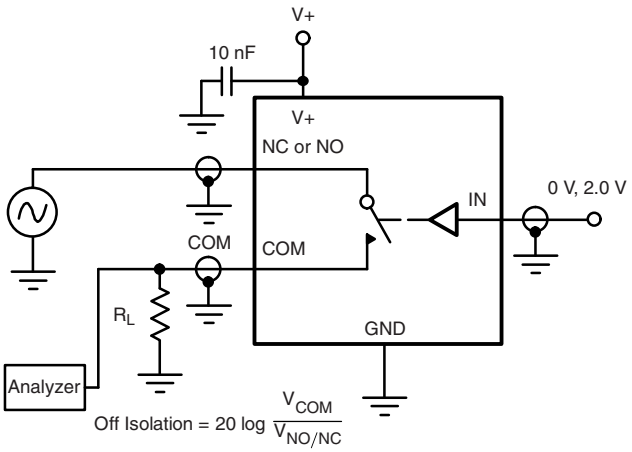



**Fig. 4 - Off-Isolation**

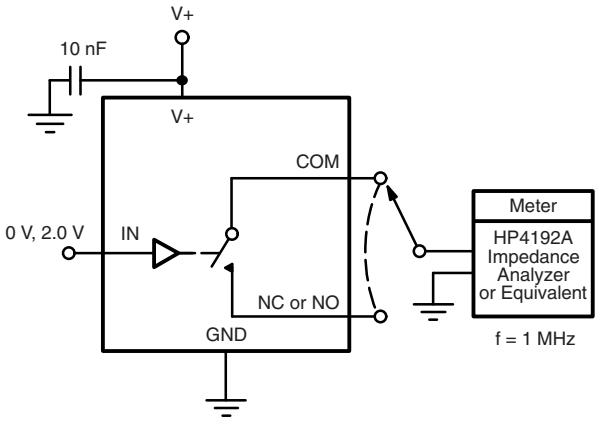



**Fig. 5 - Channel Off/On Capacitance**

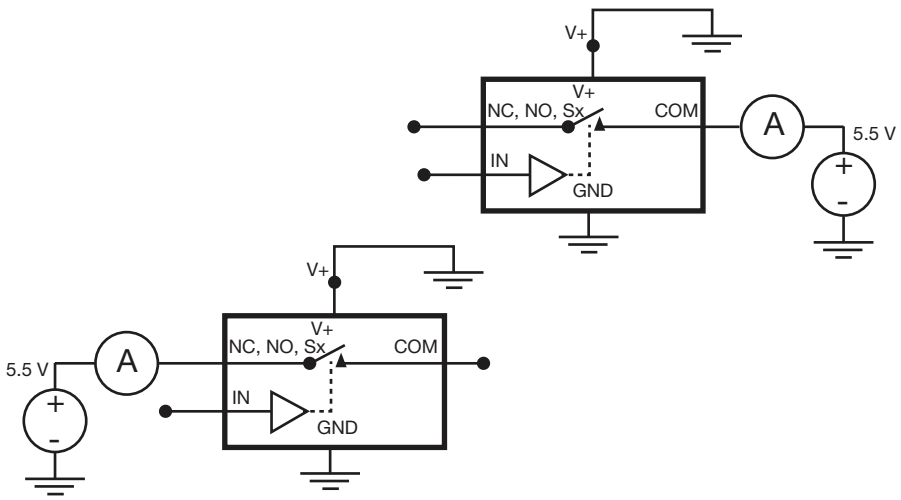
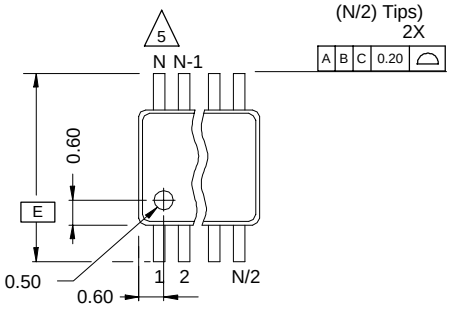



**Fig. 6 - Source / Drain Power Down Leakage**

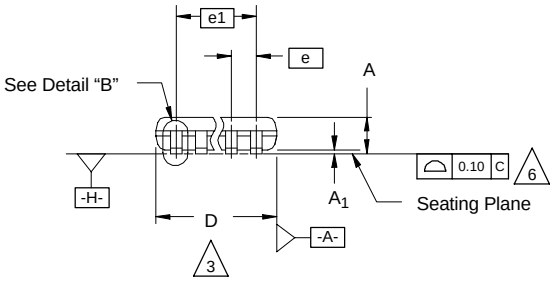
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74518.*

## MSOP: 10-LEADS

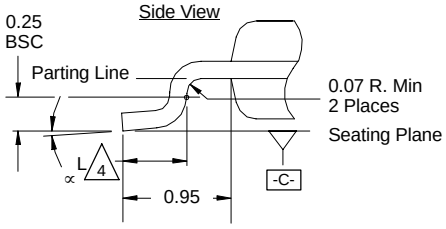
**JEDEC Part Number: MO-187, (Variation AA and BA)**



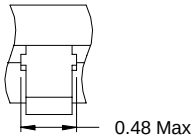

Top View



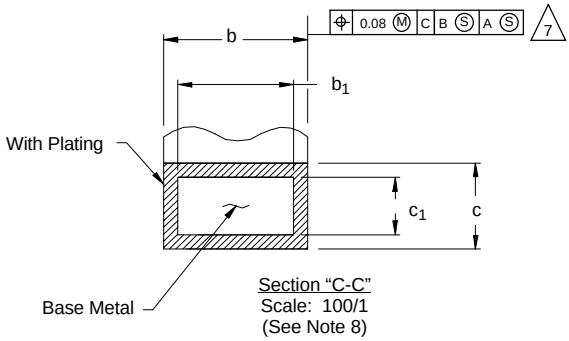

Side View



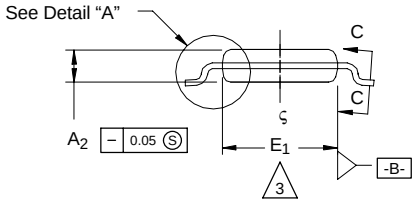

Detail "A"
(Scale: 30/1)




Detail "B"
(Scale: 30/1)
Dambar Protrusion




Section "C-C"
Scale: 100/1
(See Note 8)




End View

NOTES:

1. Die thickness allowable is $0.203 \pm 0.0127$.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "$E_1$" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

**N = 10L**

| Dim | MILLIMETERS | | | Note |
|---|---|---|---|---|
| | Min | Nom | Max | |
| A | - | - | 1.10 | |
| $A_1$ | 0.05 | 0.10 | 0.15 | |
| $A_2$ | 0.75 | 0.85 | 0.95 | |
| b | 0.17 | - | 0.27 | 8 |
| $b_1$ | 0.17 | 0.20 | 0.23 | 8 |
| c | 0.13 | - | 0.23 | |
| $c_1$ | 0.13 | 0.15 | 0.18 | |
| D | 3.00 BSC | | | 3 |
| E | 4.90 BSC | | | |
| $E_1$ | 2.90 | 3.00 | 3.10 | 3 |
| e | 0.50 BSC | | | |
| $e_1$ | 2.00 BSC | | | |
| L | 0.40 | 0.55 | 0.70 | 4 |
| N | 10 | | | 5 |
| ∝ | 0° | 4° | 6° | |

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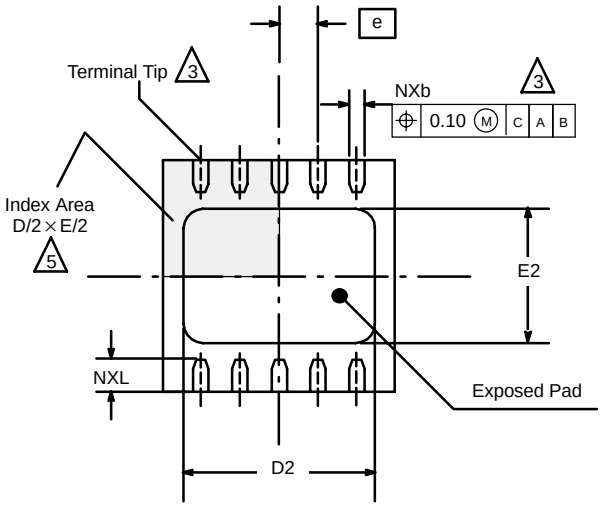
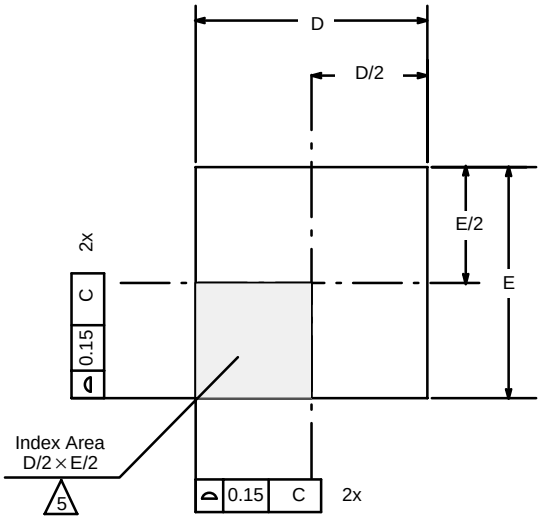
DWG: 5867

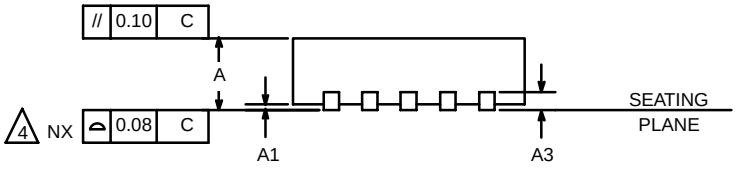
## DFN-10 LEAD (3 X 3)




BOTTOM VIEW




TOP VIEW




SIDE VIEW

NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

| Dim | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | | 0.20 BSC | | | 0.008 BSC | |
| b | 0.18 | 0.23 | 0.30 | 0.007 | 0.009 | 0.012 |
| D | | 3.00 BSC | | | 0.118 BSC | |
| D2 | 2.20 | 2.38 | 2.48 | 0.087 | 0.094 | 0.098 |
| E | | 3.00 BSC | | | 0.118 BSC | |
| E2 | 1.49 | 1.64 | 1.74 | 0.059 | 0.065 | 0.069 |
| e | | 0.50 BSC | | | 0.020 BSC | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

*Use millimeters as the primary measurement.

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