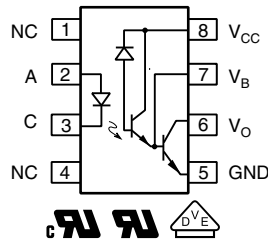
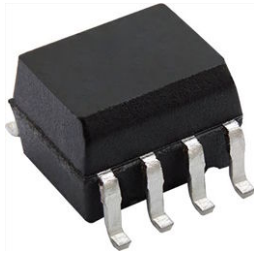


High Speed Optocoupler, 100 k Bd, Low Input Current, High Gain



FEATURES

- High current transfer ratio, 300 %
- Low input current, 0.5 mA
- High output current, 60 mA
- TTL compatible output, $V_{OL} = 0.1\text{ V}$
- Adjustable bandwidth access to base
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

LINKS TO ADDITIONAL RESOURCES



DESCRIPTION

The SFH6318 is ideal for TTL applications since the 300 % minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 k Ω pull-up resistor.

The SFH6319 is best suited for low power logic applications involving CMOS and low power TTL. A 400 % current transfer ratio with only 0.5 mA of LED current is guaranteed from 0 °C to 70 °C.

Very high current ratio together with 4000 V_{RMS} isolation are achieved by coupling an LED with an integrated high gain photo detector in a SOIC-8 package. Separate pins for the photo diode and output stage enable TTL compatible saturation voltages with high speed operation. Photodarlington operation is achieved by tying the V_{CC} and V_O terminals together. Access to the base terminal allows adjustment to the gain bandwidth.

APPLICATIONS

- Logic ground isolation - TTL / TTL, TTL / CMOS, CMOS / CMOS, CMOS / TTL
- EIA RS 232C line receiver
- Low input current line receiver long lines, party lines
- Telephone ring detector
- Line voltage status indication - low input power dissipation
- Low power systems - ground isolation

AGENCY APPROVALS

- [UL1577](#)
- [cUL](#)
- [DIN EN 60747-5-5 \(VDE 0884-5\) available with option 1](#)
- [CSA](#)

ORDERING INFORMATION			
<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 2px 5px;">S</div> <div style="border: 1px solid black; padding: 2px 5px;">F</div> <div style="border: 1px solid black; padding: 2px 5px;">H</div> <div style="border: 1px solid black; padding: 2px 5px;">6</div> <div style="border: 1px solid black; padding: 2px 5px;">3</div> <div style="border: 1px solid black; padding: 2px 5px;">1</div> <div style="border: 1px solid black; padding: 2px 5px;">#</div> <div style="border: 1px solid black; padding: 2px 5px;">-</div> <div style="border: 1px solid black; padding: 2px 5px;">X</div> <div style="border: 1px solid black; padding: 2px 5px;">0</div> <div style="border: 1px solid black; padding: 2px 5px;">#</div> <div style="border: 1px solid black; padding: 2px 5px;">#</div> <div style="border: 1px solid black; padding: 2px 5px;">T</div> </div>	PART NUMBER	PACKAGE OPTION	TAPE AND REEL
AGENCY CERTIFIED / PACKAGE	CTR (%)		
UL, cUL, CSA	≥ 300	≥ 500	
SOIC-8	SFH6318T	SFH6319T	

Note

- Additional options may be possible, please contact sales office



ABSOLUTE MAXIMUM RATINGS (T _{amb} = 25 °C, unless otherwise specified)					
PARAMETER	TEST CONDITION	PART	SYMBOL	VALUE	UNIT
INPUT					
Reverse voltage			V _R	3	V
Supply and output voltage	V _{CC} (pin 8 to 5), V _O (pin 6 to 5)	SFH6318	V _{CC} , V _O	-0.5 to 7	V
		SFH6319	V _{CC} , V _O	-0.5 to 18	V
Input power dissipation			P _{diss}	35	mW
Average input current			I _{F(AVG)}	20	mA
Peak input current	50 % duty cycle; 1 ms pulse width		I _{FRM}	40	mA
Peak transient input current	t _p ≤ 1 μs, 300 pps		I _{FSM}	1	A
OUTPUT					
Output current (pin 6)			I _O	60	mA
Emitter-base reverse current (pin 5 to 7)			V _{EB0}	0.5	V
Output power dissipation			P _{diss}	150	mW
Derate linearly from 25 °C				2	mW/°C
COUPLER					
Storage temperature			T _{stg}	-55 to +125	°C
Lead soldering temperature	t = 10 s		T _{slid}	260	°C
Junction temperature			T _j	125	°C
Ambient temperature range			T _{amb}	-55 to +100	°C
Total power dissipation			P _{diss}	185	mW

Note

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability

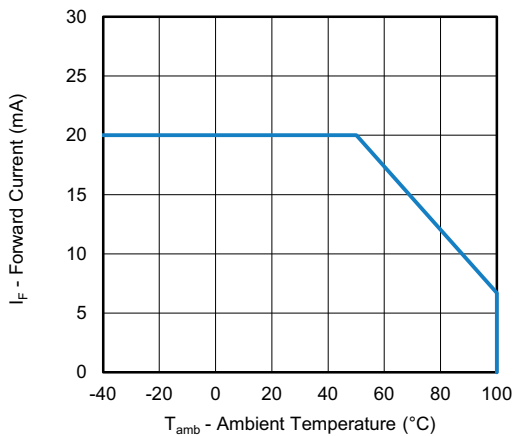


Fig. 1 - Forward Current vs. Ambient Temperature

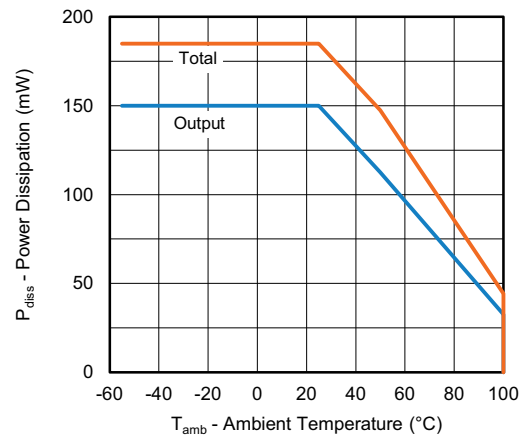


Fig. 2 - Power Dissipation vs. Ambient Temperature



ELECTRICAL CHARACTERISTICS ($T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; typical values are at $T_{amb} = 25\text{ }^{\circ}\text{C}$)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Forward voltage	$I_F = 1.6\text{ mA}$	V_F	-	1.28	1.7	V
Temperature coefficient of forward voltage	$I_F = 1.6\text{ mA}$	$\Delta V_F / \Delta T_{amb}$	-	-2.3	-	mV/ $^{\circ}\text{C}$
Input capacitance	$f = 1\text{ MHz}, V_F = 0$	C_{IN}	-	55	-	pF
OUTPUT						
Logic low output voltage ⁽¹⁾	$I_F = 1.6\text{ mA}, I_O = 4.8\text{ mA}, V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.1	0.4	V
	$I_F = 1.6\text{ mA}, I_O = 8\text{ mA}, V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.1	0.4	V
	$I_F = 5\text{ mA}, I_O = 15\text{ mA}, V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.15	0.4	V
	$I_F = 12\text{ mA}, I_O = 24\text{ mA}, V_{CC} = 4.5\text{ V}$	V_{OL}	-	0.25	0.4	V
Logic high output current ⁽¹⁾	$I_F = 0\text{ mA}, V_O = V_{CC} = 7\text{ V}$	I_{IO}	-	0.1	250	μA
	$I_F = 0\text{ mA}, V_O = V_{CC} = 18\text{ V}$	I_{IO}	-	0.05	100	μA
Logic low supply current ⁽¹⁾	$I_F = 1.6\text{ mA}, V_O = \text{OPEN}, V_{CC} = 18\text{ V}$	I_{CCL}	-	0.3	1.5	mA
Logic high supply current ⁽¹⁾	$I_F = 0\text{ mA}, V_O = \text{OPEN}, V_{CC} = 18\text{ V}$	I_{CCH}	-	0.0003	10	μA
COUPLER						
Capacitance (input to output) ⁽²⁾	$f = 1\text{ MHz}$	C_{IO}	-	0.6	-	pF

Notes

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements

(1) Pin 7 open

(2) Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together

CURRENT TRANSFER RATIO ($T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$; typical values are at $T_{amb} = 25\text{ }^{\circ}\text{C}$)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Current transfer ratio ⁽¹⁾	$I_F = 1.6\text{ mA}, V_O = 0.4\text{ V}, V_{CC} = 4.5\text{ V}$	SFH6318	CTR	300	2000	2600	%
	$I_F = 0.5\text{ mA}, V_O = 0.4\text{ V}, V_{CC} = 4.5\text{ V}$	SFH6319	CTR	400	2200	3500	%
	$I_F = 1.6\text{ mA}, V_O = 0.4\text{ V}, V_{CC} = 4.5\text{ V}$	SFH6319	CTR	500	2000	2600	%

Notes

- DC current transfer ratio is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F times 100 %

(1) Pin 7 open

SWITCHING CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to low output level	$I_F = 1.6\text{ mA}, R_L = 2.2\text{ k}\Omega$	SFH6318	t_{PHL}	-	2	10	μs
Propagation delay time to low output level ⁽¹⁾⁽²⁾	$I_F = 0.5\text{ mA}, R_L = 4.7\text{ k}\Omega$	SFH6319	t_{PHL}	-	4	25	μs
Propagation delay time to high output level ⁽¹⁾⁽²⁾	$I_F = 12\text{ mA}, R_L = 270\ \Omega$	SFH6319	t_{PHL}	-	0.5	1	μs
Propagation delay time to high output level	$I_F = 1.6\text{ mA}, R_L = 2.2\text{ k}\Omega$	SFH6318	t_{PLH}	-	15	35	μs
Propagation delay time to high output level ⁽¹⁾⁽²⁾	$I_F = 0.5\text{ mA}, R_L = 4.7\text{ k}\Omega$	SFH6319	t_{PLH}	-	30	60	μs
Propagation delay time to high output level ⁽¹⁾⁽²⁾	$I_F = 12\text{ mA}, R_L = 270\ \Omega$	SFH6319	t_{PLH}	-	3	7	μs

Notes

(1) Pin 7 open

(2) Using a resistor between pin 5 and 7 will decrease gain and delay time

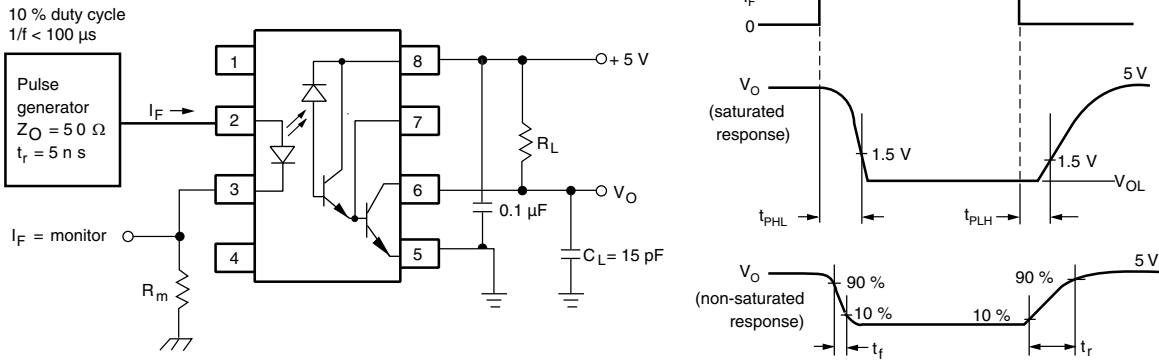


Fig. 3 - Switching Test Circuit

COMMON MODE TRANSIENT IMMUNITY ($T_{amb} = 25 \text{ }^\circ\text{C}$)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Common mode transient immunity at logic high level output ⁽¹⁾⁽²⁾	$I_F = 0 \text{ mA}$, $R_L = 2.2 \text{ k}\Omega$, $V_{CM} = 10 \text{ V}_{PP}$	$ CM_H $	-	1000	-	V/μs
Common mode transient immunity at logic low level output ⁽¹⁾⁽²⁾	$I_F = 1.6 \text{ mA}$, $R_L = 2.2 \text{ k}\Omega$, $V_{CM} = 10 \text{ V}_{PP}$	$ CM_L $	-	1000	-	V/μs

Notes

- (1) Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a logic high state (i.e. $V_O > 2 \text{ V}$) common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e. $V_O < 0.8 \text{ V}$)
- (2) In applications where dv/dt may exceed 50 000 V/μs (such as state discharge) a series resistor, R_{CC} should be included to protect I_C from destructively high surge currents. The recommended value is refer to Fig. 2.
 $R_{CC} \equiv [V/(0.15 \times I_F \text{ (mA)})] \text{ k}\Omega$.

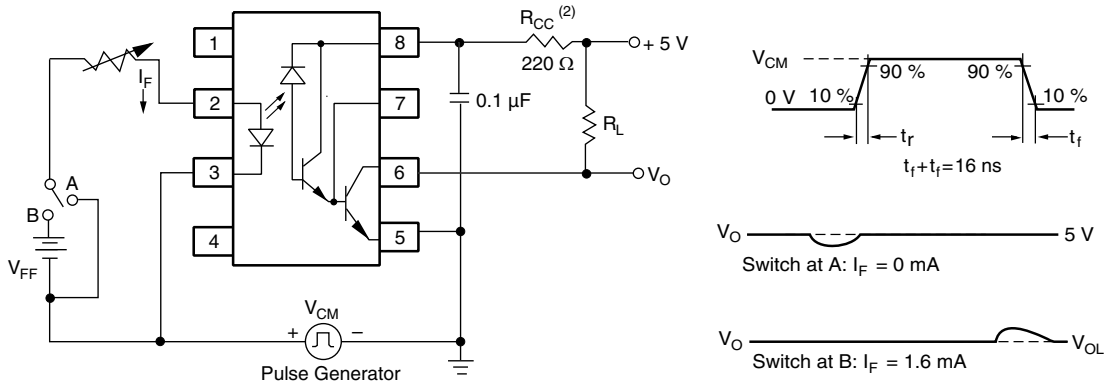


Fig. 4 - Test Circuit for Transient Immunity and Typical Waveforms



SAFETY AND INSULATION RATINGS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		55 / 100 / 21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, $t = 1\text{ min}$	V_{ISO}	3333	V_{RMS}
Tested withstanding isolation voltage	According to UL1577, $t = 1\text{ s}$	V_{ISO}	4000	V_{RMS}
Maximum transient isolation voltage	According to DIN EN 60747-5-5	V_{IOTM}	6000	V_{peak}
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	V_{IORM}	560	V_{peak}
Isolation resistance	$V_{IO} = 500\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$	R_{IO}	$\geq 10^{12}$	Ω
	$V_{IO} = 500\text{ V}$, $T_{amb} = 100\text{ }^{\circ}\text{C}$	R_{IO}	$\geq 10^{11}$	Ω
	$V_{IO} = 500\text{ V}$, $T_{amb} = T_s$	R_{IO}	$\geq 10^9$	Ω
Output safety power		P_{SO}	350	mW
Input safety current		I_{SI}	150	mA
Safety temperature		T_s	165	$^{\circ}\text{C}$
Creepage distance			≥ 4	mm
Clearance distance			≥ 4	mm
Insulation thickness		DTI	≥ 0.3	mm
Input to output test voltage, method B	$V_{IORM} \times 1.875 = V_{PR}$, 100 % production test with $t_M = 1\text{ s}$, partial discharge $< 5\text{ pC}$	V_{PR}	1050	V_{peak}
Input to output test voltage, method A	$V_{IORM} \times 1.6 = V_{PR}$, 100 % sample test with $t_M = 10\text{ s}$, partial discharge $< 5\text{ pC}$	V_{PR}	896	V_{peak}

Note

- As per IEC 60747-5-5, § 7.4.3.8.2, this optocoupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits

TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

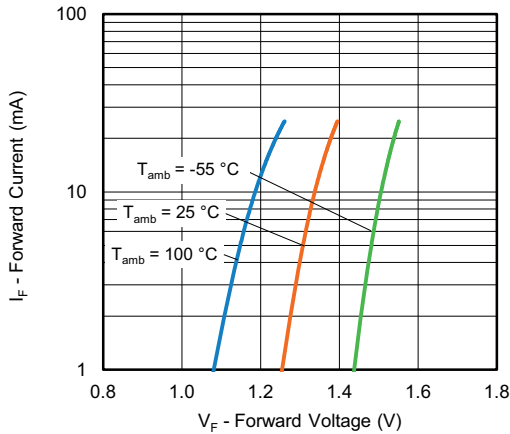


Fig. 5 - Forward Current vs. Forward Voltage

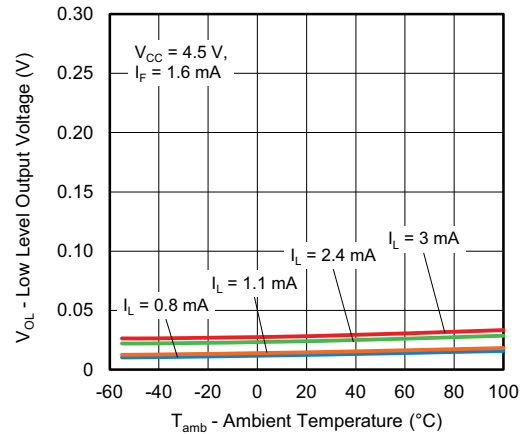


Fig. 8 - Low Level Output Voltage vs. Ambient Temperature

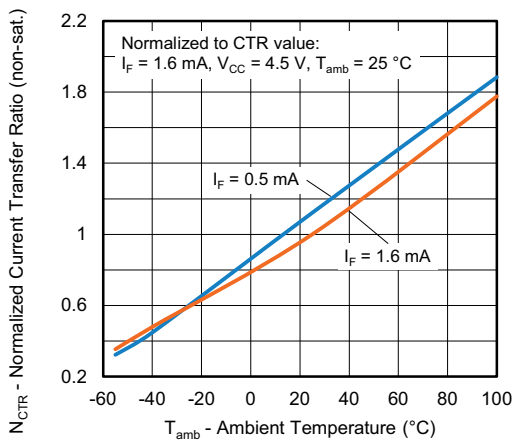


Fig. 6 - Normalized Current Transfer Ratio (non-saturated) vs. Ambient Temperature

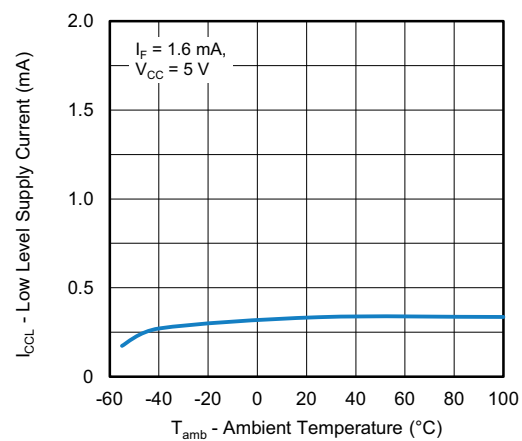


Fig. 9 - Low Level Supply Current vs. Ambient Temperature

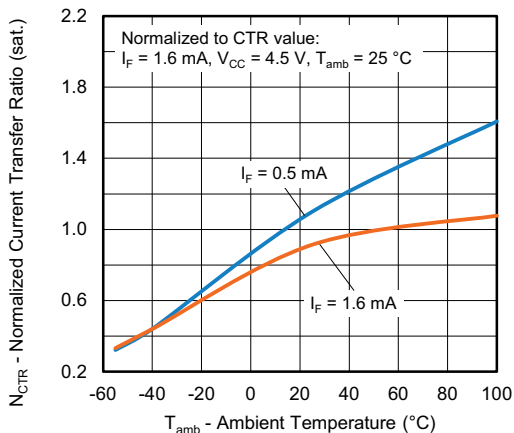
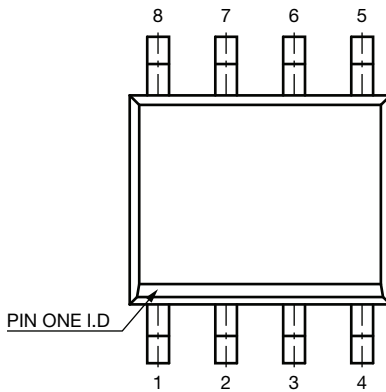
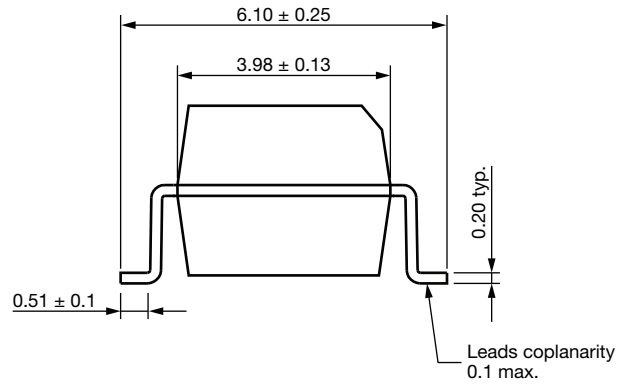
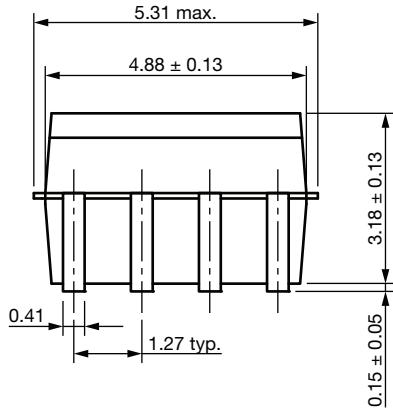


Fig. 7 - Normalized Current Transfer Ratio (saturated) vs. Ambient Temperature



PACKAGE DIMENSIONS (in millimeters)



Technical drawings according to DIN specifications

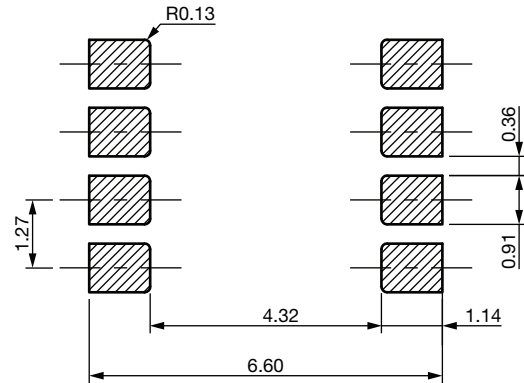


Fig. 10 - Package Drawing

PACKAGE MARKING

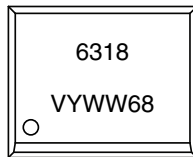


Fig. 11 - Example of SFH6318

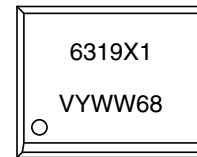
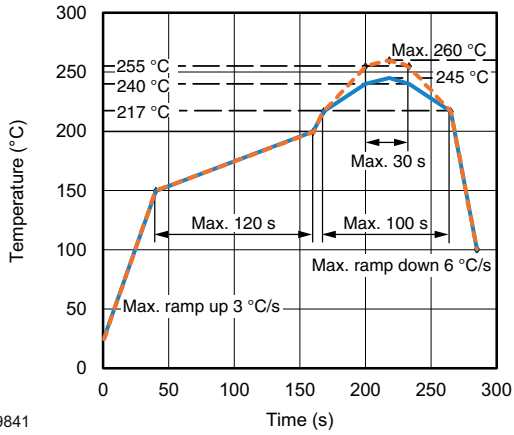


Fig. 12 - Example of SFH6319-X001T

Notes

- "YWW" is the date code marking (Y = year code, WW = week code)
- "X1" is only marked on option 1 parts
- Tape and reel suffix (T) is not part of the package marking

SOLDER PROFILE



19841

Fig. 15 - Lead (Pb)-free Reflow Solder Profile according to J-STD-020

HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 2

Floor life: unlimited

Conditions: $T_{amb} < 30\text{ °C}$, RH < 85 %

Moisture sensitivity level 1, according to J-STD-020



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