0.3 pC Charge Injection, 100 pA Leakage CMOS ± 5 V / 5 V / 3 V 4-Channel Multiplexer

DESCRIPTION

The DG604E is an analog 4-channel CMOS, multiplexer, designed to operate from a +3 V to +16 V single supply, or from ± 3 V to ± 8 V, dual supplies. The DG604E is fully specified at +3 V, +5 V and ± 5 V.

The DG604E offers ultralow charge injection less than ± 0.4 pC over the entire signal range and leakage currents of 16 pA typical at 25 °C. It offers on resistance of 64 Ω typ., and low parasitic capacitance of 4.2 pF source off, and 11 pF Drain on. The part is ideal for analog front end, data acquisition and sample and hold designs providing fast and precision signal switching.

The DG604E switches one of four inputs to a common output as determined by the 3-bit binary address lines: A0, A1, and EN. Each switch conducts equally well in both directions when on, blocks input voltages up to the supply level when off, and exhibits break before make switching action.

All control logic inputs have guaranteed 2 V logic high limits when operating from +5 V or ± 5 V supplies and 1.4 V when operating from a 3 V supply.

The DG604E operating temperature range is specified from -40 °C to +125 °C. It is available in 14 lead TSSOP and the space saving 1.8 mm x 2.6 mm miniQFN package.

FEATURES

- Ultra low charge injection (less than ± 0.4 pC, typ. over the full analog signal range)
- Leakage current < 0.5 nA max. at 85 °C (for DG604EEQ-T1-GE4)
- Low switch capacitance ($C_{S(off)}$, 4.2 pF typ.)
- Fully specified with single supply operation at 3 V, 5 V, and dual supplies at ± 5 V
- CMOS / TTL compatible
- 414 MHz, -3 dB bandwidth
- Excellent isolation and crosstalk performance (typ. > -60 dB at 10 MHz)
- Fully specified from -40 °C to +85 °C and -40 °C to +125 °C
- 14 pin TSSOP and 16 pin miniQFN package (1.8 mm x 2.6 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

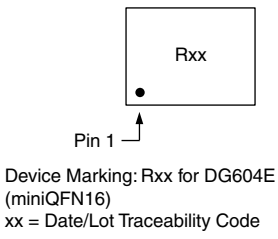
RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

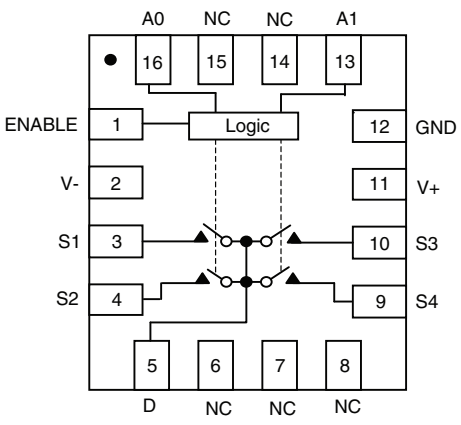
- Data acquisition systems
- Medical instruments
- Precision instruments
- Communications systems
- Automated test equipment
- Sample and hold circuit
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



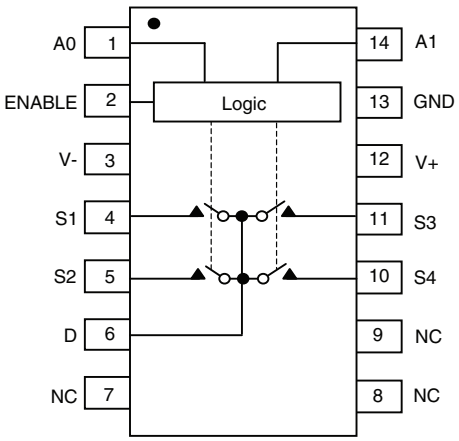
Device Marking: Rxx for DG604E (miniQFN16)
xx = Date/Lot Traceability Code

DG604E
mQFN-16



Top View

DG604E
TSSOP14



Top View

TRUTH TABLE

ENABLE INPUT	SELECTED INPUT		ON SWITCHES
	A1	A0	DG604E
L	X	X	All switches open
H	L	L	D to S1
H	L	H	D to S2
H	H	L	D to S3
H	H	H	D to S4

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +125 °C [a]	14 pin TSSOP	DG604EEQ-T1-GE4
	16 pin miniQFN	DG604EEN-T1-GE4

Note

a. -40 °C to +85 °C datasheet limits apply

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
V+ to V-		-0.3 to +18	V
GND to V-		18	
V_S, V_D		(V-) -0.3 to (V+) + 0.3 or 30 mA, whichever occurs first	
Digital inputs [a]		(GND) -0.3 to (V+) + 0.3	
Continuous current (any terminal)		30	mA
Peak current, S or D (pulsed 1 ms, 10 % duty cycle)		100	
Storage temperature		-65 to +150	°C
Power dissipation (package) [b]	14 pin TSSOP [c]	450	mW
	16 pin miniQFN [d, e]	525	
Thermal resistance (package) [b]	14 pin TSSOP	178	°C/W
	16 pin miniQFN	152	
ESED / HBM	EIA / JESD22-A114-A	2K	V
ESD / CDM	EIA / JESD22-C101-A	1K	
Latch up	JESD78	300	mA

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 5.6 mW/°C above 70 °C
d. Derate 6.6 mW/°C above 70 °C
e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

SPECIFICATIONS FOR DUAL SUPPLIES (V+ = 5 V, V- = -5 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = -5 V $V_{IN\ A0,\ A1,\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	TEMP.[b]	TYP.[c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN.[d]	MAX.[d]	MIN.[d]	MAX.[d]	
Analog Switch									
Analog signal range [e]	V_{ANALOG}		Full	-	-5	5	-5	5	V
Drain-source On-resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	64	-	101	-	101	Ω
			Full	-	-	135	-	119	
On-resistance match	$\Delta R_{DS(on)}$	I_S = 1 mA, V_D = ± 3 V	Room	0.5	-	5	-	5	
			Full	-	-	7	-	6	
On-resistance flatness	$R_{flat(on)}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	15	-	20	-	20	
			Full	-	-	25	-	23	
Switch off leakage current (for 14 pin TSSOP)	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V V_D = ± 4.5 V, V_S = ∓ 4.5 V	Room	± 0.003	-0.1	0.1	-0.1	0.1	nA
			Full	-	-18	18	-0.5	0.5	
	$I_{D(off)}$		Room	± 0.009	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch on leakage current (for 14 pin TSSOP)	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_D = V_S = ± 4.5 V	Room	± 0.016	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch off leakage current (for 16 pin miniQFN)	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V V_D = ± 4.5 V, V_S = ∓ 4.5 V	Room	± 0.003	-1	1	-1	1	
			Full	-	-18	18	-2	2	
	$I_{D(off)}$		Room	± 0.009	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Switch on leakage current (for 16 pin miniQFN)	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_D = V_S = ± 4.5 V	Room	± 0.016	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Digital Control									
Input current, V_{IN} low	I_{IL}	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 0.8 V	Full	0.00001	-0.1	0.1	-0.1	0.1	µA
Input current, V_{IN} high	I_{IH}	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 2 V	Full	0.00001	-0.1	0.1	-0.1	0.1	
Input capacitance	C_{IN}	f = 1 MHz	Room	5	-	-	-	-	pF
Dynamic Characteristics									
Transition time	t_{TRANS}	$V_{S(CLOSE)}$ = 3 V, $V_{S(OPEN)}$ = 0 V, R_L = 300 Ω, C_L = 35 pF	Room	29	-	67	-	67	ns
			Full	-	-	87	-	82	
Turn-on time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 3 V	Room	26	-	54	-	54	
			Full	-	-	61	-	58	
Turn-off time	t_{OFF}		Room	22	-	52	-	52	
			Full	-	-	70	-	57	
Break-before-make time	t_{BBM}	V_S = 3 V R_L = 300 Ω, C_L = 35 pF	Room	7	-	-	-	-	
			Full	-	2	-	2	-	
Charge injection [e]	Q_{INJ}	V_{GEN} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF	Room	-0.3	-	-	-	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-67	-	-	-	-	dB
Bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	414	-	-	-	-	MHz
Channel-to-channel crosstalk [e]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-65	-	-	-	-	dB
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	4.2	-	-	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	6.8	-	-	-	-	
Drain on capacitance [e]	$C_{D(on)}$		Room	11	-	-	-	-	

SPECIFICATIONS FOR DUAL SUPPLIES (V+ = 5 V, V- = -5 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, V- = -5 V $V_{IN\ A0,\ A1,\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	**TEMP.** [b]	**TYP.** [c]	-40 °C to +125 °C		-40 °C to +85 °C		**UNIT**
					MIN. [d]	**MAX.** [d]	**MIN.** [d]	**MAX.** [d]	
Power Supply									
Power supply current	I+	V_{IN} = 0 V or V+	Room	0.0004	-	0.5	-	0.5	µA
			Full	-	-	1	-	1	
Negative supply current	I-		Room	-0.0004	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	
Ground current	I_{GND}		Room	-0.0004	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings

b. All leads welded or soldered to PC board

c. Derate 5.6 mW/°C above 70 °C

d. Derate 6.6 mW/°C above 70 °C

e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

SPECIFICATIONS FOR SINGLE SUPPLY (V+ = 5 V, V- = 0 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = 0 V $V_{IN\ A0,\ A1,\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	TEMP.[b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog signal range [e]	V_{ANALOG}		Full	-	0	5	0	5	V
Drain-source On-resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = +3.5 V	Room	134	-	181	-	181	Ω
			Full	-	-	232	-	208	
On-resistance match	$\Delta R_{DS(on)}$	I_S = 1 mA, V_D = +3.5 V	Room	1.4	-	7	-	7	
			Full	-	-	9	-	8	
On-resistance flatness	$R_{flat(on)}$	I_S = 1 mA, V_D = 0 V, +3.5 V	Room	36	-	50	-	50	
			Full	-	-	54	-	52	
Switch off leakage current (for 14 pin TSSOP)	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V V_D = 1 V / 4.5 V, V_S = 4.5 V / 1 V	Room	± 0.002	-0.1	0.1	-0.1	0.1	nA
			Full	-	-18	18	-0.5	0.5	
	$I_{D(off)}$		Room	± 0.007	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch on leakage current (for 14 pin TSSOP)	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V V_D = V_S = 1 V / 4.5 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch off leakage current (for 16 pin miniQFN)	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V V_D = 1 V / 4.5 V, V_S = 4.5 V / 1 V	Room	± 0.002	-1	1	-1	1	
			Full	-	-18	18	-2	2	
	$I_{D(off)}$		Room	± 0.007	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Switch on leakage current (for 16 pin miniQFN)	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V, V_D = V_S = 1 V / 4.5 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Digital Control									
Input current, V_{IN} low	I_{IL}	$V_{IN\ A0,\ A1,\ and\ ENABLE}$ Under test = 0.8 V	Full	0.00001	-0.1	0.1	-0.1	0.1	µA
Input current, V_{IN} high	I_{IH}	$V_{IN\ A0,\ A1,\ and\ ENABLE}$ Under test = 2 V	Full	0.00001	-0.1	0.1	-0.1	0.1	
Input capacitance	C_{IN}	f = 1 MHz	Room	5	-	-	-	-	pF
Dynamic Characteristics									
Transition time	t_{TRANS}	$V_{S(CLOSE)}$ = 3 V, $V_{S(OPEN)}$ = 0 V, R_L = 300 Ω, C_L = 35 pF	Room	47	-	70	-	70	ns
			Full	-	-	116	-	91	
Turn-on time	t_{ON}		Room	32	-	52	-	52	
			Full	-	-	63	-	57	
Turn-off time	t_{OFF}		Room	26	-	46	-	46	
			Full	-	-	61	-	55	
Break-before-make-time	t_{BMM}		Room	22	-	-	-	-	
			Full	-	3	-	3	-	
Charge injection [e]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Full	-0.03	-	-	-	-	pC
Off-isolation [e]	OIRR	f = 10 MHz, R_L = 50 Ω, C_L = 5 pF	Room	-66	-	-	-	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-64	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	358	-	-	-	-	MHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	4.4	-	-	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$			7.3	-	-	-	-	
Drain on capacitance [e]	$C_{D(on)}$			12	-	-	-	-	

SPECIFICATIONS FOR SINGLE SUPPLY (V+ = 5 V, V- = 0 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, V- = 0 V $V_{IN\ A0,\ A1,\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	**TEMP.[b]**	**TYP. [c]**	-40 °C to +125 °C		-40 °C to +85 °C		**UNIT**
					MIN. [d]	**MAX. [d]**	**MIN. [d]**	**MAX. [d]**	
Power Supply									
Power supply current	I+	V_{IN} = 0 V or V+	Room	0.0002	-	0.5	-	0.5	µA
			Full	-	-	1	-	1	
Negative supply current	I-		Room	-0.0002	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	
Ground current	I_{GND}		Room	-0.0002	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 5.6 mW/°C above 70 °C
d. Derate 6.6 mW/°C above 70 °C
e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

SPECIFICATIONS FOR SINGLE SUPPLY (V+ = 3 V, V- = 0 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V- = 0 V $V_{IN\ A0,\ A1,\ AND\ ENABLE}$ = 1.4 V, 0.6 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog signal range [e]	V_{ANALOG}		Full	-	-	3	-	3	V
Drain-source On-resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = +1.5 V	Room	319	-	416	-	416	Ω
			Full	-	-	478	-	453	
On-resistance match	$\Delta R_{DS(on)}$	I_S = 1 mA, V_D = +1.5 V	Room	7	-	15	-	15	
			Full	-	-	17	-	16	
Switch off leakage current (for 14 pin TSSOP)	$I_{S(off)}$	V+ = 3.3 V, V- = 0 V V_D = 1 V / 3 V, V_S = 3 V / 1 V	Room	± 0.001	-0.1	0.1	-0.1	0.1	nA
			Full	-	-18	18	-0.5	0.5	
	$I_{D(off)}$		Room	± 0.006	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch on leakage current (for 14 pin TSSOP)	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V V_D = V_S = 1 V / 3 V	Room	± 0.006	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch off leakage current (for 16 pin miniQFN)	$I_{S(off)}$	V+ = 3.3 V, V- = 0 V V_D = 1 V / 3 V, V_S = 3 V / 1 V	Room	± 0.001	-1	1	-1	1	
			Full	-	-18	18	-2	2	
	$I_{D(off)}$		Room	± 0.006	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Switch on leakage current (for 16 pin miniQFN)	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V, V_D = V_S = 1 V / 3 V	Room	± 0.006	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Digital Control									
Input current, V_{IN} low	I_{IL}	$V_{IN\ A0,\ A1\ and\ ENABLE}$ under test = 0.6 V	Full	0.000008	-1	1	-1	1	µA
Input current, V_{IN} high	I_{IH}	$V_{IN\ A0,\ A1\ and\ ENABLE}$ under test = 1.4 V	Full	0.000008	-1	1	-1	1	
Input capacitance	C_{IN}	f = 1 MHz	Room	5	-	-	-	-	pF
Dynamic Characteristics									
Transition time	t_{TRANS}	$V_{S(CLOSE)}$ = 3 V, $V_{S(OPEN)}$ = 0 V, R_L = 300 Ω, C_L = 35 pF	Room	138	-	163	-	163	ns
			Full	-	-	197	-	195	
Turn-on time	t_{ON}		Room	95	-	117	-	117	
			Full	-	-	145	-	135	
Turn-off time	t_{OFF}		Room	55	-	76	-	76	
			Full	-	-	98	-	90	
Break-before-make-time	t_{BMM}		Room	58	-	-	-	-	
			Full	-	5	-	5	-	
Charge injection [e]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Full	0.01	-	-	-	-	pC
Off-isolation [e]	OIRR	f = 10 MHz, R_L = 50 Ω, C_L = 5 pF	Room	-66	-	-	-	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-64	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	318	-	-	-	-	MHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	4.6	-	-	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	7.7	-	-	-	-	
Channel on capacitance [e]	$C_{D(on)}$		Room	12.6	-	-	-	-	

SPECIFICATIONS FOR SINGLE SUPPLY (V+ = 3 V, V- = 0 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 3 V, V- = 0 V $V_{IN\ A0,\ A1,\ AND\ ENABLE}$ = 1.4 V, 0.6 V [a]	**TEMP.** [b]	**TYP.** [c]	-40 °C to +125 °C		-40 °C to +85 °C		**UNIT**
					MIN. [d]	**MAX.** [d]	**MIN.** [d]	**MAX.** [d]	
Power Supply									
Power supply current	I+	V_{IN} = 0 V or V+	Room	0.0001	-	0.5	-	0.5	µA
			Full	-	-	1	-	1	
Negative supply current	I-		Room	-0.0001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	
Ground current	I_{GND}		Room	-0.0001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 5.6 mW/°C above 70 °C
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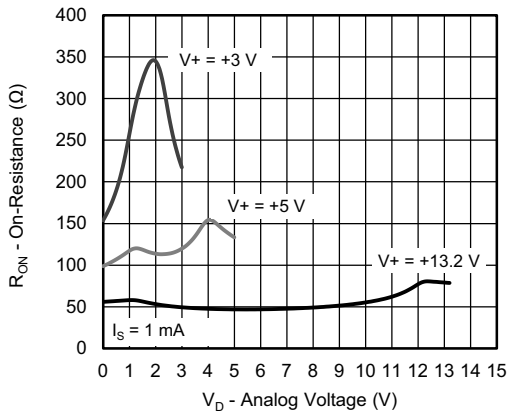
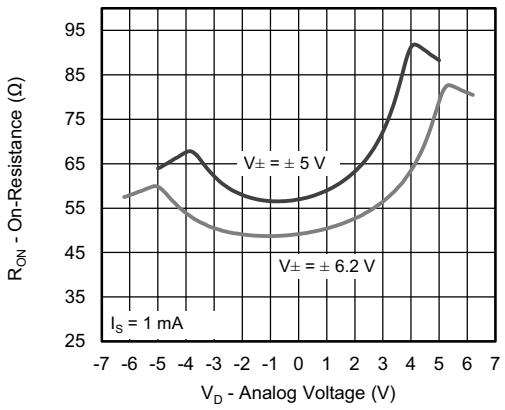
e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

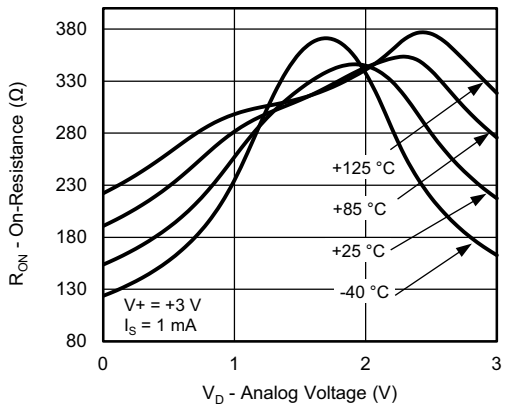
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



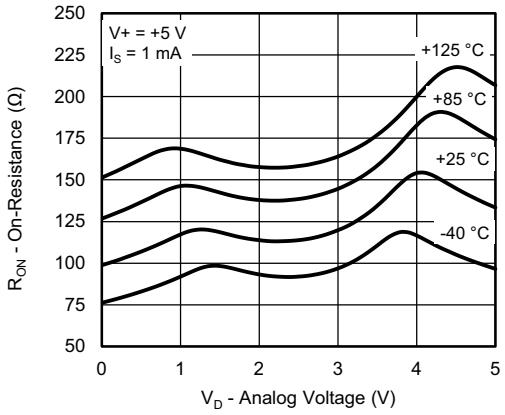
On-Resistance vs. V_D (Single Supply Voltage)



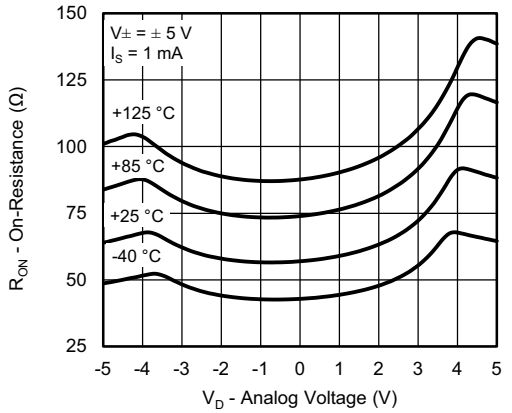
On-Resistance vs. V_D (Dual Supply Voltage)



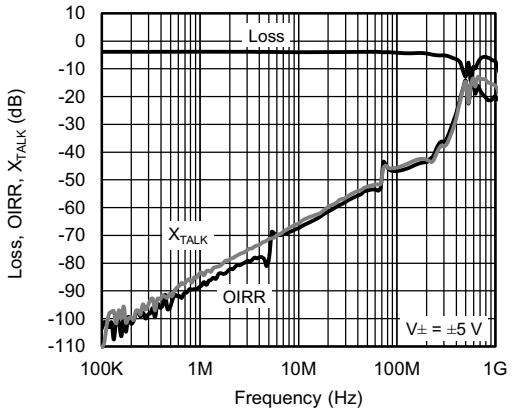
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

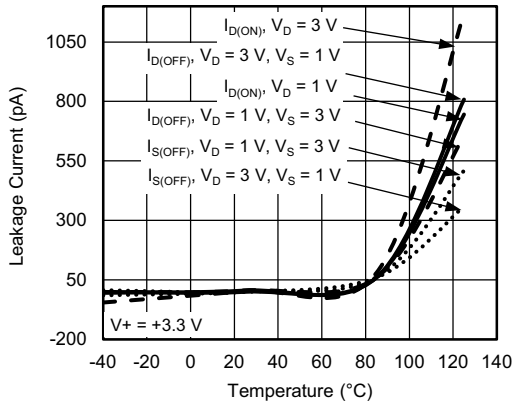


On-Resistance vs. Analog Voltage and Temperature

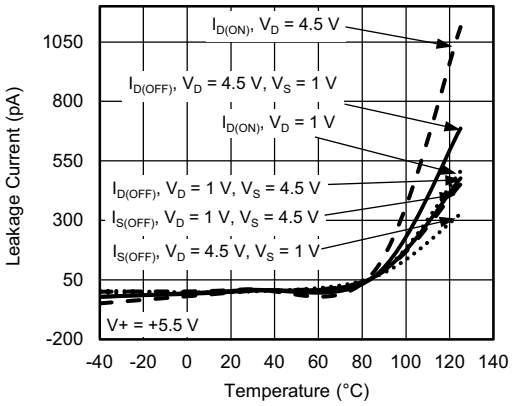


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

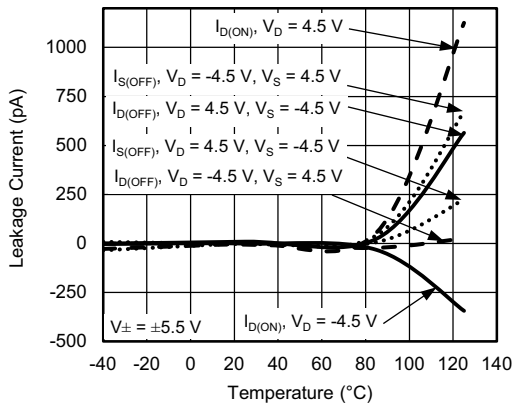
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



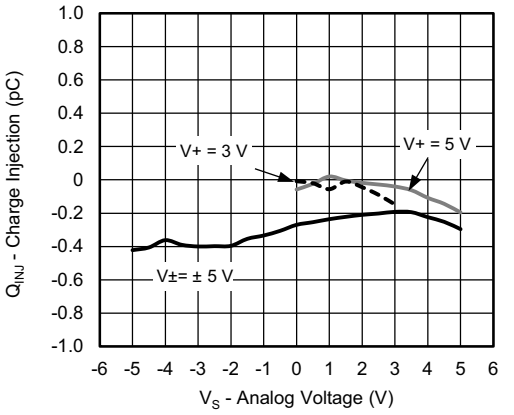
Leakage Current vs. Temperature



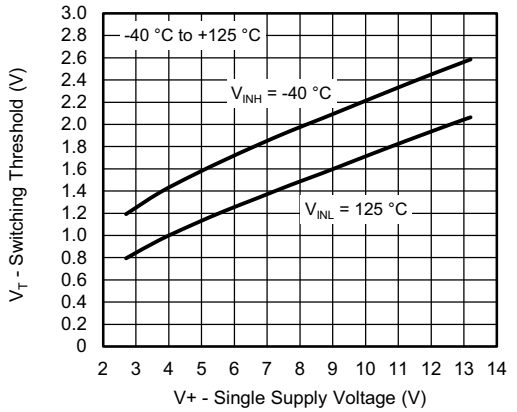
Leakage Current vs. Temperature



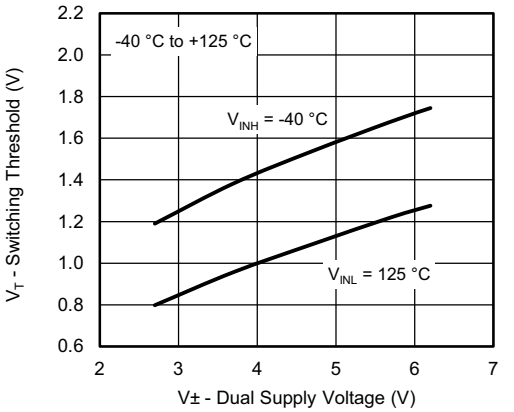
Leakage Current vs. Temperature



Charge Injection vs. Analog Voltage

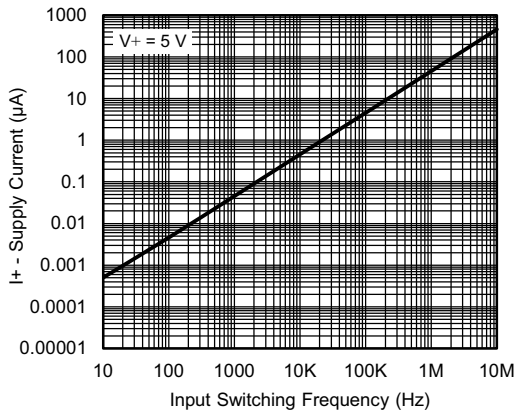


Switching Threshold vs. Supply Voltage

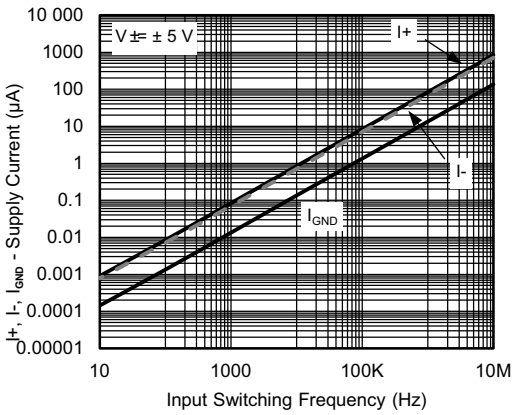


Switching Threshold vs. Supply Voltage

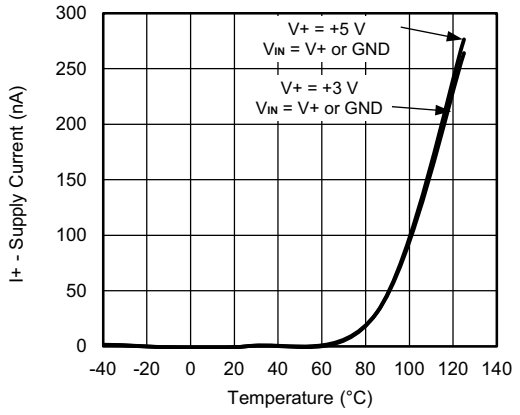
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



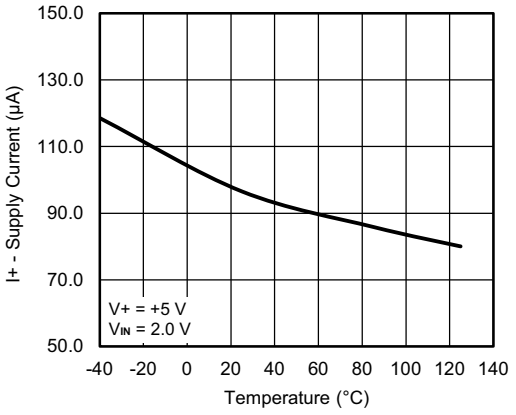
Supply Current vs. Switching Frequency



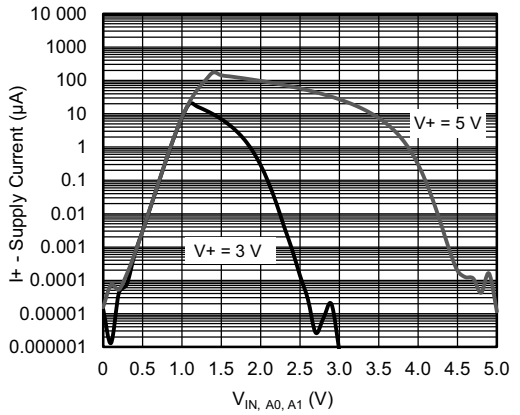
Supply Current vs. Switching Frequency



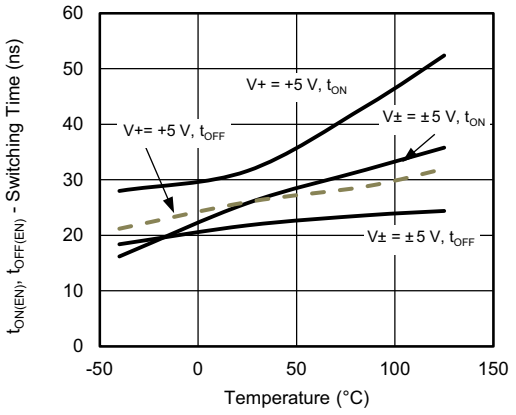
Supply Current vs. Temperature



Supply Current vs. Temperature



Supply Current vs. Enable Input Voltage



Switching Time vs. Temperature

TEST CIRCUITS

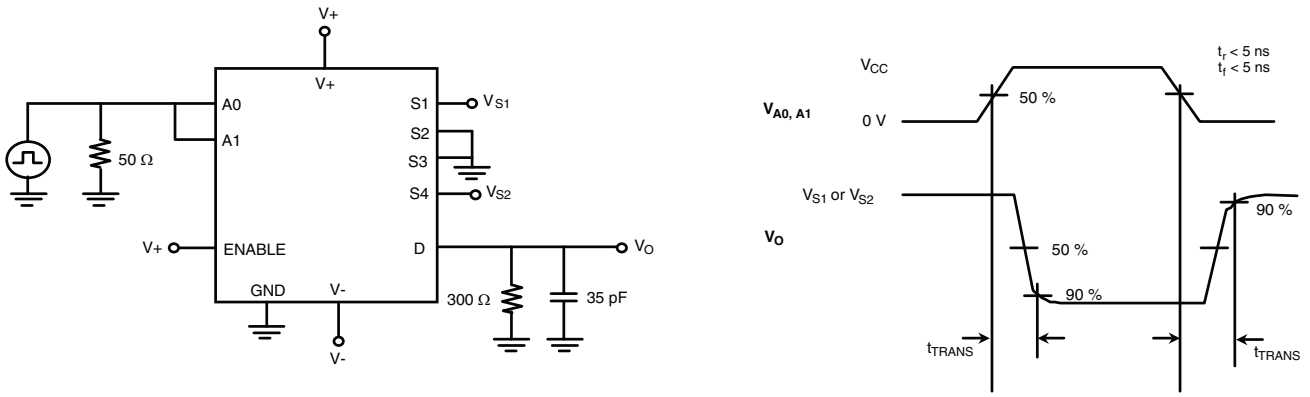


Fig. 1 - Transition Time

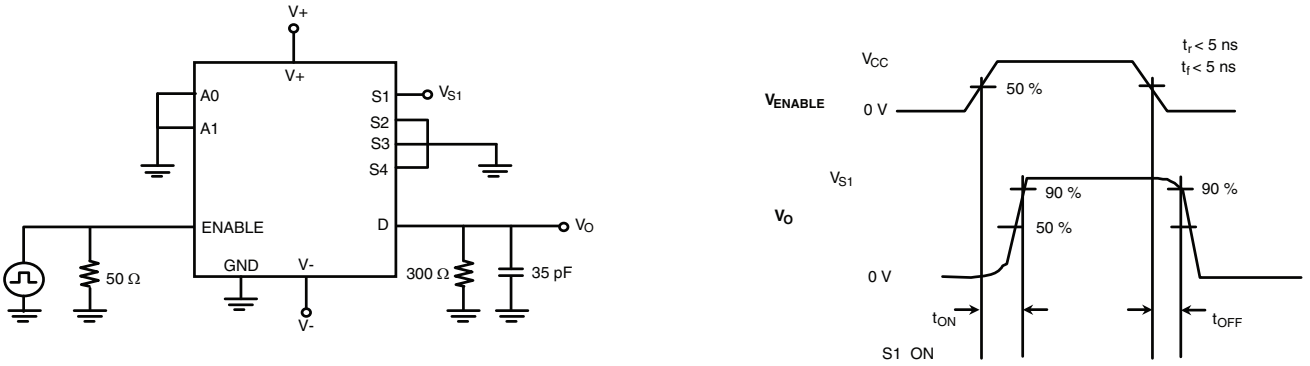


Fig. 2 - Enable Switching Time

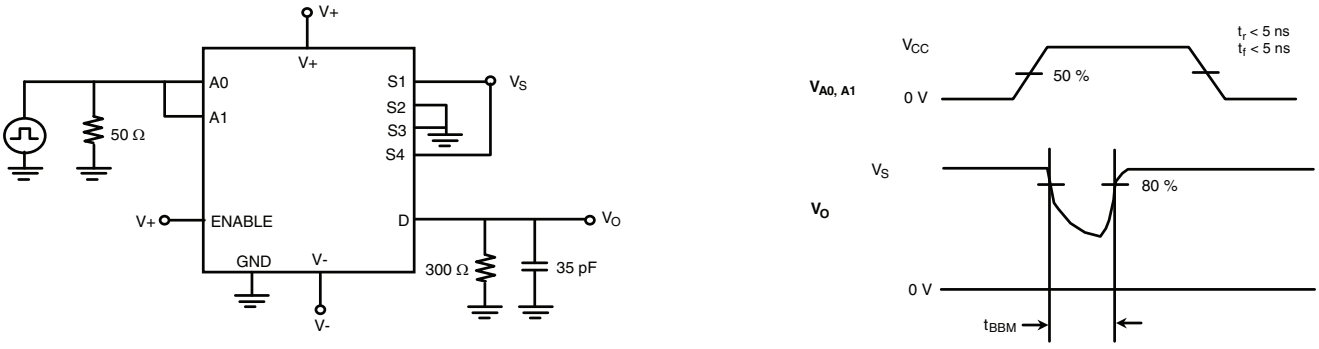
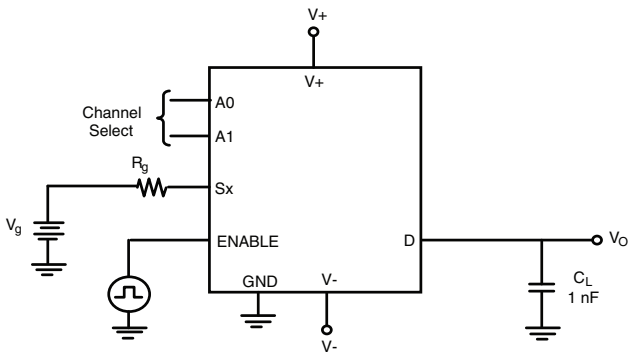


Fig. 3 - Break-Before-Make

TEST CIRCUITS



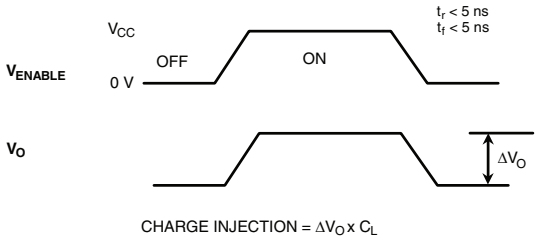


Fig. 4 - Charge Injection

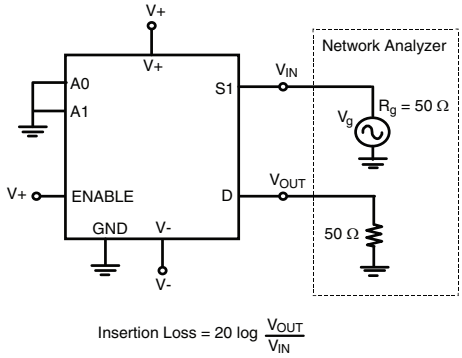


Fig. 5 - Insertion Loss

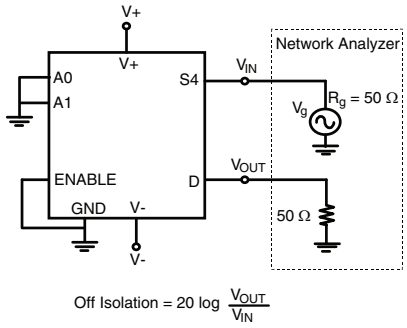


Fig. 6 - Off-Isolation

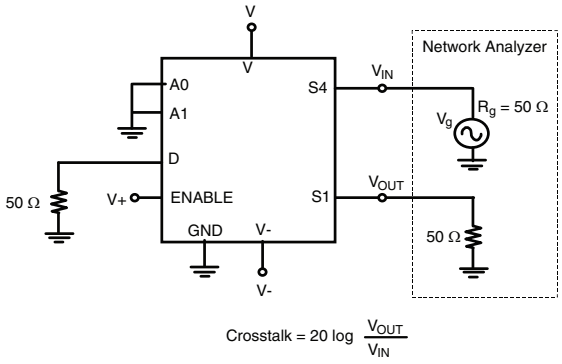


Fig. 7 - Crosstalk

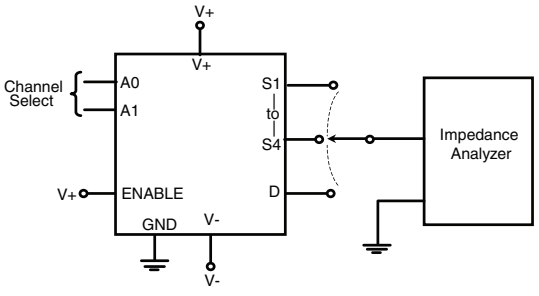
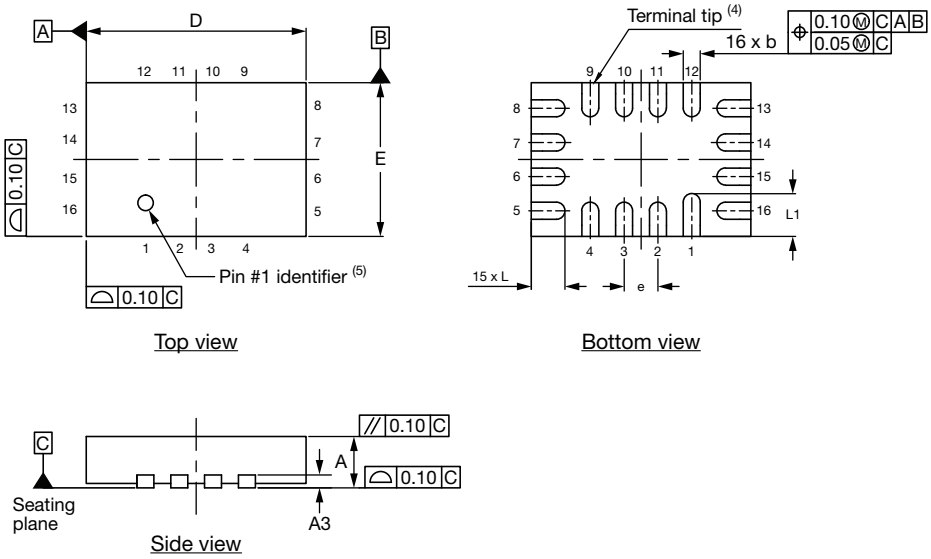


Fig. 8 - Source / Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75612.

Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

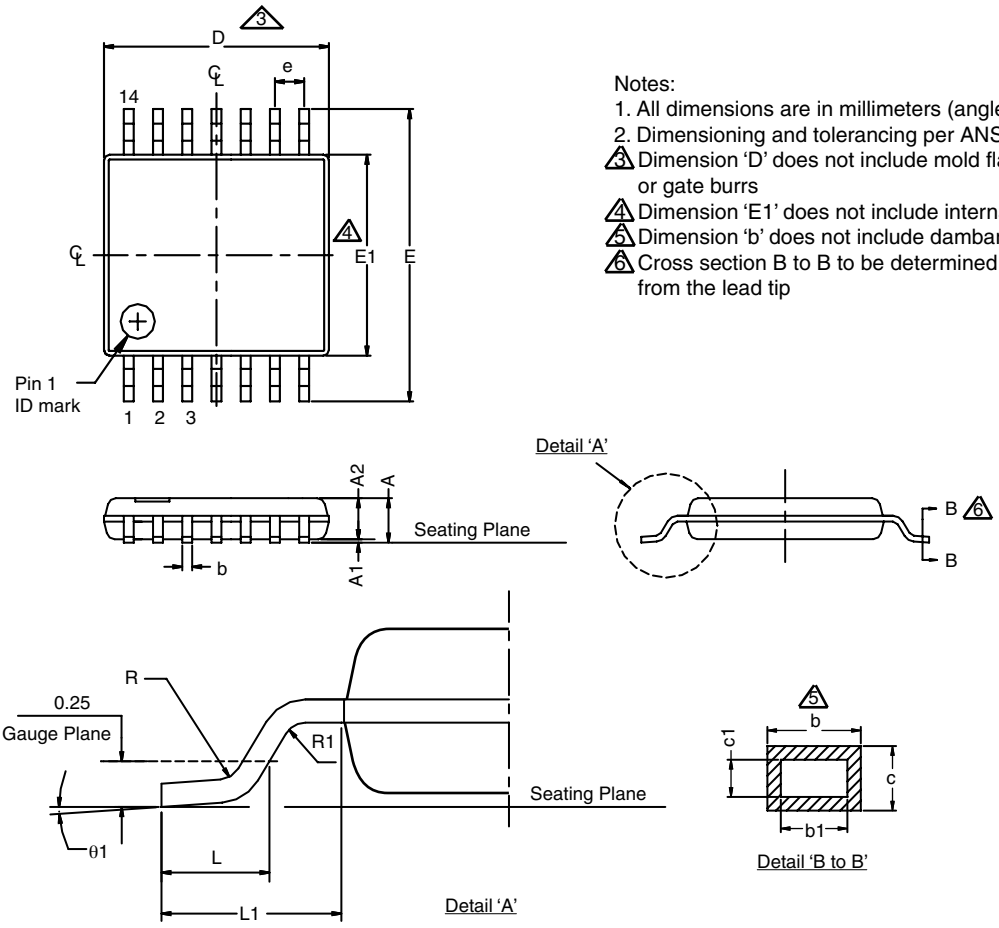
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

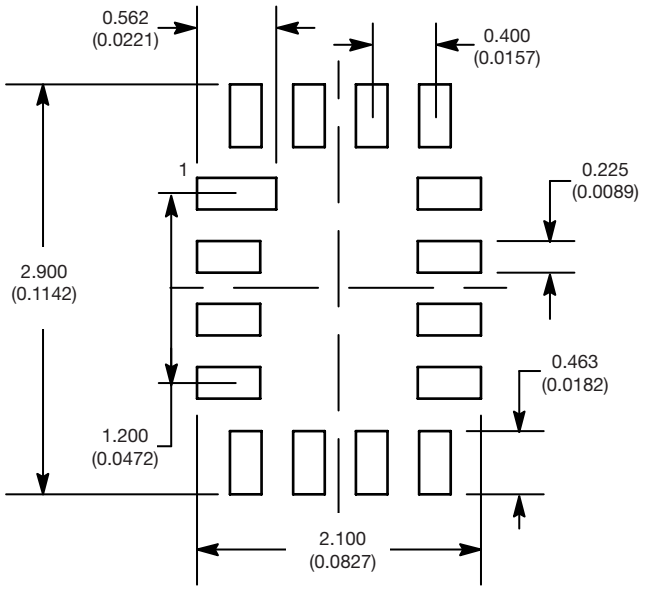
14L TSSOP



Notes:
1. All dimensions are in millimeters (angles in degrees)
2. Dimensioning and tolerancing per ANSI Y14.5M-1982
3. Dimension 'D' does not include mold flash, protrusions or gate burrs
4. Dimension 'E1' does not include internal flash or protrusion
5. Dimension 'b' does not include dambar protrusion
6. Cross section B to B to be determined at 0.10 mm to 0.25 mm from the lead tip

SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.05
D	4.9	5.0	5.1
E1	4.3	4.4	4.5
E	6.2	6.4	6.6
L	0.45	0.60	0.75
R	0.09	-	-
R1	0.09	-	-
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
θ1	0°	-	8°
L1	1.0 ref.		
e	0.65 BSC		
ECN: T-07766-Rev. A, 14-Jan-08 DWG: 5962			

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

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