

Vishay Siliconix

Automotive Dual N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.060			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.080			
I _D (A) per leg	8			
Configuration	Dual			

FEATURES

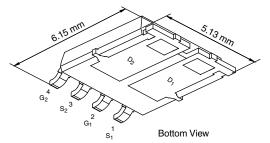
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified
- 100 % R_q and UIS Tested
- Material categorization:
 For definitions of compliance please see www.vishay.com/doc?99912

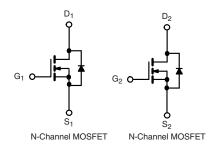




ROHS COMPLIANT HALOGEN FREE

PowerPAK® SO-8L Dual





ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ962EP-T1-GE3

ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unless	s otherwise noted	d)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	60		
Gate-Source Voltage		V _{GS} ± 20		V	
Continuous Drain Current ^a	T _C = 25 °C	l _D	8		
	T _C = 125 °C		8		
Continuous Source Current (Diode Conduction) ^a		I _S	8	А	
Pulsed Drain Current ^b		I _{DM}	32		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	10		
Single Pulse Avalanche Energy	L = U.1 Min	E _{AS}	5	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	25	W	
	T _C = 125 °C		8	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg} - 55 to + 17		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260	U	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	85	°C/W	
Junction-to-Case (Drain)		R_{thJC}	6	C/VV	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static						l .		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60		-	V	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		1.5	2.0	2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current		V _{GS} = 0 V	V _{DS} = 60 V	-	-	1		
	I _{DSS}	V _{GS} = 0 V	V _{DS} = 60 V, T _J = 125 °C	-	-	50	μA	
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 175 °C	-	-	150		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	15	-	-	Α	
Drain-Source On-State Resistance ^a		V _{GS} = 10 V	I _D = 4.3 A	-	0.046	0.060	Ω	
		V _{GS} = 10 V	I _D = 4.3 A, T _J = 125 °C	-		0.102		
	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.3 A, T _J = 175 °C	-	-	0.127		
		V _{GS} = 4.5 V	I _D = 3.5 A	-	0.060	0.080		
Forward Transconductance ^b	9 _{fs}	V _{DS} = 15 V, I _D = 4.3 A		-	10	-	S	
Dynamic ^b								
Input Capacitance	C _{iss}		V _{DS} = 25 V, f = 1 MHz	-	379	475	pF	
Output Capacitance	C _{oss}	V _{GS} = 0 V		-	72	90		
Reverse Transfer Capacitance	C _{rss}			-	32	40		
Total Gate Charge ^c	Qg		V _{DS} = 30 V, I _D = 4.5 A	-	8.5	14	nC	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V		-	1.4	-		
Gate-Drain Charge ^c	Q_{gd}			-	3.3	-		
Gate Resistance	R _g	f = 1 MHz		2.25	4.50	6.75	Ω	
Turn-On Delay Time ^c	t _{d(on)}			-	5	8		
Rise Time ^c	t _r	$V_{DD} = 30 \text{ V}, \text{ R}_{L} = 30 \Omega$ $I_{D} \cong 1 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	11	17	ns	
Turn-Off Delay Time ^c	t _{d(off)}			-	16	24		
Fall Time ^c	t _f			-	6	9		
Source-Drain Diode Ratings and Char	acteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	32	Α	
Forward Voltage	V_{SD}	$I_F = 3.5 \text{ A}, V_{GS} = 0 \text{ V}$		-	0.8	1.1	V	

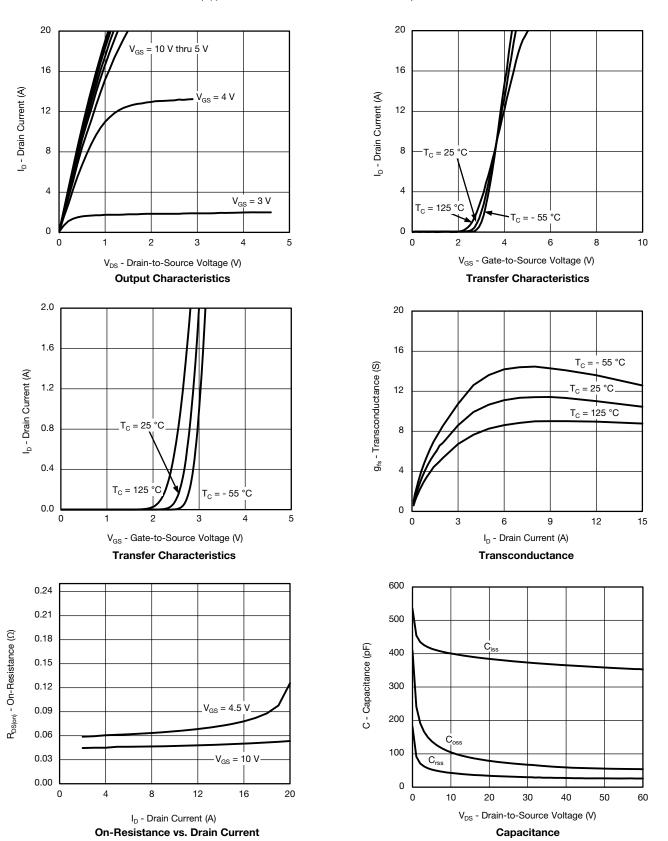
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

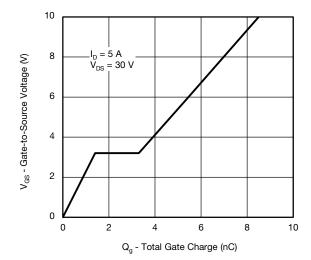


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

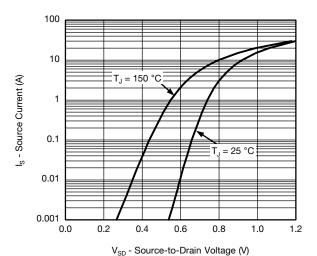




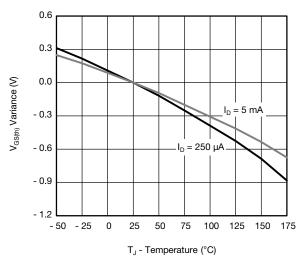
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



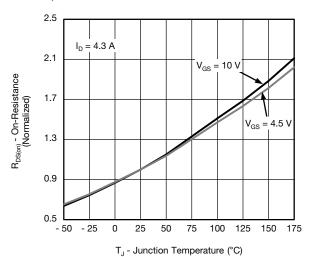
Gate Charge



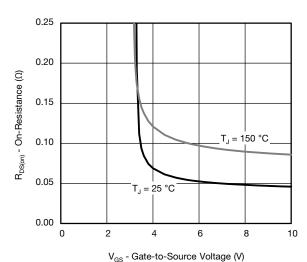
Source Drain Diode Forward Voltage



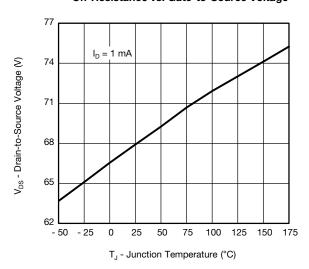
Threshold Voltage



On-Resistance vs. Junction Temperature



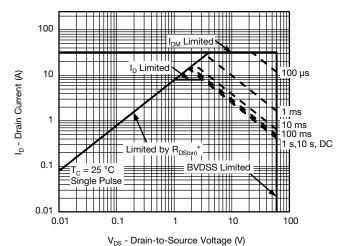
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature

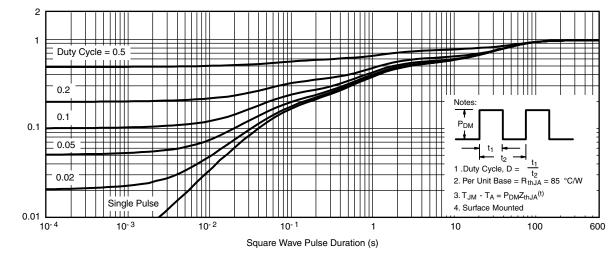
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

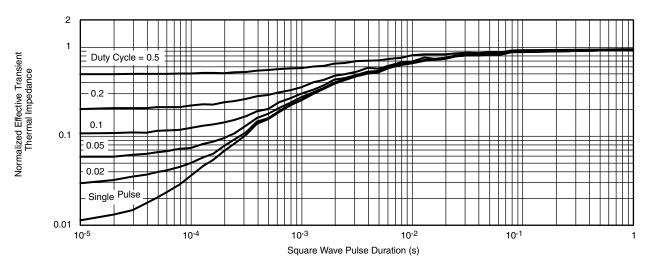


Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Effective Transient Thermal Impedance

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 - are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67018.

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