



N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (TYP.)			
30	0.560 at V _{GS} = 4.5 V	0.5				
	0.620 at V _{GS} = 2.5 V	0.2	0.72 nC			
	0.700 at V _{GS} = 1.8 V	0.2	0.72110			
	1.100 at V _{GS} = 1.5 V	0.05				



FEATURES

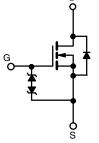
- TrenchFET® power MOSFET
- 100 % R_a tested
- Gate-source ESD protected: 1000 V
- Material categorization:
 For definitions of compliance please see www.vishay.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- · Load switch
- · High speed switching
- DC/DC converters / boost converters
- For smart phones, tablet PCs and mobile computing



N-Channel MOSFET

Marking Code: L Ordering Information:

Si1002R-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 8]	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	- I _D	0.61 ^{a,b}		
	T _A = 70 °C		0.49 ^{a,b}	А	
Pulsed Drain Current (t = 100 μs)		I _{DM}	2		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.18 ^{a,b}	А	
Maximum Dayyar Dissination 8	T _A = 25 °C	- P _D	0.22 ^{a,b}	10/	
Maximum Power Dissipation ^a	T _A = 70 °C		0.14 ^{a,b}	W	
Operating Junction and Storage Temperature R	T _J , T _{stg}	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient ^b	t ≤ 5 s	R _{thJA}	470	565	°C/W	
Waximum Junction-to-Ambient ~	Steady State		560	675		

Notes

a. Surface mounted on 1" x 1" FR4 board.

b. t = 5 s.



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$		-	29	-	mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	I _D = 250 μA	-	-1.8	-		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	0.4	-	1	V	
0.1.0.0		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	-	-	± 30		
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	-	-	± 1		
Zoro Cata Valtaga Drain Current	1	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	– μA –	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 85 °C	-	-	3		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	2	-	-	Α	
		$V_{GS} = 4.5 \text{ V}, I_D = 0.5 \text{ A}$	-	0.450	0.560	Ω	
Duain Course On State Desigtance A	В	$V_{GS} = 2.5 \text{ V}, I_D = 0.2 \text{ A}$	-	0.500	0.620		
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	V _{GS} = 1.8 V, I _D = 0.2 A	-	0.560	0.700		
		V _{GS} = 1.5 V, I _D = 0.05 A	-	0.647	1.100		
Forward Transconductance	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 0.5 \text{ A}$	-	7.5	-	S	
Dynamic ^b							
Input Capacitance	C _{iss}		-	36	-		
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	9	-	pF	
Reverse Transfer Capacitance	C _{rss}		-	5	-		
Total Cata Charge	Qg	V _{DS} = 15 V, V _{GS} = 8 V, I _D = 0.5 A	-	1.2	2	nC	
Total Gate Charge			-	0.72	1.2		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 0.5 \text{ A}$	-	0.1	-		
Gate-Drain Charge	Q _{gd}		-	0.16	-		
Gate Resistance	Rg	f = 1 MHz	2.4	12.2	24.4	Ω	
Turn-On Delay Time	t _{d(on)}		-	6	15		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 37.5 \Omega$	-	13	24		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 0.4 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	20	30	ns	
Fall Time	t _f		-	11	20		
Drain-Source Body Diode Characterist	tics						
Pulse Diode Forward Current ^a	I _{SM}		-	-	2	Α	
Body Diode Voltage	V_{SD}	I _S = 0.5 A	-	0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}		-	8	15	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			2	4	nC	
Reverse Recovery Fall Time t_a $I_F = 0.4 \text{ A}, dI/dt = 100 A/\mu s$ Reverse Recovery Rise Time t_b		IF = 0.4 A, αΙ/ατ = 100 A/μS	-	4	-	r	
		-	4	-	ns		

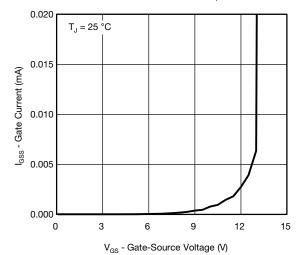
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

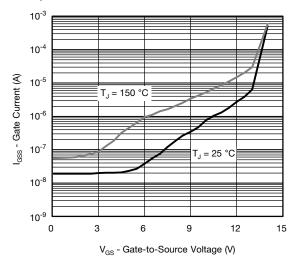
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



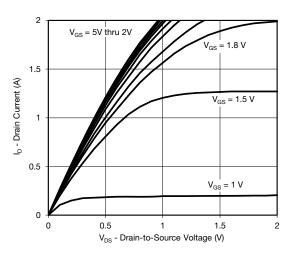
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



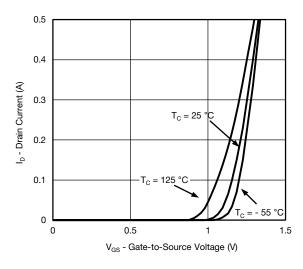
Gate Current vs. Gate-Source Voltage



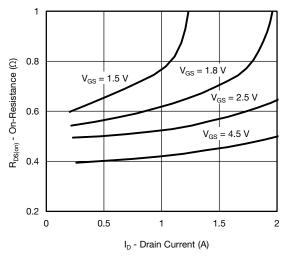
Gate Current vs. Gate-Source Voltage

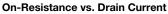


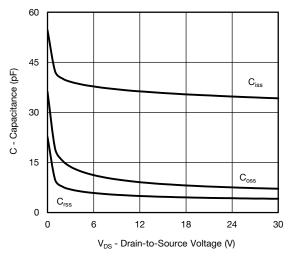
Output Characteristics



Transfer Characteristics



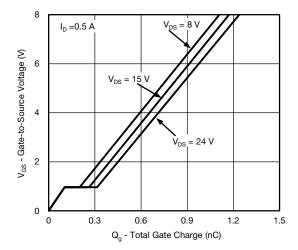




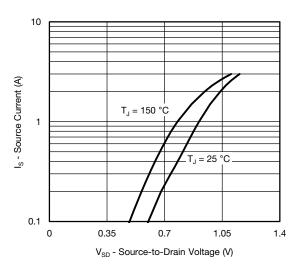
Capacitance



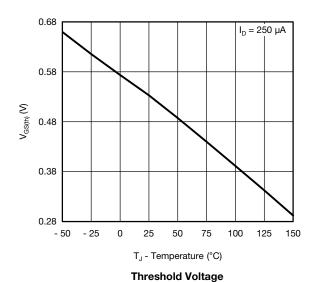
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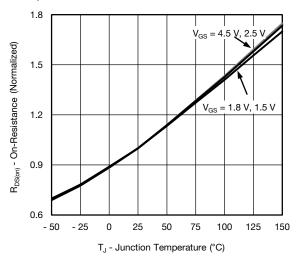


Gate Charge

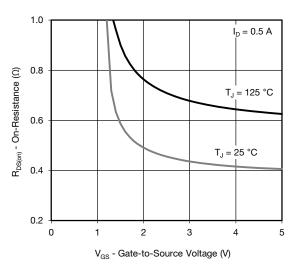


Soure-Drain Diode Forward Voltage

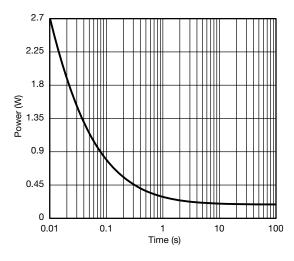




On-Resistance vs. Junction Temperature



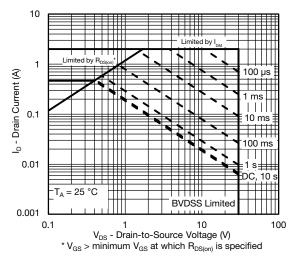
On-Resistance vs. Gate-to-Source Voltage

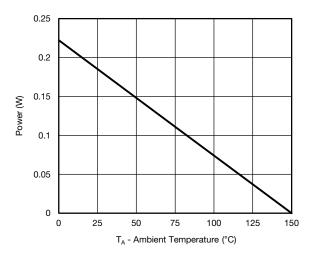


Single Pulse Power, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

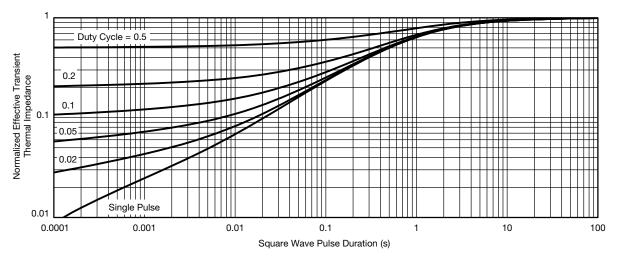




Safe Operating Area, Junction-to-Ambient

Power Derating, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

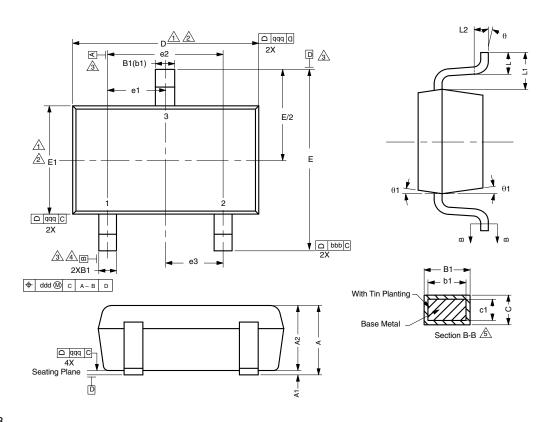


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg264257.



SC-75A: 3 Leads



DWG: 5868

Notes

Dimensions in millimeters will govern.

- Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
- Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- ②Datums A, B and D to be determined 0.10 mm from the lead tip.

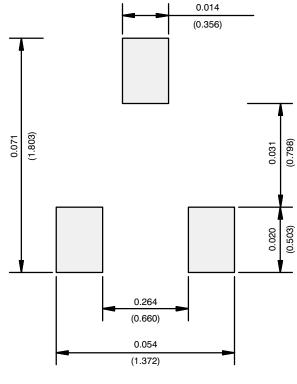
 4\text{Terminal positions are shown for reference only.}
- These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.10		

DIM.	ı	NOTE		
	MIN.	NOM.	MAX.	NOTE
Α	-	-	0.80	
A1	0.00	-	0.10	
A2	0.65	0.70	0.80	
B1	0.19	-	0.24	5
b1	0.17	-	0.21	
С	0.13	-	0.15	5
c1	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
Е	1.50	1.60	1.70	
E1	0.66	0.76	0.86	1, 2
e1	0.50 BSC			
e2	1.00 BSC			
e3	0.50 BSC			
L	0.15	0.205	0.30	
L1	0.40 ref.			
L2	0.15 BSC			
q	0°	- 8°		
q1	4°	- 10°		



RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE

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