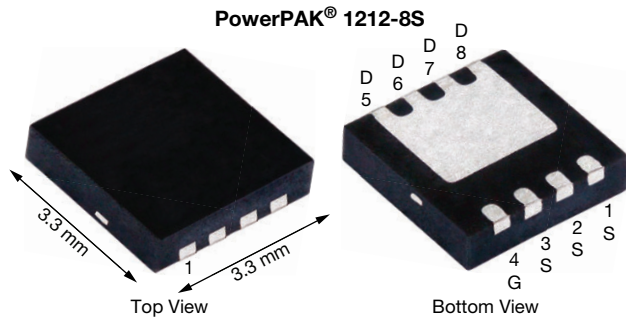


N-Channel 30 V (D-S) MOSFET



FEATURES

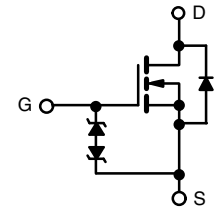
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Thin 0.75 mm height
- Typical ESD performance 2500 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC converter
- Battery switch
- Power management
- For mobile computing



N-Channel MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0048
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0062
Q _g typ. (nC)	14
I _D (A)	50 ^a
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiS496EDNT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	30	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	50 ^a
		T _C = 70 °C	50 ^a
		T _A = 25 °C	20.4 ^{b, c}
		T _A = 70 °C	16.3 ^{b, c}
Pulsed drain current (t = 100 μs)	I _{DM}	200	
Avalanche current	L = 0.1 mH	I _{AS}	25
Avalanche energy		E _{AS}	31
Continuous source-drain diode current	I _S	T _C = 25 °C	43.3
		T _A = 25 °C	3.2 ^{b, c}
Maximum power dissipation	P _D	T _C = 25 °C	52
		T _C = 70 °C	33
		T _A = 25 °C	3.8 ^{b, c}
		T _A = 70 °C	2 ^{b, c}
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{b, f}	R _{thJA}	24	33	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	1.9	2.4		

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The Thin PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 81 °C/W



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	30	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.2	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	-	2.5	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 20	μA
		$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 10\text{ V}$	-	-	± 1	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$	-	-	5	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	20	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	0.0040	0.0048	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 18\text{ A}$	-	0.0051	0.0062	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 20\text{ A}$	-	80	-	S
Dynamic ^b						
Input capacitance	C_{ISS}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	1515	-	pF
Output capacitance	C_{OSS}		-	322	-	
Reverse transfer capacitance	C_{RSS}		-	175	-	
Total gate charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	29	45	nC
		$V_{DS} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$	-	14	21	
Gate-source charge	Q_{gs}		-	4.5	-	
Gate-drain charge	Q_{gd}		-	4.2	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.2	1.2	2.4	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	20	30	ns
Rise time	t_r		-	125	190	
Turn-off delay time	$t_{d(off)}$		-	24	40	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	-	10	20	
Rise time	t_r		-	16	24	
Turn-off delay time	$t_{d(off)}$		-	25	40	
Fall time	t_f		-	3	8	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	50	A
Pulse diode forward current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	200	
Body diode voltage	V_{SD}	$I_S = 10\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	-	20	40	ns
Body diode reverse recovery charge	Q_{rr}		-	10	20	nC
Reverse recovery fall time	t_a		-	8	-	ns
Reverse recovery rise time	t_b		-	12	-	

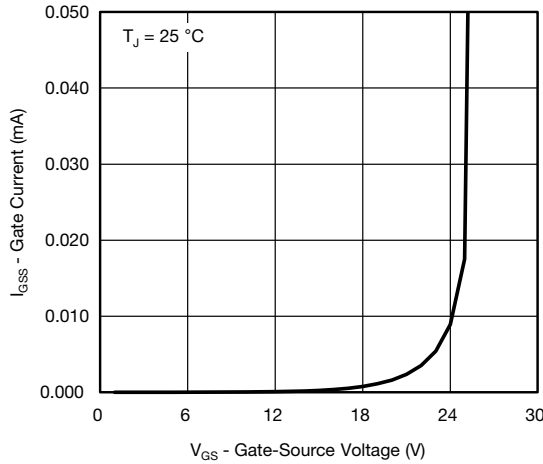
Notes

- a. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

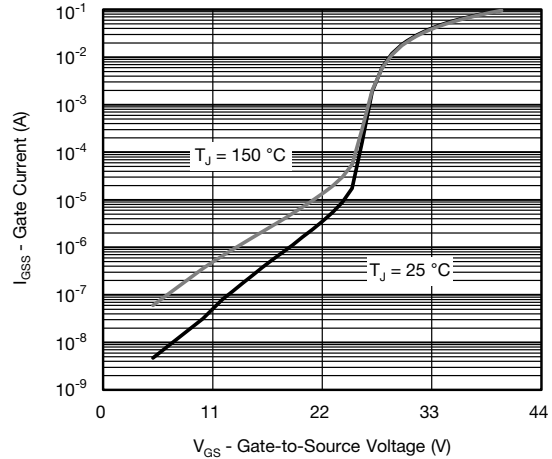
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



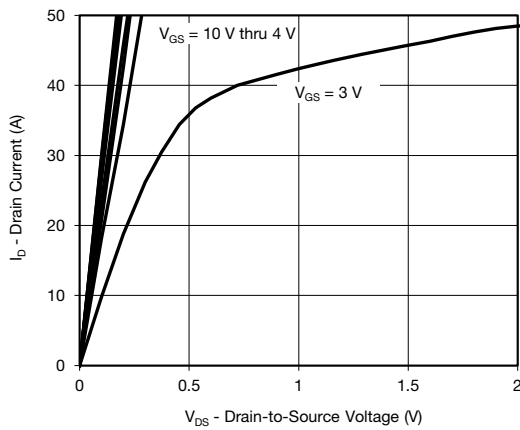
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



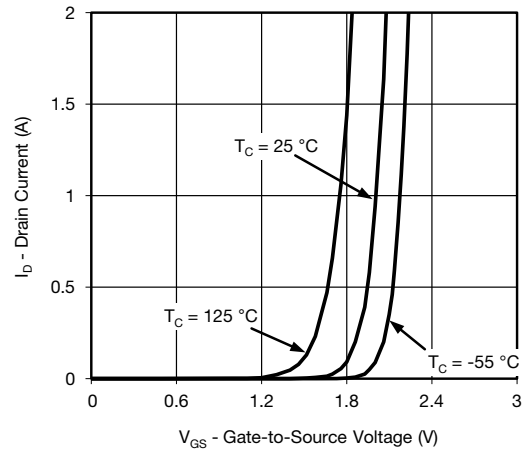
Gate Source Voltage vs. Gate Current



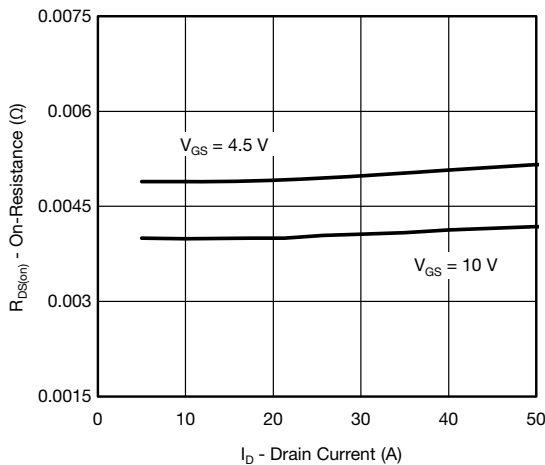
Gate Source Voltage vs. Gate Current



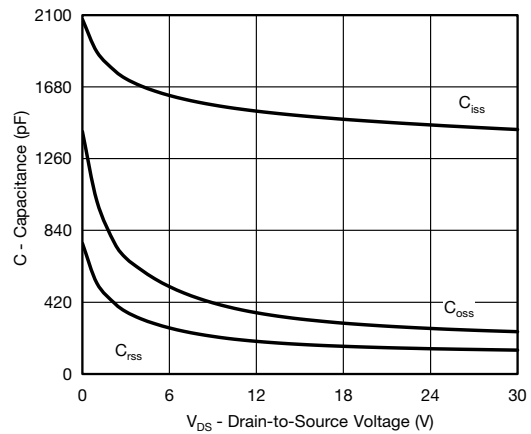
Output Characteristics



Transfer Characteristics



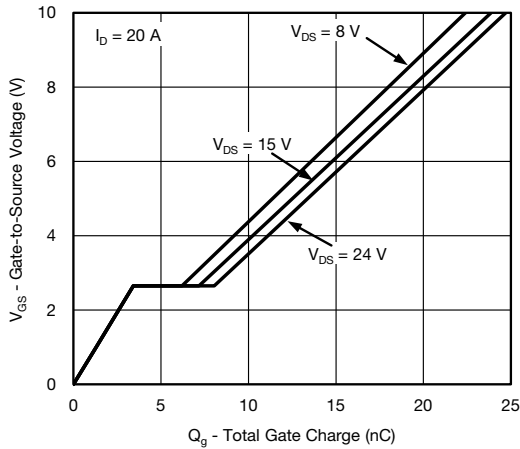
On-Resistance vs. Drain Current



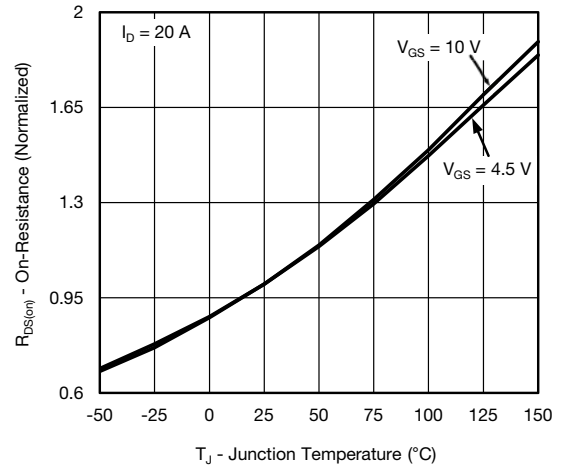
Capacitance



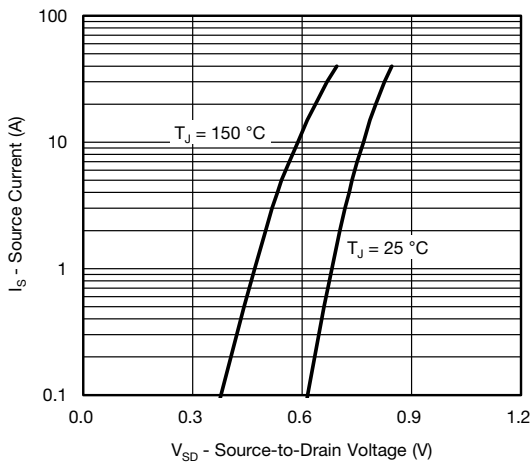
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



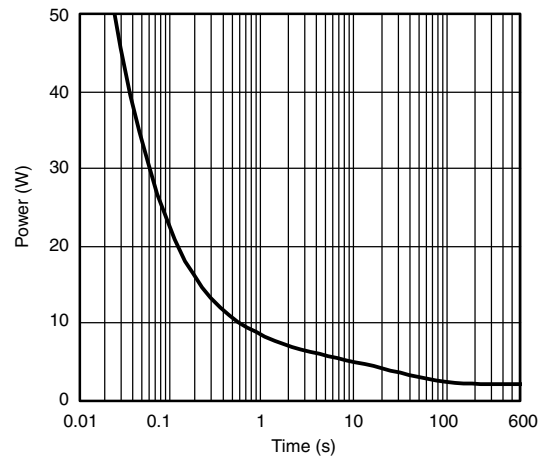
Gate Charge



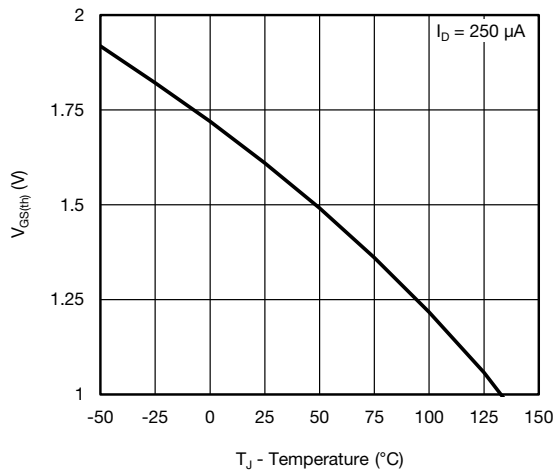
On-Resistance vs. Junction Temperature



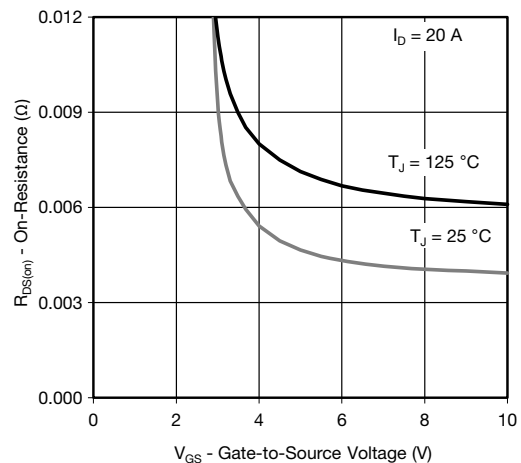
Source-Drain Diode Forward Voltage



Single Pulse Power (Junction-to-Ambient)

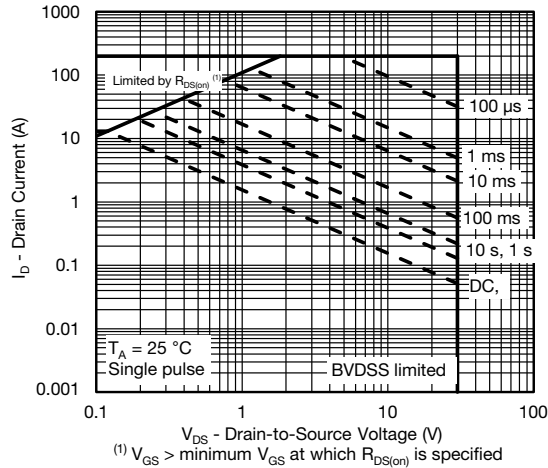


Threshold Voltage

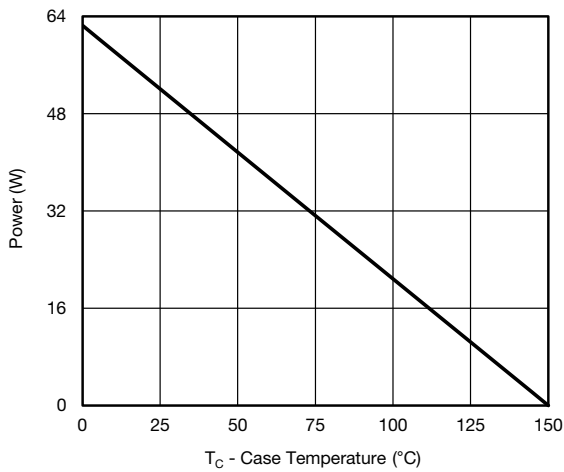


On-Resistance vs. Gate-to-Source Voltage

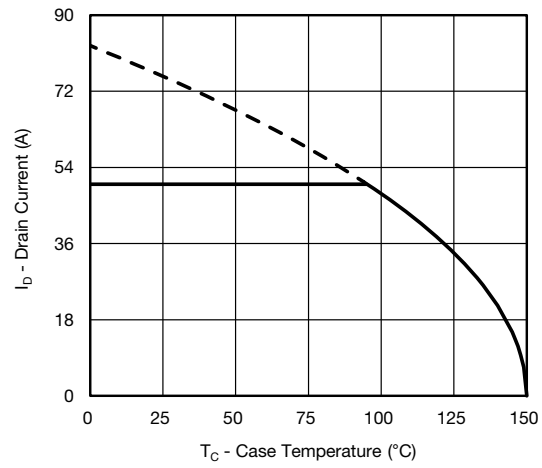
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Power Junction-to-Case



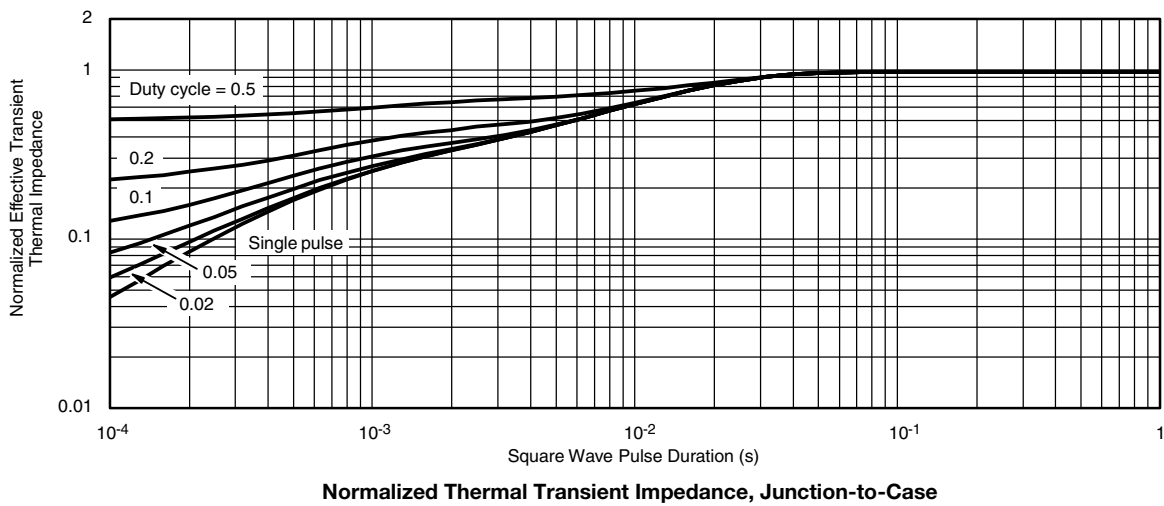
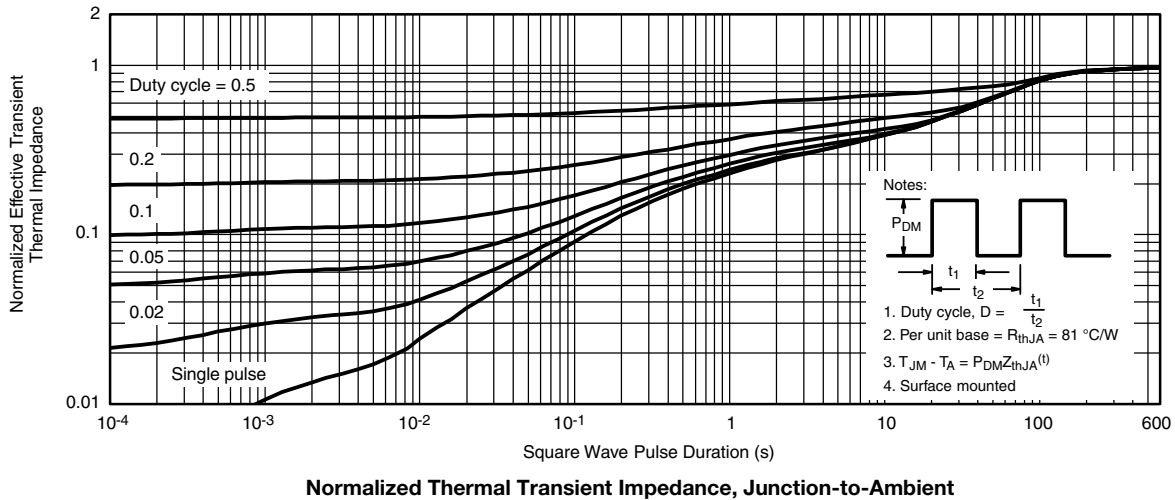
Current Derating ^a

Note

- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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