8-Channel, Triple 2-Channel Multiplexers

DESCRIPTION

The DG9451, and DG9453 are high precision single and dual supply CMOS analog multiplexers. DG9451 is an 8-channel multiplexer, and the DG9453 is a triple 2-channel multiplexer or triple SPDT.

Designed to operate from a +2.7 V to +12 V single supply or from a ± 2.5 V to ± 5 V dual supplies, the DG9451, and DG9453 are fully specified at +12 V, +5 V and ± 5 V. All control logic inputs have guaranteed 1.4 V high limit when operating from +5 V or ± 5 V supplies and 1.65 V when operating from a +12 V supply.

The DG9451, and DG9453 are precision multiplexers of low leakage, low charge injection, and low parasitic capacitance. They conduct equally well in both directions, offer rail to rail analog signal handling and can be used both as multiplexers as well as de-multiplexers.

The DG9451, and DG9453 operating temperature is specified from -40 °C to +85 °C and are available in 16 pin TSSOP and the ultra compact 1.8 mm x 2.6 mm miniQFN16 packages.

FEATURES

- +2.7 V to +12 V single supply operation
  ± 2.5 V to ± 5 V dual supply operation
- Fully specified at +12 V, +5 V, ± 5 V
- Low charge injection (< 0.5 pC typ.)
- High bandwidth: 270 MHz
- Low switch capacitance ($C_{s(off)}$ 1 pF typ.)
- Good isolation and crosstalk performance
  (typ. -44 dB at 100 MHz)
- MiniQFN16 package (1.8 mm x 2.6 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

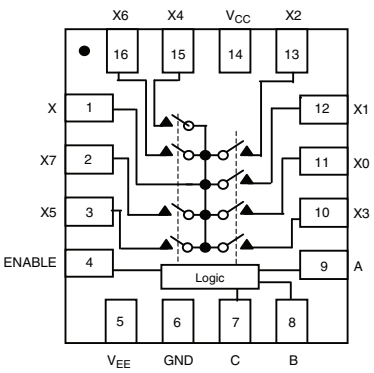
HALOGEN FREE

APPLICATIONS

- Data acquisition
- Medical and healthcare devices
- Control and automation equipments
- Test instruments
- Touch panels
- Consumer

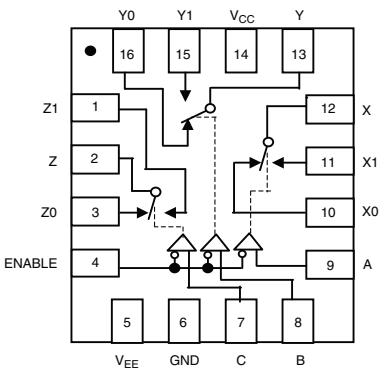
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG9451
mQFN-16

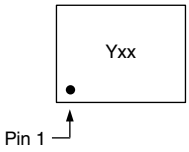


Top View

DG9453
mQFN-16



Top View



Device Marking: Yxx for DG9451
(miniQFN16) 4xx for DG9453

xx = Date/Lot Traceability Code

TRUTH TABLE

ENABLE INPUT	SELECT INPUTS			ON SWITCHES	
	C	B	A	DG9451	DG9453
H	X	X	X	All Switches Open	All Switches Open
L	L	L	L	X to X0	X to X0, Y to Y0, Z to Z0
L	L	L	H	X to X1	X to X1, Y to Y0, Z to Z0
L	L	H	L	X to X2	X to X0, Y to Y1, Z to Z0
L	L	H	H	X to X3	X to X1, Y to Y1, Z to Z0
L	H	L	L	X to X4	X to X0, Y to Y0, Z to Z1
L	H	L	H	X to X5	X to X1, Y to Y0, Z to Z1
L	H	H	L	X to X6	X to X0, Y to Y1, Z to Z1
L	H	H	H	X to X7	X to X1, Y to Y1, Z to Z1

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER
DG9451, DG9453		
-40 °C to +125 °C [a]	16-Pin miniQFN	DG9451EN-T1-E4
		DG9453EN-T1-E4

Note

a. -40 °C to +85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
V+ to V-		14	V
GND to V-		7	
Digital Inputs [a], V_S, V_D		(V-) -0.3 to (V+) +0.3 or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)		30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature		-65 to +150	°C
Power Dissipation [b]	16-Pin miniQFN [c, d]	525	mW
Thermal Resistance [b]	16-Pin miniQFN [d]	152	°C/W
Latch-up (per JESD78)		> 300	mA

Notes

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.6 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS FOR DUAL SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_{CC} = +5 V, V_{EE} = -5 V $V_{IN(A, B, C AND ENABLE)}$ = 1.4 V, 0.3 V [a]		TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
						MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch										
Analog Signal Range [e]	V_{ANALOG}			Full	-	-5	5	-5	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = -3 V, 0 V, +3 V		Room	66	-	100	-	100	Ω
				Full	-	-	125	-	118	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = ± 3 V		Room	3	-	6	-	6	
				Full	-	-	10	-	8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V		Room	10.2	-	16	-	16	
				Full	-	-	20	-	18	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V, V_D = ± 4.5 V, V_S = ∓ 4.5 V		Room	± 0.02	-1	1	-1	1	nA
				Full	-	-50	50	-5	5	
	$I_{D(off)}$			Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_S = V_D = ± 4.5 V		Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Digital Control										
$V_{IN(A, B, C and ENABLE)}$ Low	V_{IL}			Full	-	-	0.3	-	0.3	V
$V_{IN(A, B, C and ENABLE)}$ High	V_{IH}			Full	-	1.4	-	1.4	-	
Input Current, V_{IN} Low	I_{IL}	$V_{IN(A, B, C and ENABLE)}$ under test = 0.3 V		Full	0.01	-1	1	-1	1	µA
Input Current, V_{IN} High	I_{IH}	$V_{IN(A, B, C and ENABLE)}$ under test = 1.4 V		Full	0.01	-1	1	-1	1	
Input Capacitance [e]	C_{IN}	f = 1 MHz		Room	3.4	-	-	-	-	pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see figure 1, 2, 3		Room	66	-	180	-	180	ns
				Full	-	-	218	-	207	
Enable Turn-On Time	t_{ON}			Room	152	-	250	-	250	
				Full	-	-	295	-	282	
Enable Turn-Off Time	t_{OFF}			Room	60	-	125	-	125	
				Full	-	-	136	-	131	
Break-Before-Make Time Delay	t_D			Room	32	-	-	-	-	
				Full	-	-	13	-	13	
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 15 pF	f = 100 kHz	Room	< -90	-	-	-	-	dB
			f = 10 MHz	Room	-65	-	-	-	-	
			f = 100 MHz	Room	-44	-	-	-	-	
Channel-to-Channel Crosstalk [e]	X_{TALK}		f = 100 kHz	Room	< -90	-	-	-	-	
			f = 10 MHz	Room	-74	-	-	-	-	
			f = 100 MHz	Room	-44	-	-	-	-	
Bandwith, 3 dB	BW	R_L = 50 Ω	DG9451	Room	270	-	-	-	-	MHz
			DG9453	Room	525	-	-	-	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Room	0.20	-	-	-	-	pC
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG9451	Room	1	-	-	-	-	pF
			DG9453	Room	1	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG9451	Room	10	-	-	-	-	
			DG9453	Room	3	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG9451	Room	16	-	-	-	-	
			DG9453	Room	8	-	-	-	-	
Total Harmonic Distortion [e]	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω		Room	0.01	-	-	-	-	%
Power Supplies										
Power Supply Current	I+	V_{CC} = +5 V, V_{EE} = -5 V $V_{IN(A, B, C and ENABLE)}$ = 0 V or 5 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_{CC} = +5 V, V_{EE} = 0 V, $V_{IN(A, B, C AND ENABLE)}$ = 1.4 V, 0.3 V [a]		TEMP. [b]	TYP. [a]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
						MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch										
Analog Signal Range [e]	V_{ANALOG}			Full	-	0	5	0	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0 V, +3.5 V		Room	105	-	165	-	165	Ω
				Full	-	-	205	-	194	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = +3.5 V		Room	3.2	-	8	-	8	
				Full	-	-	13	-	10	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0 V, +3 V		Room	17	-	26	-	26	
				Full	-	-	30	-	28	
Switch Off Leakage Current	$I_{S(off)}$	V+ = +5.5 V, V- = 0 V, V_D = 1 V/4.5 V, V_S = 4.5 V/1 V		Room	± 0.02	-1	1	-1	1	nA
				Full	-	-50	50	-5	5	
	$I_{D(off)}$			Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = +5.5 V, V- = 0 V, V_D = V_S = 1 V/4.5 V		Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Digital Control										
$V_{IN(A, B, C and ENABLE)}$ Low	V_{IL}			Full	-	-	0.3	-	0.3	V
$V_{IN(A, B, C and ENABLE)}$ High	V_{IH}			Full	-	1.4	-	1.4		
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C and ENABLE)}$ under test = 0.3 V		Full	0.01	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C and ENABLE)}$ under test = 1.4 V		Full	0.01	-1	1	-1	1	
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF, See Figure 1, 2, 3		Room	79	-	205	-	205	ns
				Full	-	-	295	-	285	
Enable Turn-On Time	t_{ON}			Room	220	-	335	-	335	
				Full	-	-	403	-	393	
Enable Turn-Off Time	t_{OFF}			Room	93	-	150	-	150	
				Full	-	-	173	-	163	
Break-Before-Make Time Delay	t_D			Room	36	-	-	-	-	
				Full	-	-	20	-	20	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Full	0.81	-	-	-	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 15 pF, f = 100 kHz		Room	< -90	-	-	-	-	dB
Channel-to-Channel Crosstalk [e]	X_{TALK}			Room	< -90	-	-	-	-	
Dynamic Characteristics										
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG9451	Room	1	-	-	-	-	pF
			DG9453	Room	1	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG9451	Room	11	-	-	-	-	
			DG9453	Room	3	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG9451	Room	17	-	-	-	-	
			DG9453	Room	9	-	-	-	-	
Power Supplies										
Power Supply Current	I+	$V_{IN(A, B, C and ENABLE)}$ = 0 V or 5 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

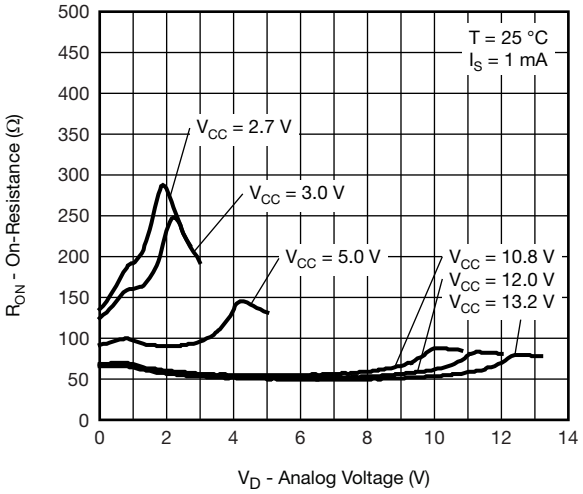
SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_{CC} = +12 V, V_{EE} = 0 V V = 1.6 V, 0.5 V [a]		TEMP. [b]	TYP. [c]	-40 °C to +125 °C MAX. [d]	-40 °C to +125 °C MIN. [d]	-40 °C to +85 °C MIN. d	-40 °C to +85 °C MAX. D	UNIT
Analog Switch										
Analog Signal Range [e]	V_{ANALOG}			Full	-	0	12	0	12	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0.7 V, 6 V, 11.3 V		Room	68	-	105	-	105	Ω
				Full	-	-	143	-	137	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = +0.7 V		Room	4	-	7	-	7	
				Full	-	-	10	-	8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0.7 V, +11.3 V		Room	32	-	45	-	45	
				Full	-	-	49	-	47	
Switch Off Leakage Current	$I_{S(off)}$	V+ = +12 V, V- = 0 V V_D = 1 V/11 V, V_S = 11 V/1 V		Room	± 0.02	-1	1	-1	1	nA
				Full	-	-50	50	-5	5	
	$I_{D(off)}$			Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = +12 V, V- = 0 V V_D = V_S = 1 V/11 V		Room	± 0.02	-1	1	-1	1	
				Full	-	-50	50	-5	5	
Digital Control										
$V_{IN(A, B, C and ENABLE)}$ Low	V_{IL}			Full	-	-	0.5	-	0.5	V
$V_{IN(A, B, C and ENABLE)}$ High	V_{IH}			Full	-	1.6	-	1.6	-	
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C and ENABLE)}$ under test = 0.5 V		Full	0.01	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C and ENABLE)}$ under test = 1.6 V		Full	0.01	-1	1	-1	1	
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see figure 1, 2, 3		Room	55	-	135	-	135	ns
				Full	-	-	166	-	155	
Enable Turn-On Time	t_{ON}			Room	106	-	185	-	185	
				Full	-	-	219	-	205	
Enable Turn-Off Time	t_{OFF}			Room	65	-	130	-	130	
				Full	-	-	144	-	137	
Break-Before-Make Time Delay	t_D			Room	30	-	-	-	-	
				Full	-	-	12	-	12	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Room	0.79	-	-	-	-	pC
Dynamic Characteristics										
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 15 pF f = 100 kHz		Room	< -90	-	-	-	-	dB
Channel-to-Channel Crosstalk [e]	X_{TALK}			Room	< -90	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	DG9451	Room	1	-	-	-	-	pF
			DG9453	Room	1	-	-	-	-	
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz	DG9451	Room	9	-	-	-	-	
			DG9453	Room	3	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$	f = 1 MHz	DG9451	Room	15	-	-	-	-	
			DG9453	Room	8	-	-	-	-	
Power Supplies										
Power Supply Current	I+	$V_{IN(A, B, C and ENABLE)}$ = 0 V or 12 V		Room	0.05	-	1	-	1	µA
				Full	-	-	10	-	10	
Negative Supply Current	I-			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	
Ground Current	I_{GND}			Room	-0.05	-1	-	-1	-	
				Full	-	-10	-	-10	-	

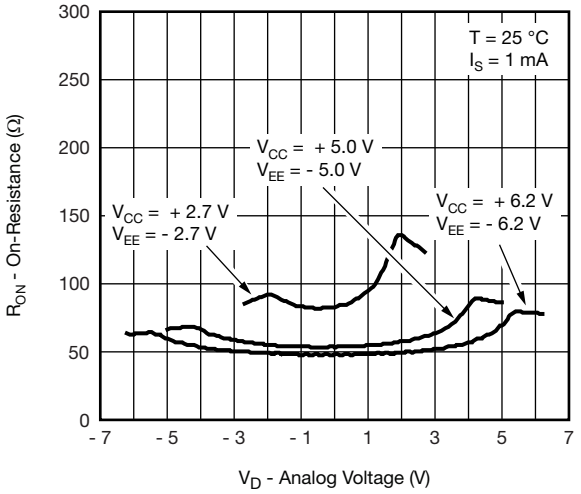
Notes
a. V_{IN} = input voltage to perform proper function.
b. Room -25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

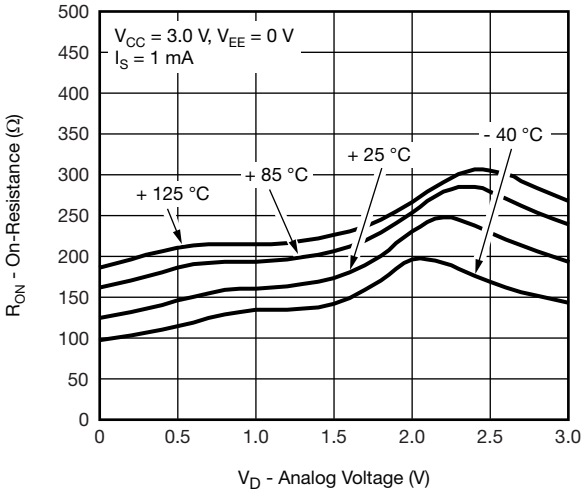
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



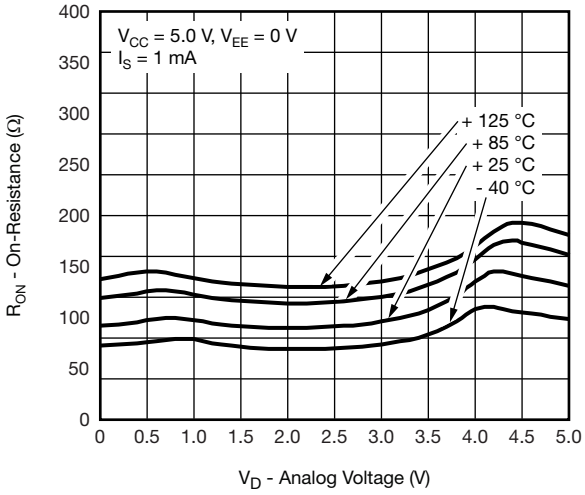
On-Resistance vs. V_D and Signal Supply Voltage



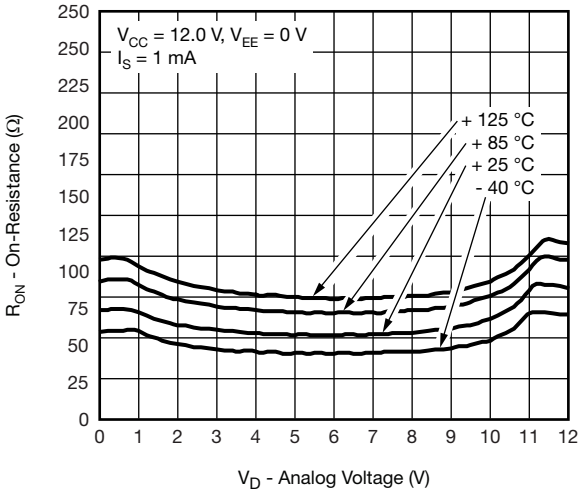
On-Resistance vs. Analog Voltage and Temperature



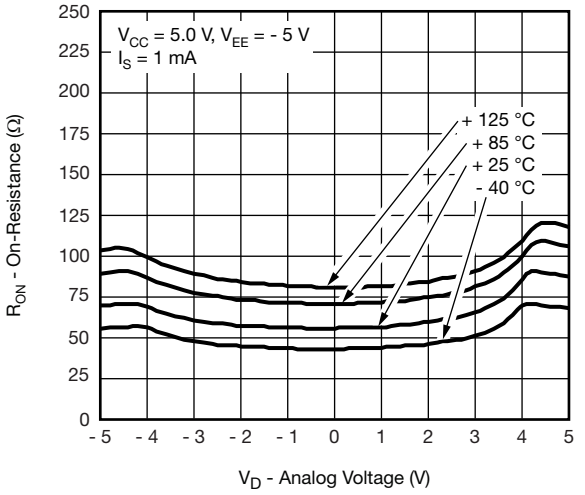
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

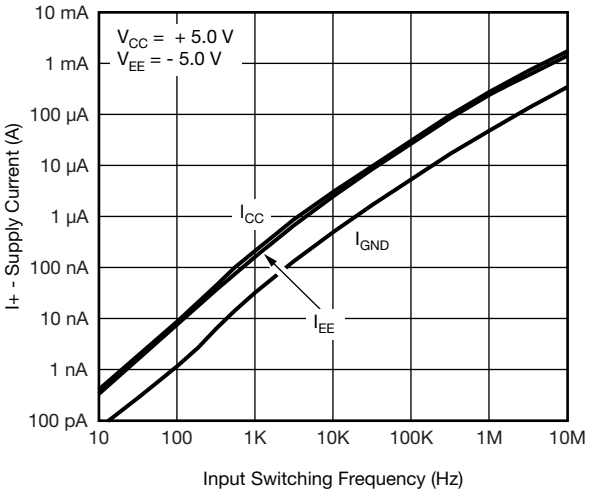


On-Resistance vs. Analog Voltage and Temperature

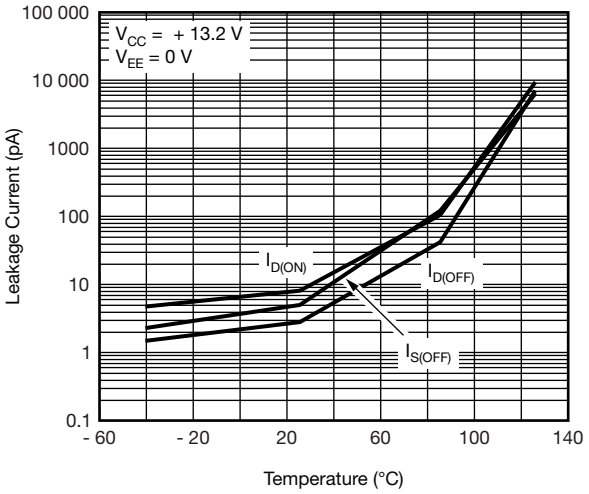


On-Resistance vs. Analog Voltage and Temperature

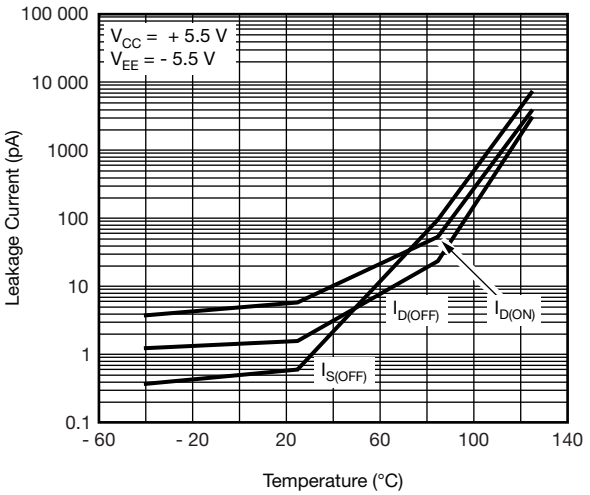
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



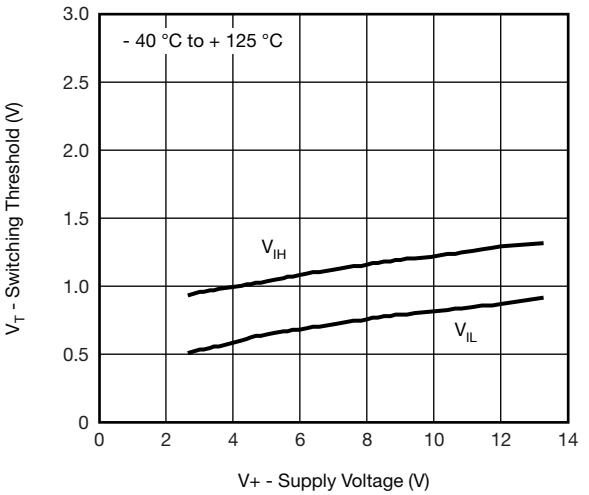
Supply Current vs. Input Switching Frequency



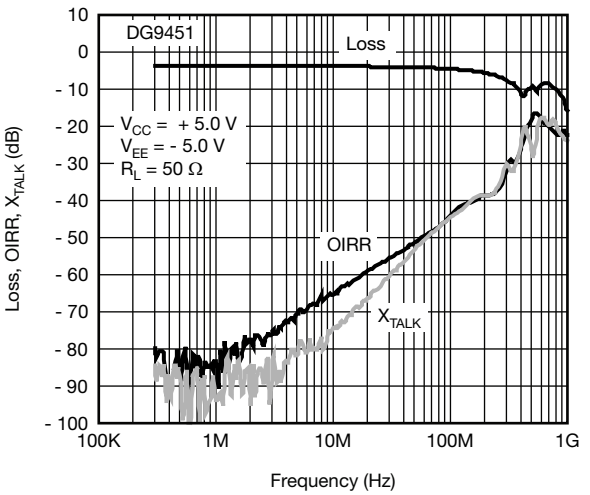
Leakage Current vs. Temperature



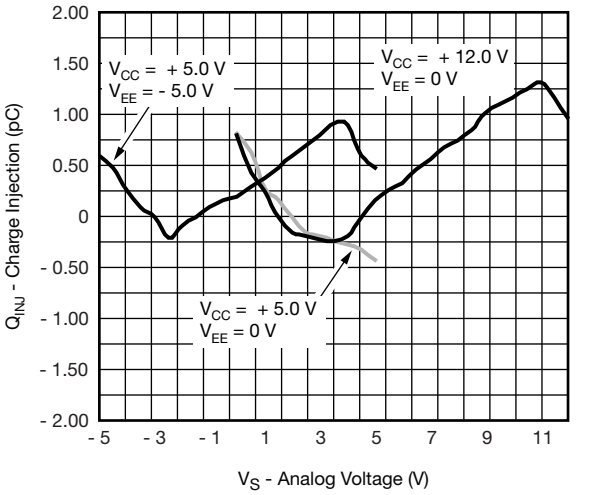
Leakage Current vs. Temperature



Switching Threshold vs. Supply Voltage

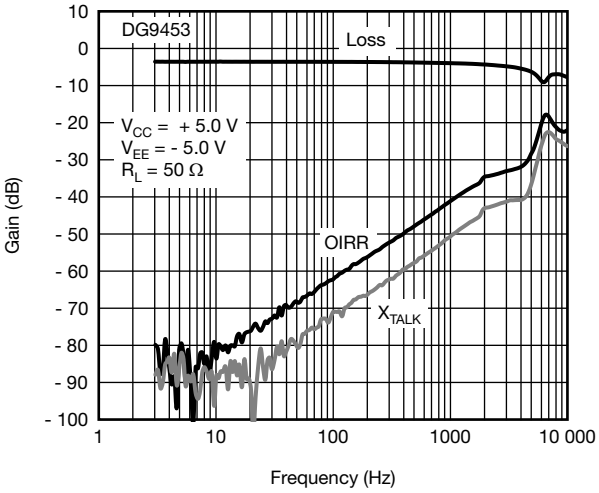


DG9451 Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

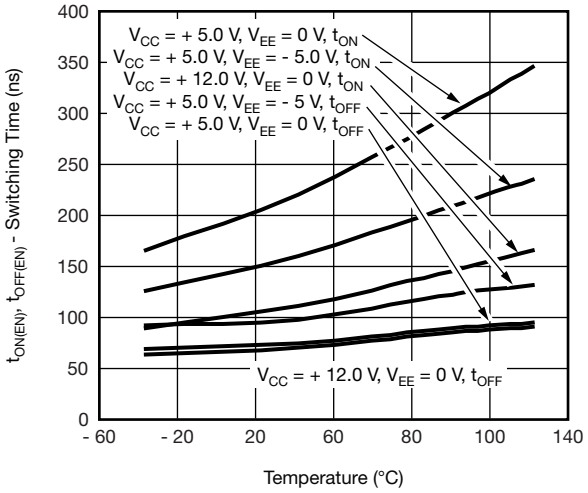


DG9451 Charge Injection vs. Analog Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Frequency Response



Switching Time vs. Temperature

TEST CIRCUITS

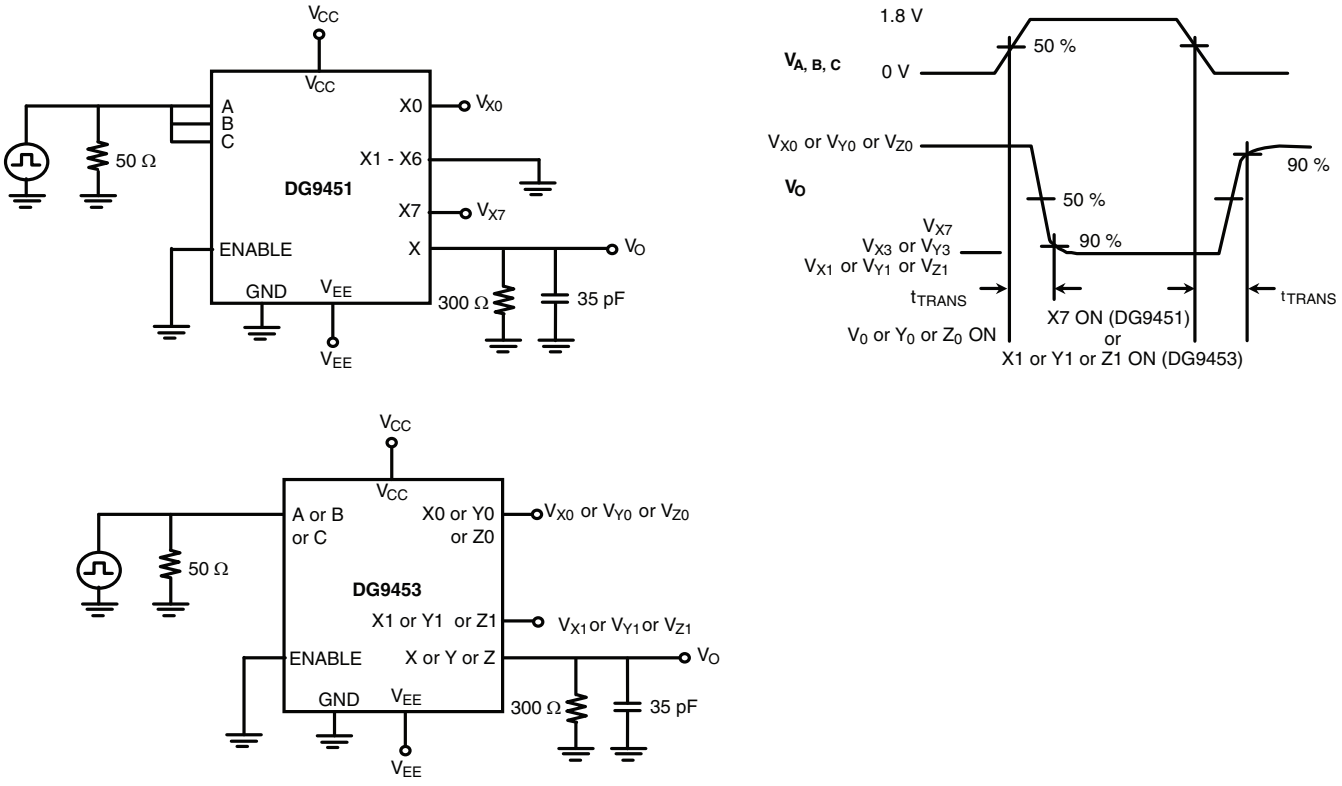
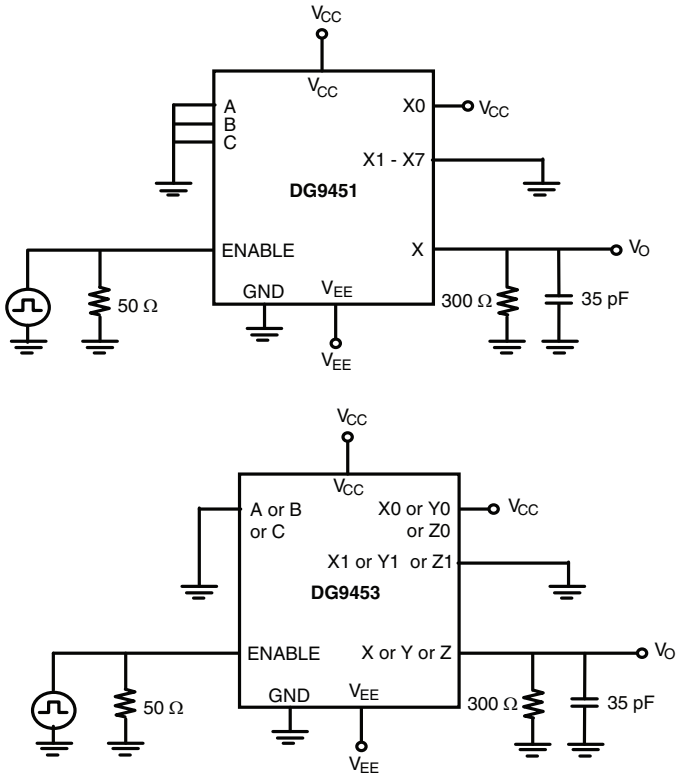


Fig. 1 - Transition Time

TEST CIRCUITS



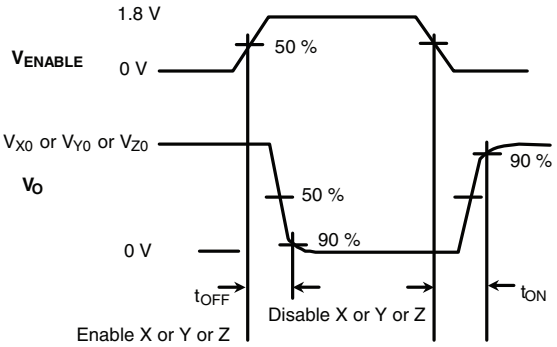
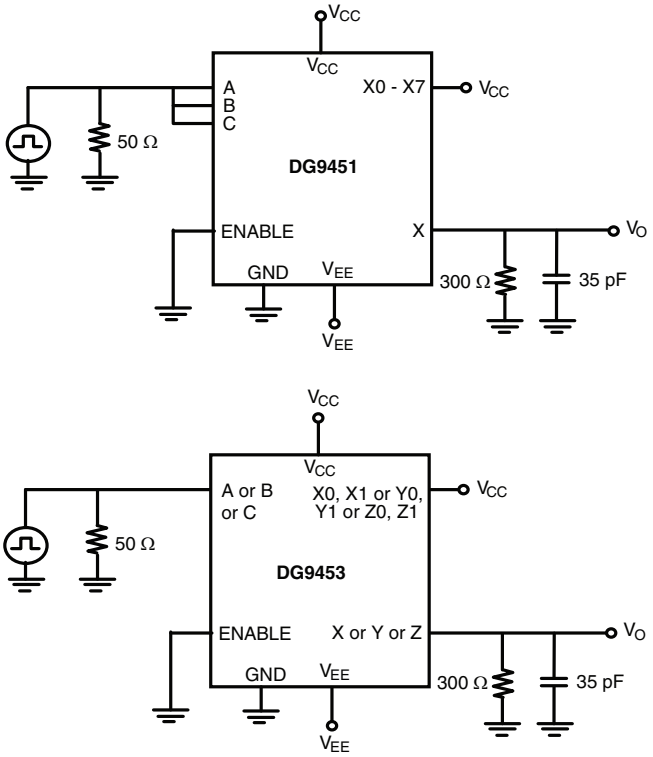


Fig. 2 - Enable Switching Time



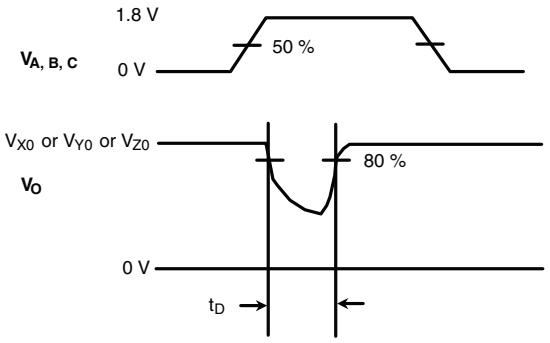
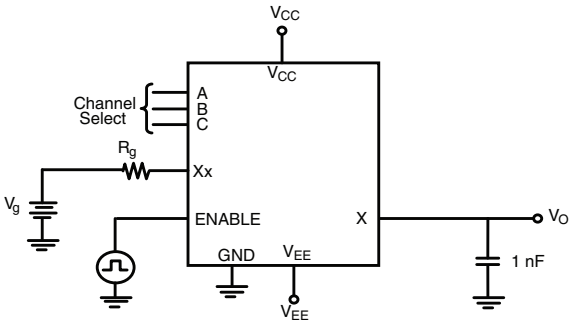


Fig. 3 - Break-Before-Make

TEST CIRCUITS



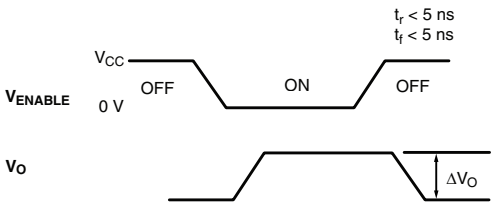


Fig. 4 - Charge Injection

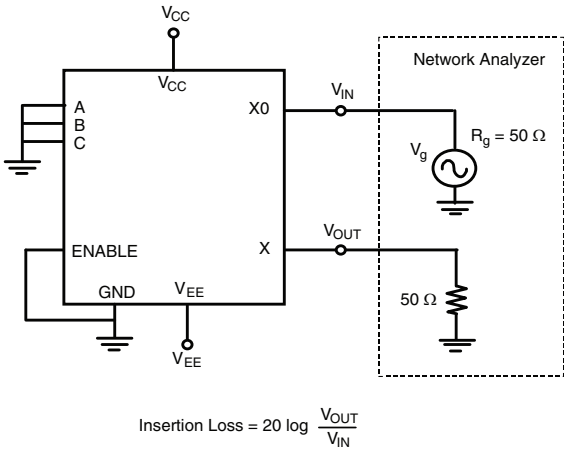


Fig. 5 - Insertion Loss

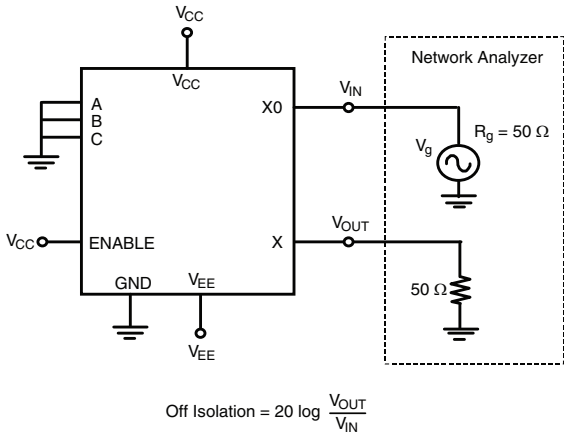


Fig. 7 - Off Isolation

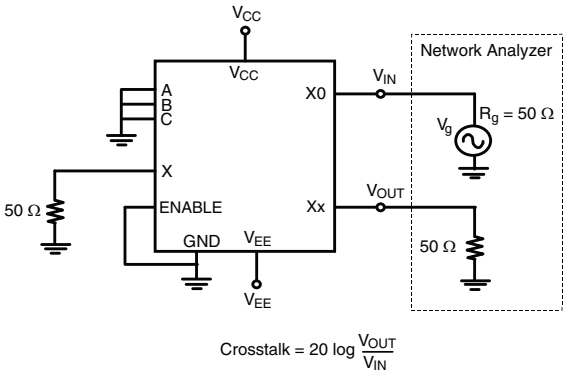


Fig. 6 - Crosstalk

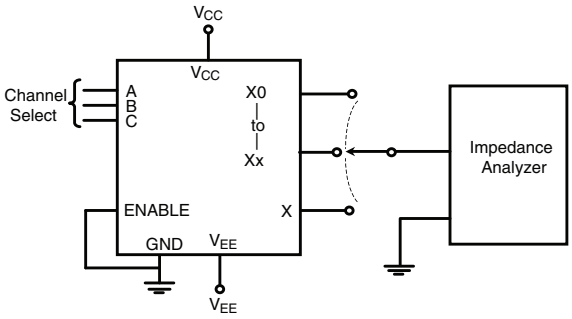


Fig. 8 - Source, Drain Capacitance

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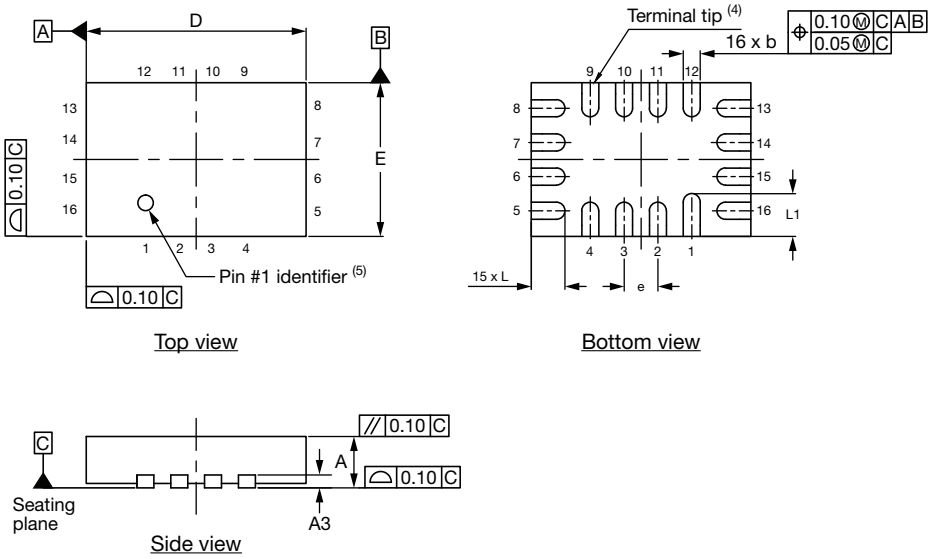
Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

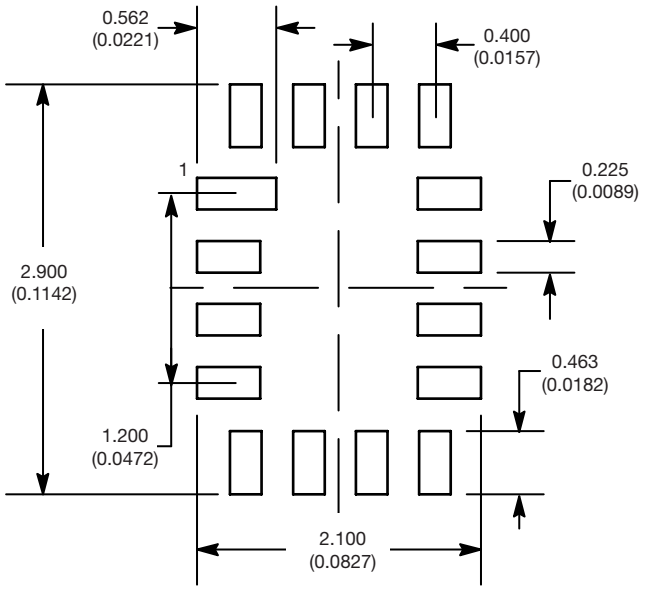
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

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