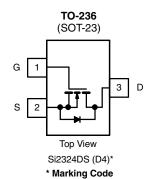




N-Channel 100 V (D-S) MOSFET

MOSFET PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)		
	0.234 at V _{GS} = 10 V	2.3			
100	0.267 at V _{GS} = 6 V	2.1	2.9 nC		
	0.278 at V _{GS} = 4.5 V	1.7			



Ordering Information:

Si2324DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g Tested 100 % UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



HALOGEN FREE

APPLICATIONS

- DC/DC Converters
- Load Switch
- LED Backlighting in LCD TVs

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	100	V		
Gate-Source Voltage	V _{GS}	± 20	v		
	T _C = 25 °C		2.3		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C	ı_	1.8		
Continuous Diam Current (1) = 130 °C)	T _A = 25 °C	I _D	1.6 ^{b, c}		
	T _A = 70 °C		1.3 ^{b, c}	A	
Pulsed Drain Current (t = 300 μs)		I _{DM}	5		
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	2.1		
Continuous Cource-Diam Diode Current	T _A = 25 °C	I _S	1.0 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	5		
Single Pulse Avalanche Energy	L = 0.111111	E _{AS}	1.25	mJ	
	T _C = 25 °C		2.5		
Maximum Power Dissipation	T _C = 70 °C	P _D	1.6	w	
Maximum Fower Dissipation	T _A = 25 °C	' D	1.25 ^{b, c}	VV	
	T _A = 70 °C		0.8 ^{b, c}		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, d}	≤ 5 s	R _{thJA}	75	100	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	40	50	0/11		

Notes:

- a. Based on T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 166 °C/W.



MOSFET SPECIFICATIONS	$(T_J = 25 ^{\circ}C)$, unless otherwise noted)					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0 \text{ V, } I_{D} = 250 \mu\text{A}$	100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	/ _{DS} /T _J		105		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.2		IIIV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.2		2.8	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zoro Cata Valtago Drain Current	I _{DSS}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$	- 1		- 1	μА	
Zero Gate Voltage Drain Current		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	5			Α	
		$V_{GS} = 10 \text{ V}, I_D = 1.5 \text{ A}$		0.195	0.234		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 6 V, I _D = 1 A		0.222	0.267	Ω	
		$V_{GS} = 4.5 \text{ V}, I_D = 0.5 \text{ A}$		0.231	0.278		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 20 \text{ V}, I_D = 1.5 \text{ A}$		2.0		S	
Dynamic ^b							
Input Capacitance	C _{iss}			190		pF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		22			
Reverse Transfer Capacitance	C _{rss}			13			
<u> </u>		$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 1.6 \text{ A}$		5.2	10.4	nC	
Total Gate Charge	Q_g			2.9	5.8		
Gate-Source Charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 1.6 A		0.75			
Gate-Drain Charge	Q_{gd}			1.4		1	
Gate Resistance	R_g	f = 1 MHz	0.3	1.4	2.8	Ω	
Turn-On Delay Time	t _{d(on)}			30	45		
Rise Time	t _r	V_{DD} = 50 V, R_L = 39 Ω		26	39	- - -	
Turn-Off Delay Time	t _{d(off)}	$I_D = 1.3 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		17	26		
Fall Time	t _f			12	20		
Turn-On Delay Time	t _{d(on)}			6	12	ns	
Rise Time	t _r	$V_{DD} = 50 \text{ V}, R_1 = 39 \Omega$		10	20	_	
Turn-Off Delay Time	t _{d(off)}	$I_D = 1.3 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		10	20		
Fall Time	t _f	-		6	12	1	
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 2.1		
Pulse Diode Forward Current ^a	I _{SM}				- 20	A	
Body Diode Voltage	V _{SD}	I _S = 1.3 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	-		22	33	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			21	32	nC	
Reverse Recovery Fall Time	t _a	$I_F = 1.3 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		16			
Reverse Recovery Rise Time	t _b			6		ns	
	U					1	

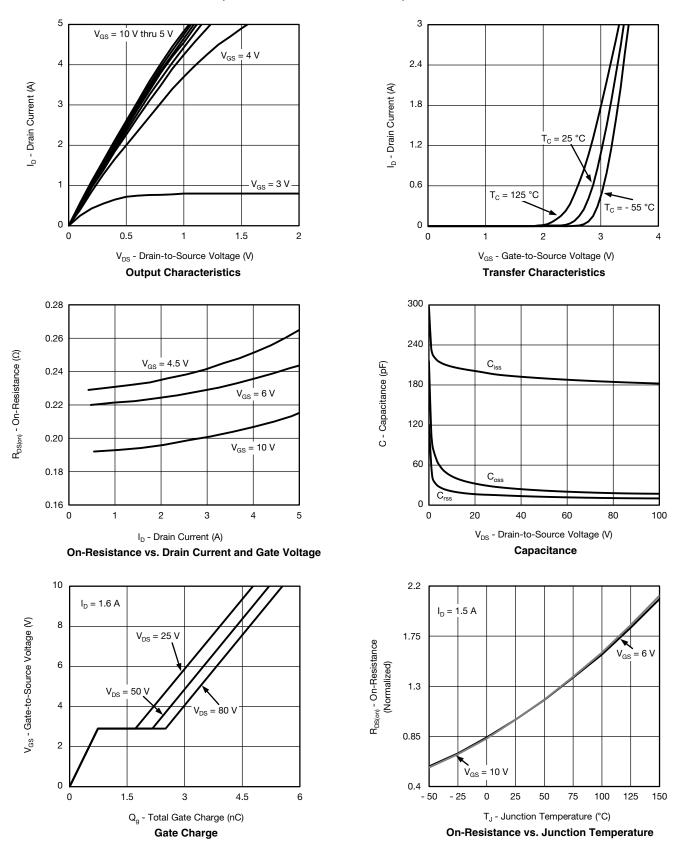
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

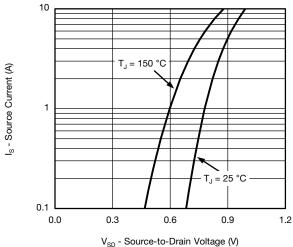


Document Number: 67691 S12-1140-Rev. B, 21-May-12

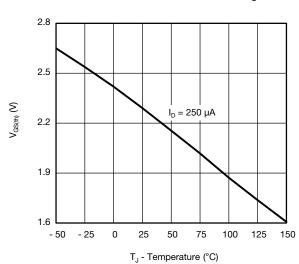
For technical questions, contact: pmostechsupport@vishay.com

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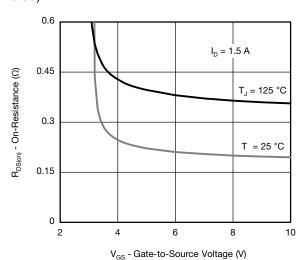
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



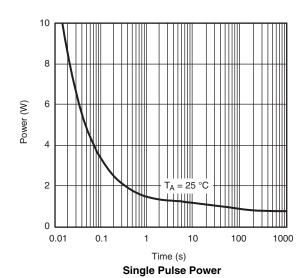


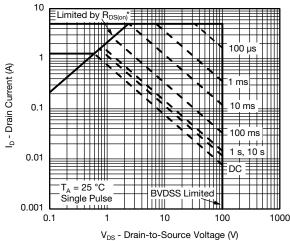


Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



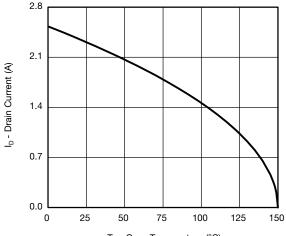


 $^{*}V_{GS}$ > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

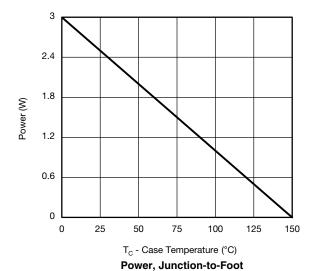


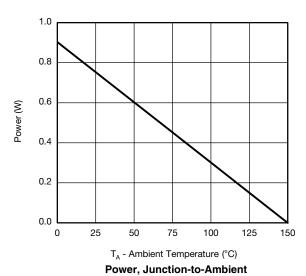
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



T_C - Case Temperature (°C)

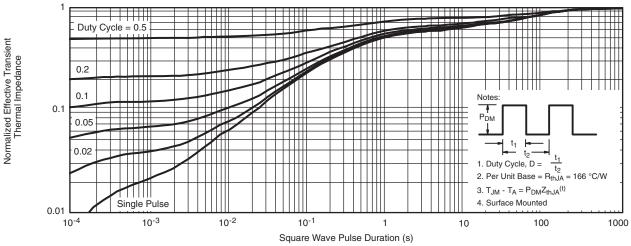
Current Derating*



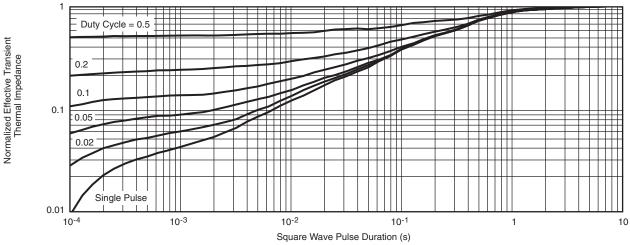


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



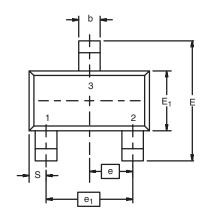
Normalized Thermal Transient Impedance, Junction-to-Ambient



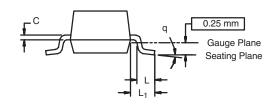
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?67691.

SOT-23 (TO-236): 3-LEAD







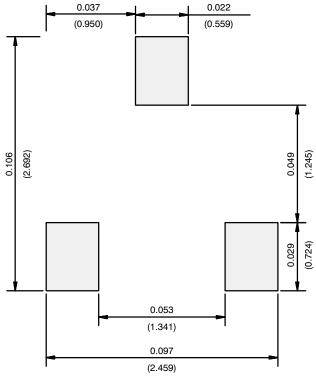
Dim	MILLIMETERS		INCHES		
	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A ₁	0.01	0.10	0.0004	0.004	
A ₂	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E ₁	1.20	1.40	0.047	0.055	
е	0.95	BSC	0.0374 Ref		
e ₁	1.90	BSC	0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L ₁	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	
ECN: S-03946-Rev. K. 09-	Jul-01				

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01



RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE

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