DMCB SERIES DIE
N-Channel Lateral DMOS FETs

The DMCB Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance of ultra-fast switching speeds. The DMCB Series also features an integrated zener diode designed to protect the gate from electrical "Spikes" or overstress.

DMCB1CHP*	DMCB2CHP*
SD210DE SD214DE	SD211DE SD215DE SST211 SST215
*Meets or exceeds specification for all part numbers listed below	

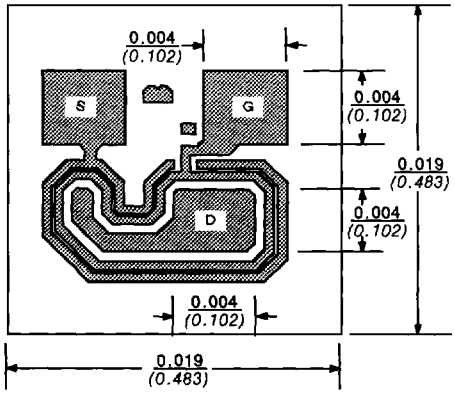
For additional design information please consult the typical performance curves DMCA/B.

DESIGNED FOR:

- Ultra-High Speed Switching
- High Gain Amplifiers

FEATURES

- < 1 ns Switching t_{ON}
  Ultra-Low Capacitance C_G < 3.5 pF
- g_{fs} (gain) > 10000 μmhos



Nominal Thickness
0.009 inches
0.228 mm

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		DMCB1CHP	DMCB2CHP	
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	±40	-30/25	V
Gate-Substrate Voltage	V_{GB}	±40	-0.3/25	
Drain-Source Voltage	V_{DS}	30		
Source-Drain Voltage	V_{SD}	10		
Drain-Substrate Voltage	V_{DB}	30		
Source-Substrate Voltage	V_{SB}	15		
Drain Current	I_D	50		mA
Storage Temperature	T_{stg}	-65 to 200		°C

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DMCB SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS					
					DMCB1CHP		DMCB2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30		30		V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	20		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	25		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA Drain OPEN		35	25		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4					nA
			$V_{DS} = 20$ V	0.9					
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{DS} = 10$ V	0.5					
			$V_{DS} = 20$ V	1					
Gate Leakage	I_{GBS}	$V_{DB} = V_{GS} = 0$ V, $V_{GB} = 30$ V		10^{-5}					µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA $V_{SB} = 0$ V		0.7	0.5	2	0.5	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58					Ω
			$V_{GS} = 10$ V	38					
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
			$V_{GS} = 25$ V	24					
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V		11					mS
Output Conductance	g_{os}	$I_D = 20$ mA, $f = 1$ kHz		0.9					
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz $V_{GS} = V_{BS} = -15$ V		2.5					pF
Drain-Node Capacitance	$C_{(GD+DB)}$			1.1					
Source-Node Capacitance	$C_{(GS+SB)}$			3.7					
Reverse Transfer Capacitance	C_{rss}			0.2					
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω $V_{IN} = 0$ to 5 V		0.5					ns
	t_r			0.8					
Turn-Off Time	$t_{d(OFF)}$			2					
	t_f			6					

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.