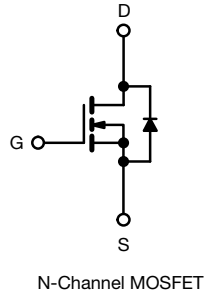
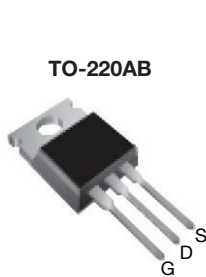


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	200
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0$ V   0.18
$Q_g$ max. (nC)	66
$Q_{gs}$ (nC)	9.0
$Q_{gd}$ (nC)	38
Configuration	Single



### FEATURES

- Dynamic  $dV/dt$  rating
- Repetitive avalanche rated
- Logic-level gate drive
- $R_{DS(on)}$  specified at  $V_{GS} = 4$  V and 5 V
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### DESCRIPTION

Third generation power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

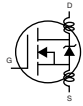
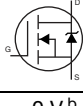
ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRL640PbF
	SiHL640-E3
SnPb	IRL640
	SiHL640

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	200	V	
Gate-Source Voltage		$V_{GS}$	$\pm 10$		
Continuous Drain Current	$V_{GS}$ at 5.0 V	$I_D$	$T_C = 25$ °C	17	A
			$T_C = 100$ °C	11	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	68		
Linear Derating Factor			1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	580	mJ	
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	10	A	
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	13	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	125	W	
Peak Diode Recovery $dV/dt$ <sup>c</sup>		$dV/dt$	5.0	V/ns	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	°C	
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 3.0$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 17$  A (see fig. 12).
- $I_{SD} \leq 17$  A,  $dI/dt \leq 150$  A/ms,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.27	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}, I_D = 10\text{ A}^b$	-	-	0.18	$\Omega$
		$V_{GS} = 4.0\text{ V}, I_D = 8.5\text{ A}^b$	-	-	0.27	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 10\text{ A}^b$	16	-	-	S
Dynamic						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	1800	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	400	-	
Reverse Transfer Capacitance	$C_{rss}$		-	120	-	
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}, I_D = 17\text{ A}, V_{DS} = 160\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	66	nC
Gate-Source Charge	$Q_{gs}$		-	-	9.0	
Gate-Drain Charge	$Q_{gd}$		-	-	38	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}, I_D = 17\text{ A}, R_g = 4.6\text{ }\Omega, R_D = 5.7\text{ }\Omega, \text{ see fig. 10}^b$	-	8.0	-	ns
Rise Time	$t_r$		-	83	-	
Turn-Off Delay Time	$t_{d(off)}$		-	44	-	
Fall Time	$t_f$		-	52	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{ open drain}$	0.3	-	1.2	$\Omega$
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	17	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	68	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 17\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	310	470	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.2	4.8	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

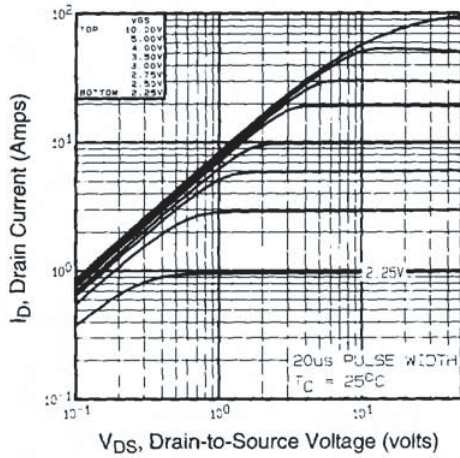


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

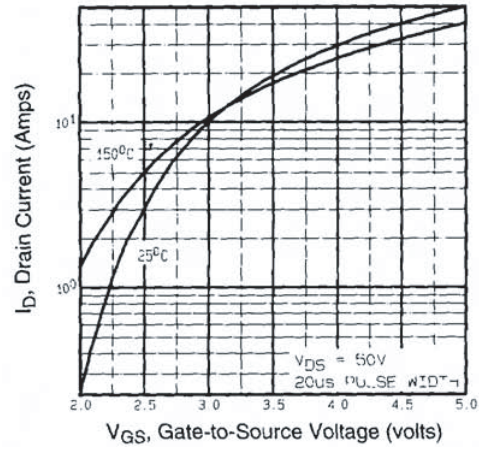


Fig. 3 - Typical Transfer Characteristics

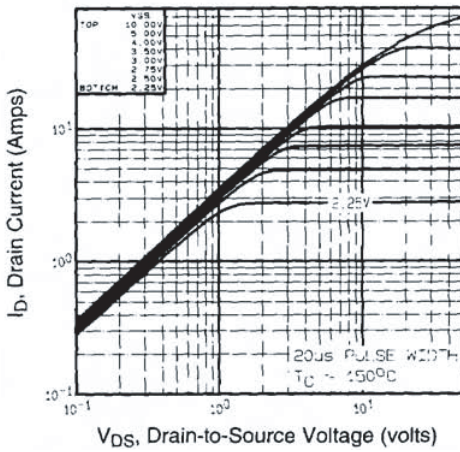


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

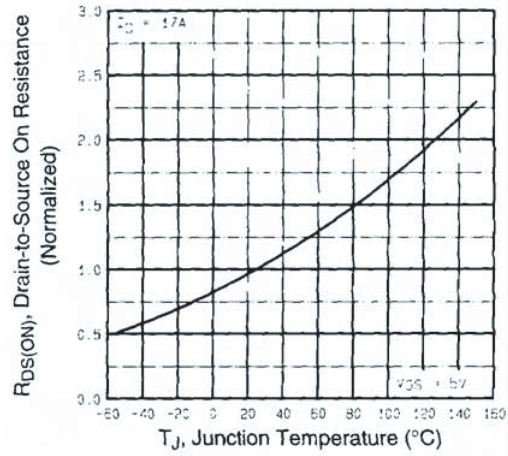


Fig. 4 - Normalized On-Resistance vs. Temperature

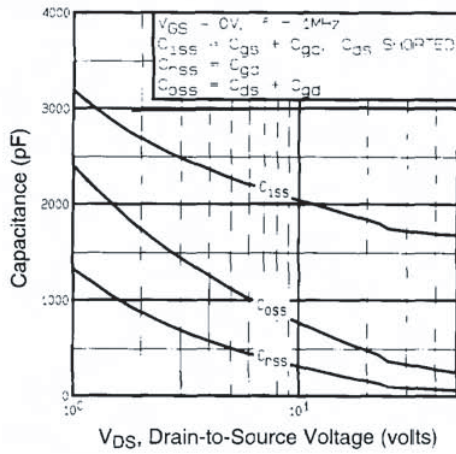


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

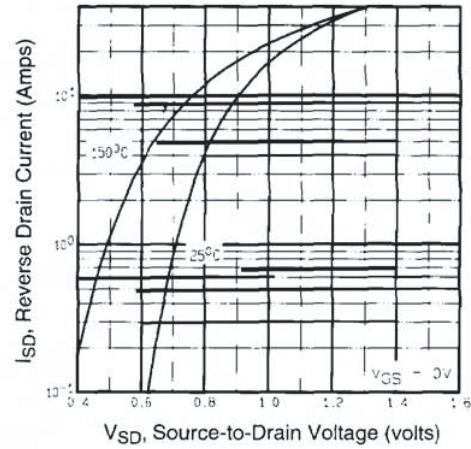


Fig. 7 - Typical Source-Drain Diode Forward Voltage

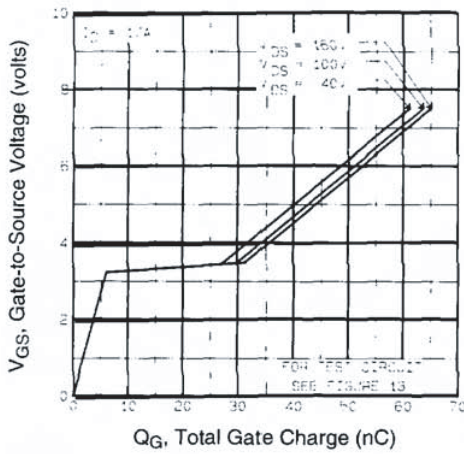


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

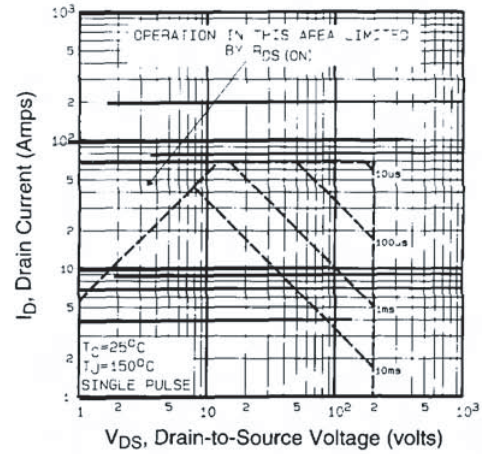


Fig. 8 - Maximum Safe Operating Area



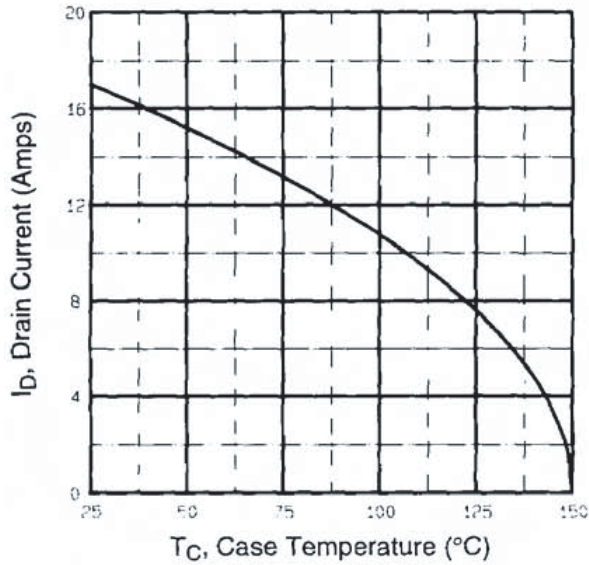


Fig. 9 - Maximum Drain Current vs. Case Temperature

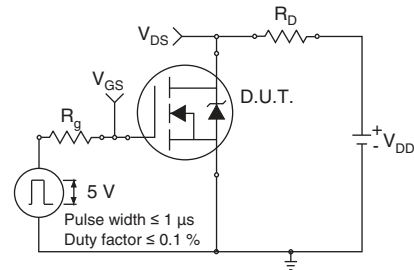


Fig. 10a - Switching Time Test Circuit

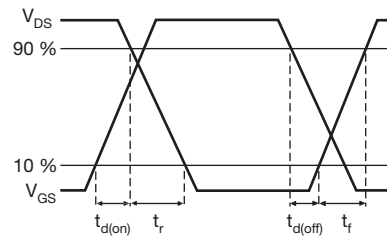


Fig. 10b - Switching Time Waveforms

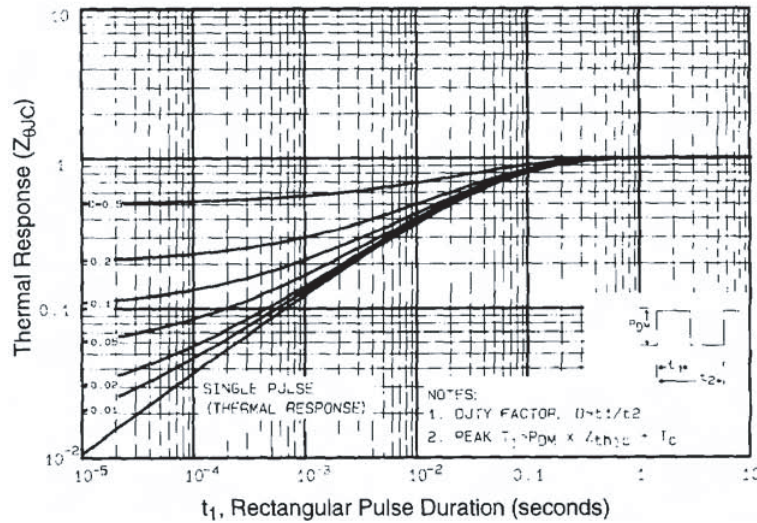


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

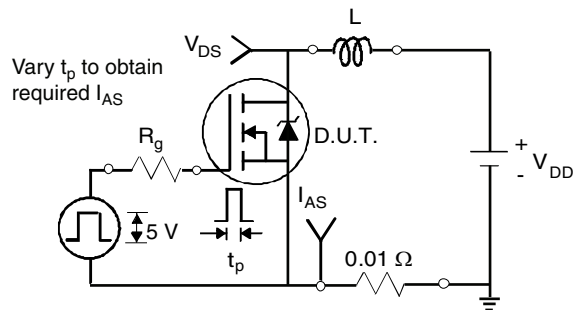


Fig. 12a - Unclamped Inductive Test Circuit

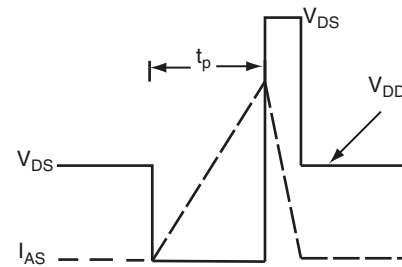


Fig. 12b - Unclamped Inductive Waveforms

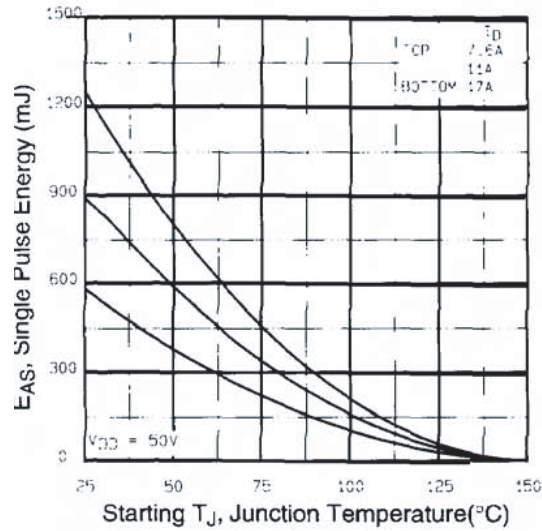


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

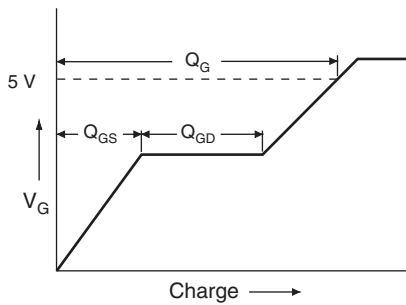


Fig. 13a - Basic Gate Charge Waveform

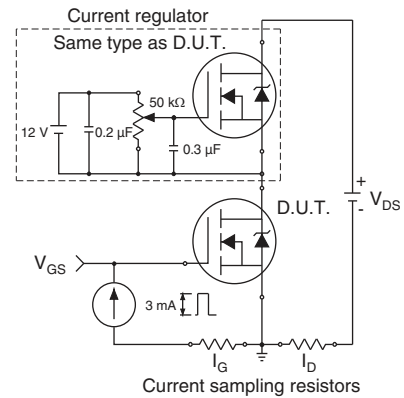
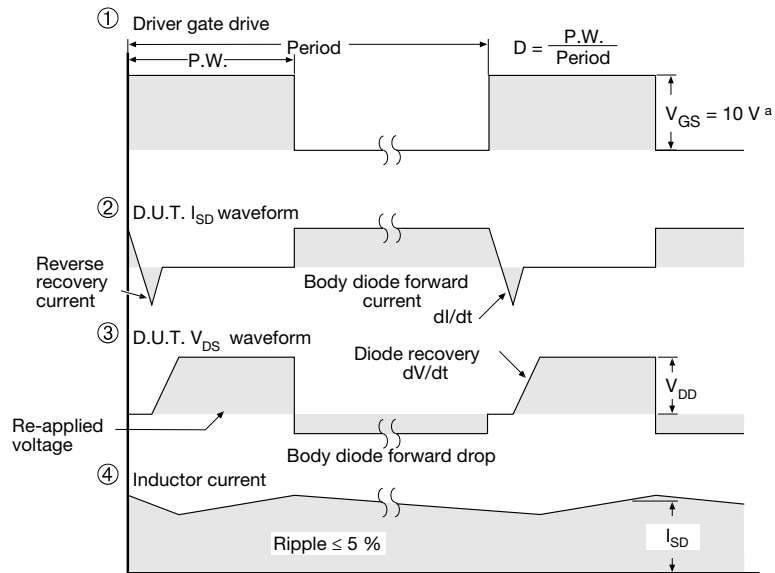
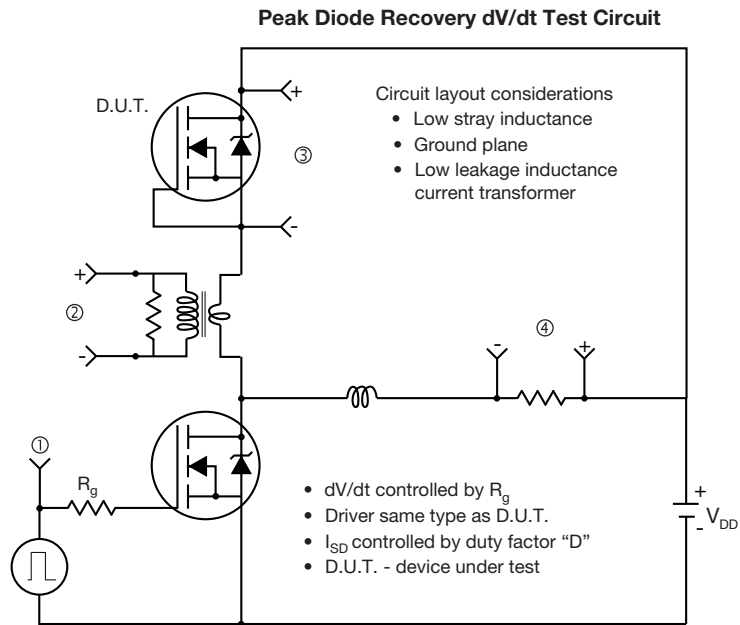


Fig. 13b - Gate Charge Test Circuit

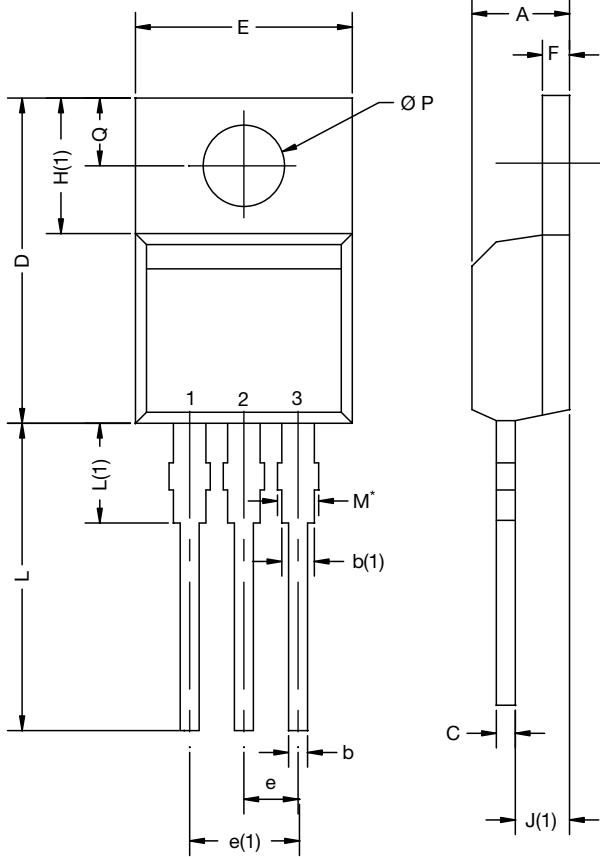


**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91305](http://www.vishay.com/ppg?91305).

## TO-220-1

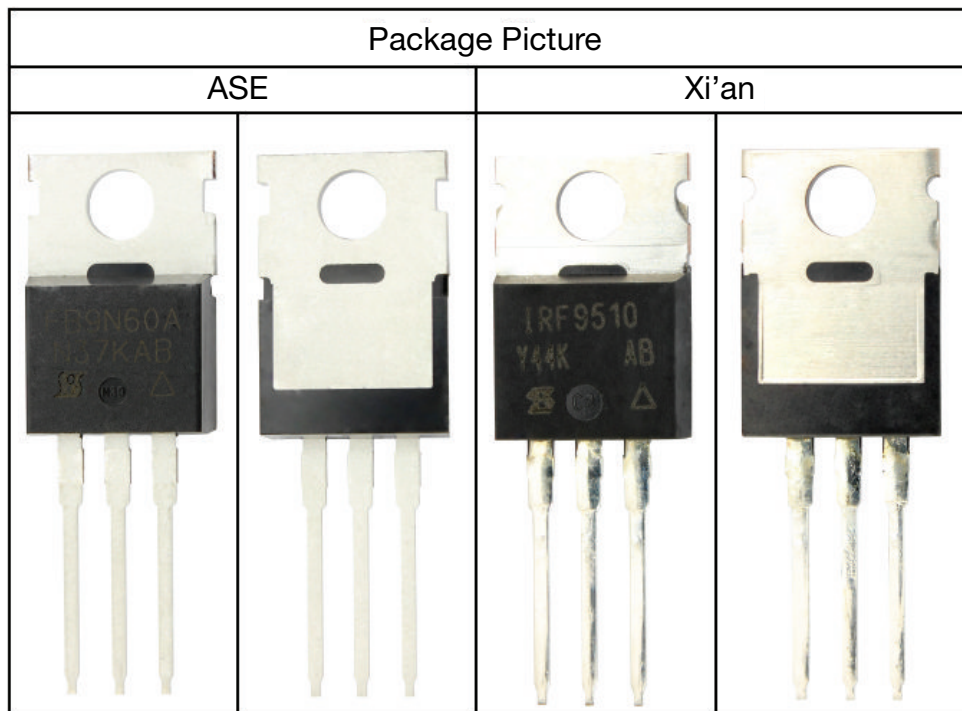


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- $M^*$  = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM







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