



Vishay Siliconix

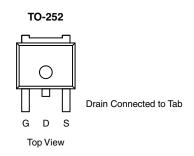
P-Channel 40 V (D-S) MOSFET

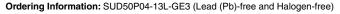
PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)		
- 40	0.013 at V _{GS} = - 10 V	- 55.7 ^c		
- 40	0.022 at V _{GS} = - 4.5 V	- 44.4		

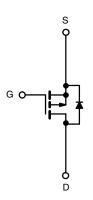
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC









P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 40		
Gate-Source Voltage		V_{GS}	± 20		
Ocaliana Basis Ocasasib	T _C = 25 °C	- I _D	- 55.7 ^c		
Continuous Drain Current ^b	T _C = 100 °C		- 35.2		
Pulsed Drain Current		I _{DM}	- 100		
Continuous Source Current (Diode Conduction)		I _S	- 52 ^c		
Avalanche Current	L = 0.1 mH		- 40		
Avalanche Energy	L = U.TIIIH	E _{AS}	80	mJ	
Mariana Barra Birataria	T _C = 25 °C	P _D	78 ^b	W	
Maximum Power Dissipation ^b	T _A = 25 °C	r D	3 ^a	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana Indiana Andriana	t ≤ 10 s	- R _{thJA}	15	18	°C/W
Maximum Junction-to-Ambient ^a	Steady State		40	50	
Maximum Junction-to-Case (Drain)		R _{thJC}	1.3	1.8	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See SOA curve for voltage derating.
- c. Calculated based on maximum allowed junction temperature. Package limitation current is 50 A.

SUD50P04-13L-GE3

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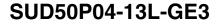
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	- 40			V
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1.0		- 3.0	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
7 0 1 1/1 5 1 0 1	,	V _{DS} = - 40 V, V _{GS} = 0 V			- 1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			- 50	μA
On-State Drain Current ^a	I _{D(on)}	V _{DS} = - 5 V, V _{GS} = - 10 V	- 50			Α
		V _{GS} = - 10 V, I _D = - 30 A		0.0105	0.013	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 30 A, T _J = 125 °C			0.020	Ω
		V _{GS} = - 4.5 V, I _D = - 20 A		0.017	0.022	1
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 30 A	15			S
Dynamic ^b						
Input Capacitance	C _{iss}			3120		pF
Output Capacitance	C _{oss}	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		440		
Reverse Transfer Capacitance	C _{rss}			320		
Gate Resistance	R_g	f = 1 MHz		4.3		Ω
Total Gate Charge ^c	Q_g			63	95	
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = -20 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -50 \text{ A}$		13		nC
Gate-Drain Charge ^c	Q_{gd}			16		
Turn-On Delay Time ^c	t _{d(on)}			15	25	
Rise Time ^c	t _r	V_{DD} = - 20 V, R_L = 0.4 Ω		18	30	20
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong -50 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 2.5 \Omega$		60	90	ns
Fall Time ^c	t _f			47	70	1
Drain-Source Body Diode Characteristic	s					
Pulse Current	I _{SM}				- 100	
Forward Voltage ^a	V_{SD}	I _F = - 50 A, V _{GS} = 0 V		- 1.0	- 1.5	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 50 A, dl/dt = 100 A/μs		36	55	ns

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

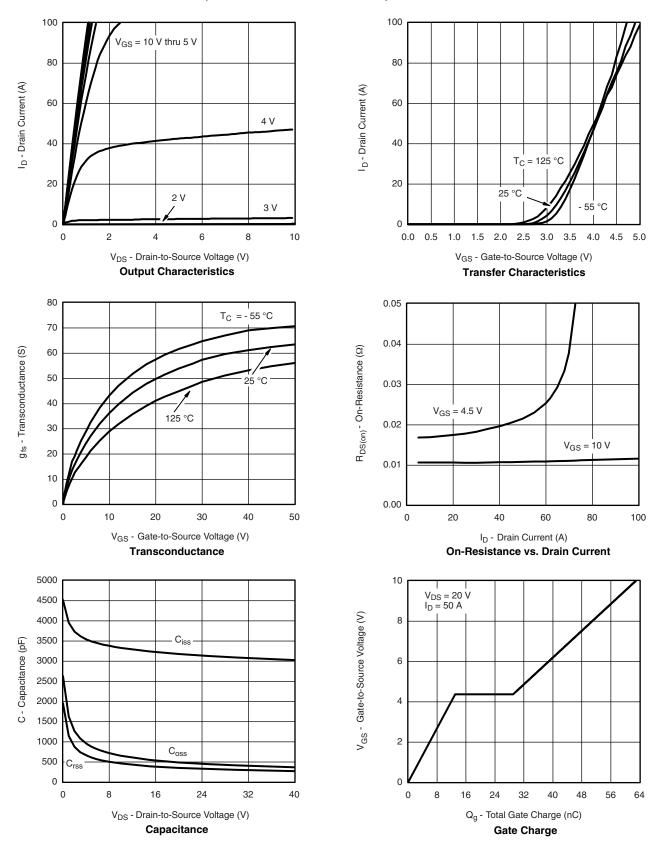
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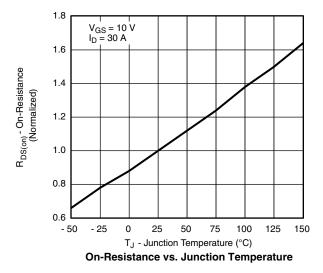
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

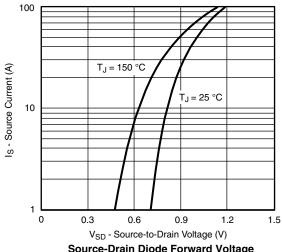


SUD50P04-13L-GE3

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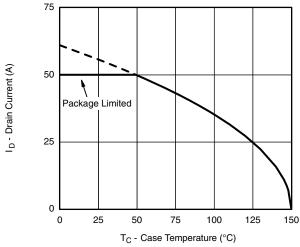
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

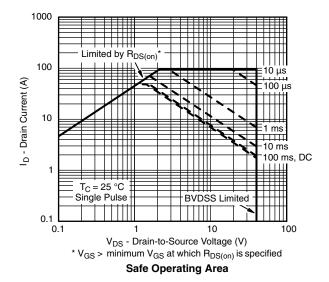




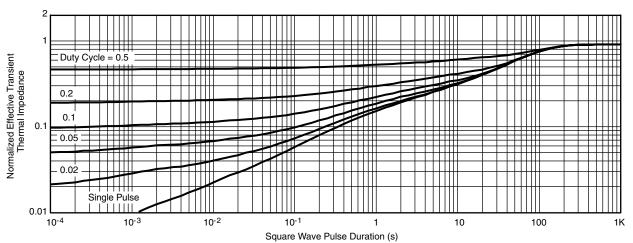
Source-Drain Diode Forward Voltage

THERMAL RATINGS









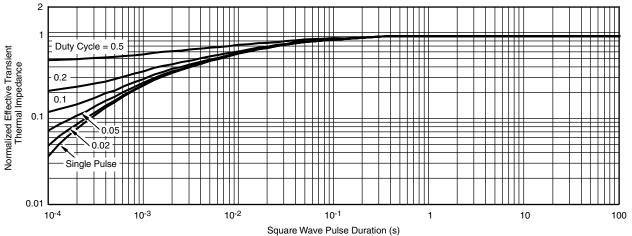
Normalized Thermal Transient Impedance, Junction-to-Ambient



SUD50P04-13L-GE3

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THERMAL RATINGS



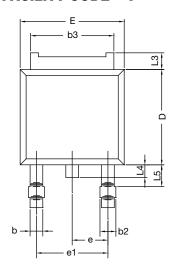
Normalized Thermal Transient Impedance, Junction-to-Case

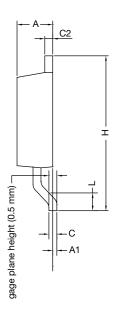
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67069.

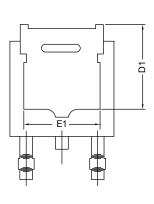
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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y







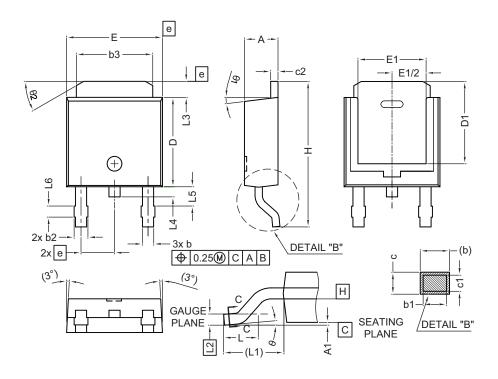
	MILLIMETERS		
DIM.	MIN.	MAX.	
А	2.18	2.38	
A1	-	0.127	
b	0.64	0.88	
b2	0.76	1.14	
b3	4.95	5.46	
С	0.46	0.61	
C2	0.46	0.89	
D	5.97	6.22	
D1	4.10	-	
Е	6.35	6.73	
E1	4.32	=	
Н	9.40	10.41	
е	2.28 BSC		
e1	4.56 BSC		
L	1.40	1.78	
L3	0.89	1.27	
L4	-	1.02	
L5	1.01	1.52	

Note

• Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	2.18	2.39	
A1	-	0.13	
b	0.65	0.89	
b1	0.64	0.79	
b2	0.76	1.13	
b3	4.95	5.46	
С	0.46	0.61	
c1	0.41	0.56	
c2	0.46	0.60	
D	5.97	6.22	
D1	5.21	=	
E	6.35	6.73	
E1	4.32 -		
е	2.29 BSC		
Н	9.94	10.34	

	MILLIMETERS		
DIM.	MIN.	MAX.	
L	1.50	1.78	
L1	2.74 ref.		
L2	0.51 BSC		
L3	0.89	1.27	
L4	-	1.02	
L5	1.14	1.49	
L6	0.65	0.85	
θ	0°	10°	
θ1	0°	15°	
θ2	25°	35°	

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- · Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019

DWG: 5347



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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