Vishay Siliconix

P-Channel 30 V (D-S) MOSFET

PowerPAK® SC-70-6L Single



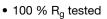


Marking code: KA

PRODUCT SUMMARY								
V _{DS} (V)	-30							
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10 \text{ V}$	0.020							
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.033							
Q _g typ. (nC)	8.3							
I _D (A) ^f	-12							
Configuration	Single							

FEATURES

- TrenchFET® Gen IV p-channel power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
- Provides excellent R_{DS}-Q_g Figure-of-Merit (FOM) for switching applications



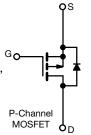
 Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Pb-free

ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Battery charging and management
- Load switch
- DC/DC converters
- Power management in battery-operated, mobile and wearable devices



ORDERING INFORMATION	
Package	PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiA483ADJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
PARAMETER		SYMBOL	LIMIT	UNIT			
Drain-source voltage		V _{DS}	-30	V			
Gate-source voltage		V_{GS}	-20 / +16	7 v			
	T _C = 25 °C		-12 ^f				
Continuous drain current (T _{.1} = 150 °C)	T _C = 70 °C	1 ,	-12 ^f				
Continuous drain current (1, = 150 °C)	T _A =25 °C	I _D	-10.6 ^{a, b}				
	T _A = 70 °C		-8.5 ^{a, b}	Α			
Pulsed drain current (t = 100 μs)		I _{DM}	-60				
Continuous source-drain diode current	T _C = 25 °C		-12 ^f				
Continuous source-drain diode current	T _A = 25 °C	I _S	-2.9 ^{a, b}				
	T _C = 25 °C		17.9				
Maximum power dissipation	T _C = 70 °C		11.4	w			
Maximum power dissipation	T _A = 25 °C	P _D	3.4 ^{a, b}				
	T _A = 70 °C	1	2.2 ^{a, b}				
Operating junction and storage temperature	range	T _J , T _{stg}	-55 to +150	°C			
Soldering recommendations (peak tempera	ture) ^{c, d}		260				

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum junction-to-ambient a, e	t ≤ 5 s	R _{thJA}	29	37	°C/W				
Maximum junction-to-case (drain)	Steady state	R _{thJC}	5.5	7	C/VV				

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 5 s
- c. See solder profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- e. Maximum under steady state conditions is 80 °C/W
- f. Package limited



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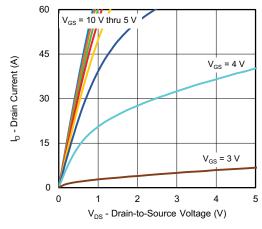
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	•			•	•	
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-30	-	-	٧
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	-26	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	5	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-	-2.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = -20 \text{ V} / +16 \text{ V}$	-	-	± 100	nA
Zoro goto voltago droip ourrent		V _{DS} = -30 V, V _{GS} = 0 V	-	-	-1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = 0 \text{ V}$	-10	-	-	Α
Darie de la contra del contra de la contra del la contra de la contra de la contra de la contra del la contra de la contra de la contra del la contra de la contra de la contra de la contra del la contra del la contra de la contra de la contra del la c	_	$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	-	0.016	0.020	_
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$	-	0.025	0.033	Ω
Forward transconductance ^a	9 _{fs}	$V_{DS} = -10 \text{ V}, I_D = -5 \text{ A}$	-	25	-	S
Dynamic ^b				•	•	
Input capacitance	C _{iss}		-	950	-	
Output capacitance	C _{oss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	460	-	pF
Reverse transfer capacitance	C _{rss}		-	50	-	
Total gate charge	Qg	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10.6 \text{ A}$	-	17	26	
		$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10.6 \text{ A}$	-	8.3	12.5	
Gate-source charge	Q _{gs}	V 45VV 45VI 40CA	-	3.7	-	nC
Gate-drain charge	Q _{gd}	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10.6 \text{ A}$	-	3	-	1
Gate resistance	R_{g}	f = 1 MHz	1.5	8.8	15	Ω
Turn-on delay time	t _{d(on)}		-	26	52	
Rise time	t _r	$V_{DD} = -15 \text{ V}, R_1 = 1.8 \Omega, I_D \cong -8.5 \text{ A},$	-	95	190	
Turn-off delay time	t _{d(off)}	$V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	24	80	
Fall time	t _f		-	16	32	
Turn-on delay time	t _{d(on)}		-	12	24	ns
Rise time	t _r	$V_{DD} = -15 \text{ V}, R_{I} = 1.8 \Omega, I_{D} \cong -8.5 \text{ A},$	-	6	12	
Turn-off delay time	t _{d(off)}	$V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	30	60	
Fall time	t _f		-	8	16	
Drain-Source Body Diode Characteristi	cs			•	•	
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-12	_
Pulse diode forward current	I _{SM}		-	-	-60	A
Body diode voltage	V_{SD}	I _S = -10 A, V _{GS} = 0 V	-	-0.85	-1.2	V
Body diode reverse recovery time	t _{rr}		-	19	38	ns
Body diode reverse recovery charge	Q _{rr}	I _F = -8.5 A, di/dt = 100 A/μs,	-	7	14	nC
Reverse recovery fall time	T _J = 25 °C	-	9	-		
Reverse recovery rise time	t _a		_	10	_	ns

Notes

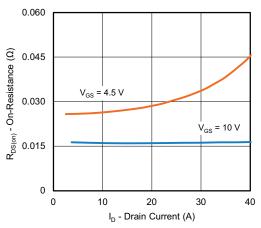
- a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

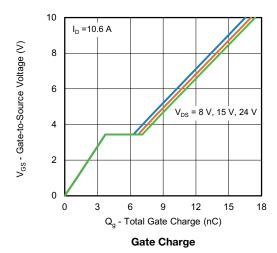


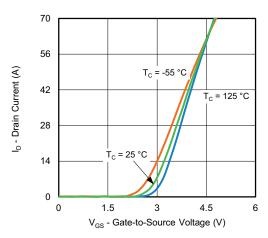


Output Characteristics

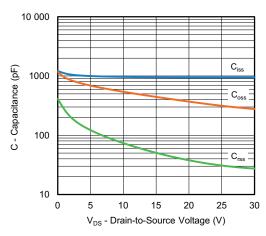


On-Resistance vs. Drain Current and Gate Voltage

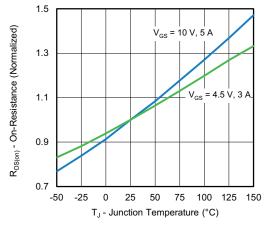




Transfer Characteristics

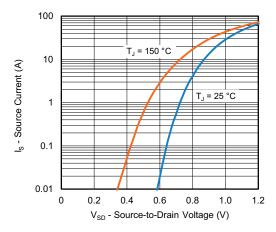


Capacitance

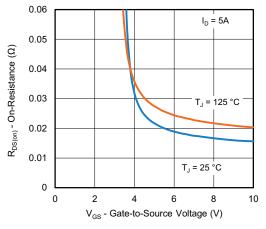


On-Resistance vs. Junction Temperature

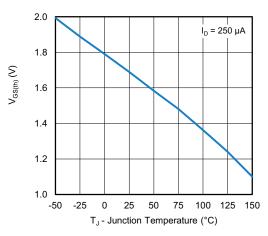




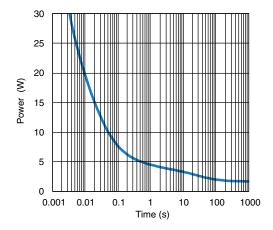
Source-Drain Diode Forward Voltage



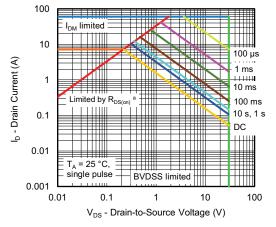
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



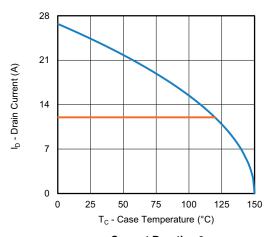
Safe Operating Area, Junction-to-Ambient

Note

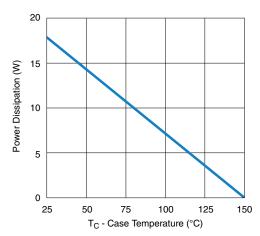
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

S19-0391-Rev. A, 29-Apr-2019

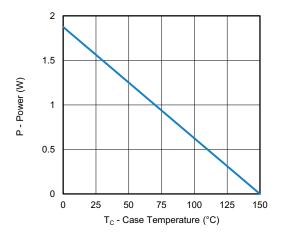




Current Derating a





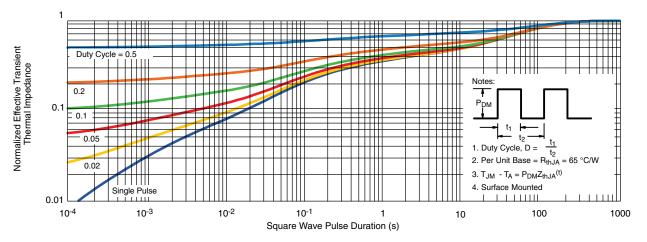


Power, Junction-to-Ambient

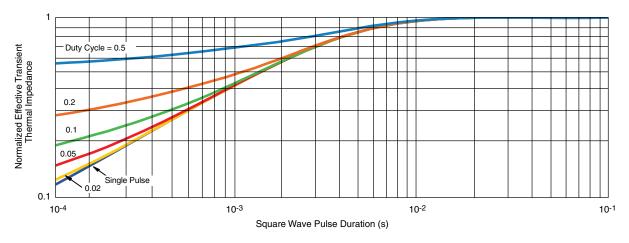
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

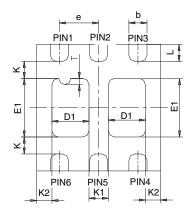
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77080.



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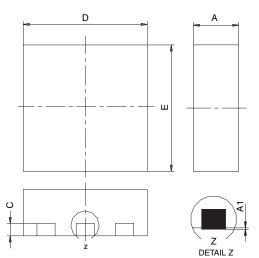
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

	SINGLE PAD						DUAL PAD						
DIM	M	ILLIMETER	RS	INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC			
K		0.275 TYP			0.011 TYP	1	0.275 TYP			0.011 TYP			
K1		0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
К3		0.225 TYP		0.009 TYP									
K4		0.355 TYP		0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
ECN: C-07431 - Rev. C. 06-Aug-07													

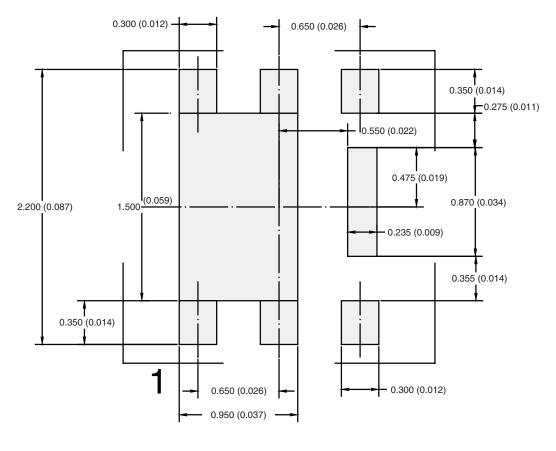
DWG: 5934

Document Number: 73001 06-Aug-07

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RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOTE

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