

N-Channel 240-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
240	2.9 at V _{GS} = 10 V	1.52	2.54 nC
	2.95 at V _{GS} = 4.5 V	1.5	
	3.5 at V _{GS} = 2.5 V	1.44	

FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance

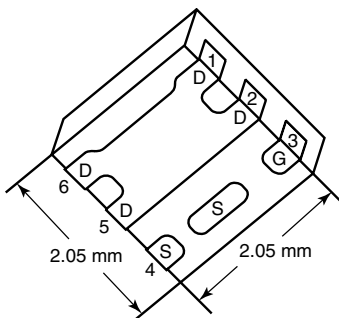


RoHS
COMPLIANT

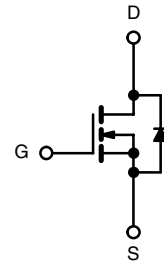
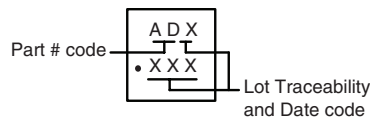
APPLICATIONS

- Boost Converter for Portable Devices

PowerPAK SC-70-6L-Single



Marking Code



N-Channel MOSFET

Ordering Information: SiA450DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	240	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	1.52	A
	T _C = 70 °C	1.21	
	T _A = 25 °C	0.70 ^{a, b}	
	T _A = 70 °C	0.56 ^{a, b}	
Pulsed Drain Current	I _{DM}	1.5	
Continuous Source-Drain Diode Current	T _C = 25 °C	12.8	
	T _A = 25 °C	2.74 ^{a, b}	
Maximum Power Dissipation	T _C = 25 °C	15	W
	T _C = 70 °C	9.8	
	T _A = 25 °C	3.3 ^{a, b}	
	T _A = 70 °C	2.1 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, e}	R _{thJA}	30	38	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	6.5	8.1	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed solder tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 80 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	240			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		247.4		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.22		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	0.8		2.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 240\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = 240\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 10\text{ V}$, $V_{GS} = 10\text{ V}$	1.5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 0.70\text{ A}$		2.4	2.9	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 0.65\text{ A}$		2.46	2.95	
		$V_{GS} = 2.5\text{ V}$, $I_D = 0.50\text{ A}$		2.85	3.5	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 120\text{ V}$, $I_D = 0.70\text{ A}$		3.14		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 120\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		167		pF
Output Capacitance	C_{oss}			10		
Reverse Transfer Capacitance	C_{rss}			3.4		
Total Gate Charge	Q_g	$V_{DS} = 120\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 0.70\text{ A}$		4.69	7.035	nC
				2.54	3.81	
Gate-Source Charge	Q_{gs}	$V_{DS} = 120\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 0.70\text{ A}$		0.58		
Gate-Drain Charge	Q_{gd}			1.14		
Gate Resistance	R_g	$f = 1\text{ MHz}$		2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 120\text{ V}$, $R_L = 200\text{ }\Omega$ $I_D \cong 0.60\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		13.7	21	ns
Rise Time	t_r			22	33	
Turn-Off Delay Time	$t_{d(off)}$			23	35	
Fall Time	t_f			19	29	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 120\text{ V}$, $R_L = 184\text{ }\Omega$ $I_D \cong 0.70\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		4.5	6.75	
Rise Time	t_r			11	16.5	
Turn-Off Delay Time	$t_{d(off)}$			12	18	
Fall Time	t_f			15	22.5	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			2.7	A
Pulse Diode Forward Current	I_{SM}				12.8	
Body Diode Voltage	V_{SD}	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 0.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		50.2	75.3	ns
Body Diode Reverse Recovery Charge	Q_{rr}			68	102	nC
Reverse Recovery Fall Time	t_a			25		ns
Reverse Recovery Rise Time	t_b			25.2		

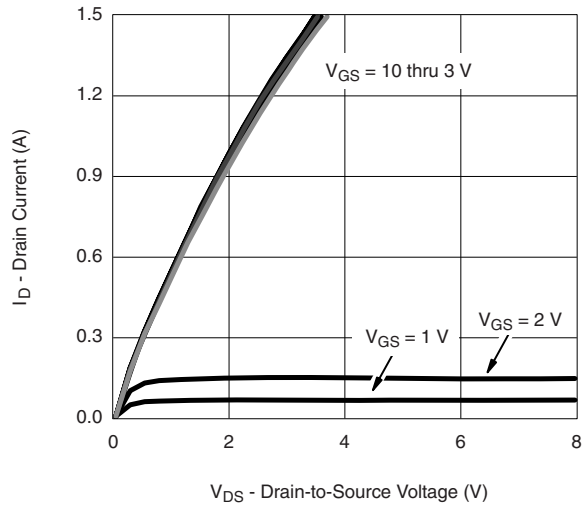
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

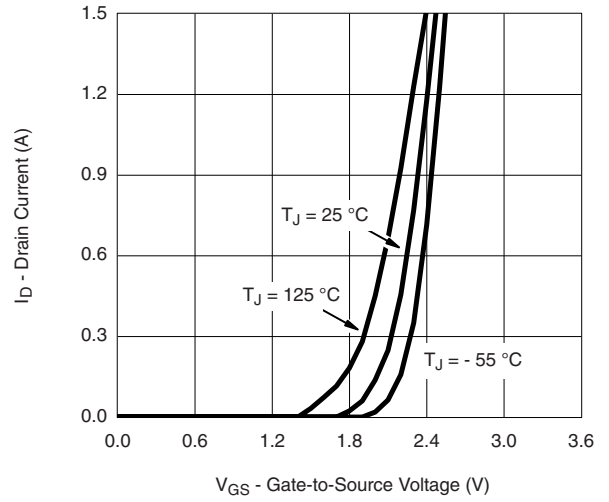
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



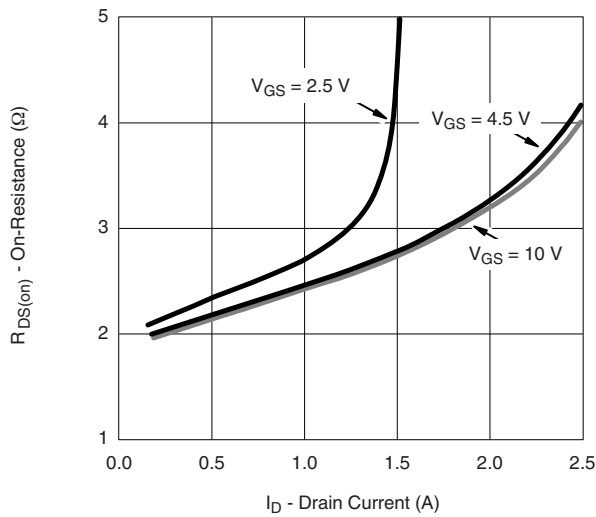
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



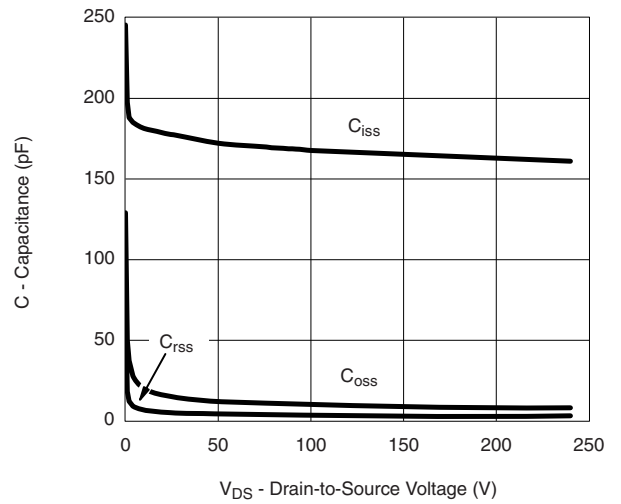
Output Characteristics



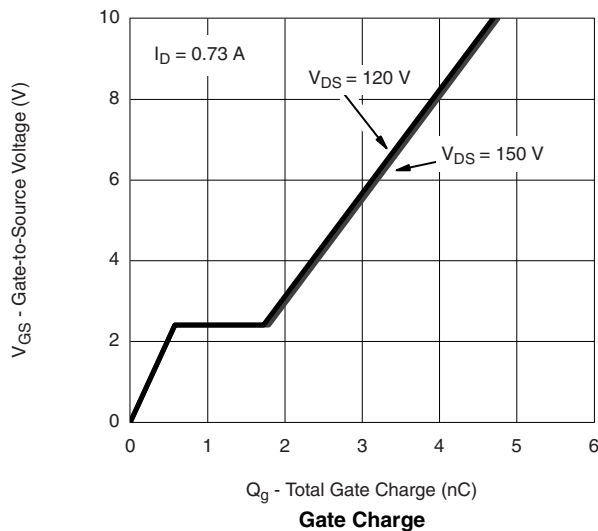
Transfer Characteristics



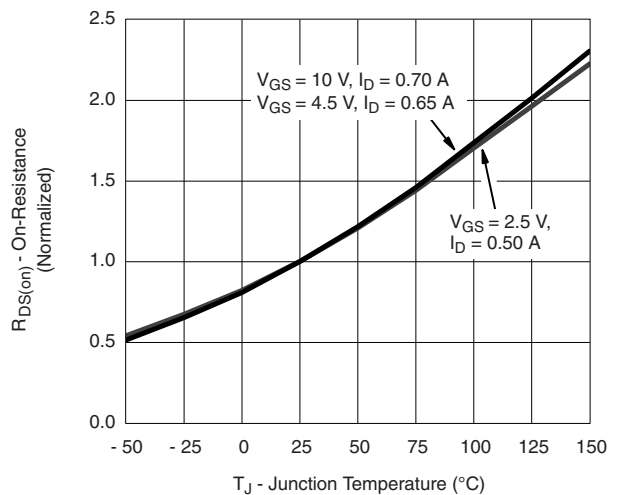
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



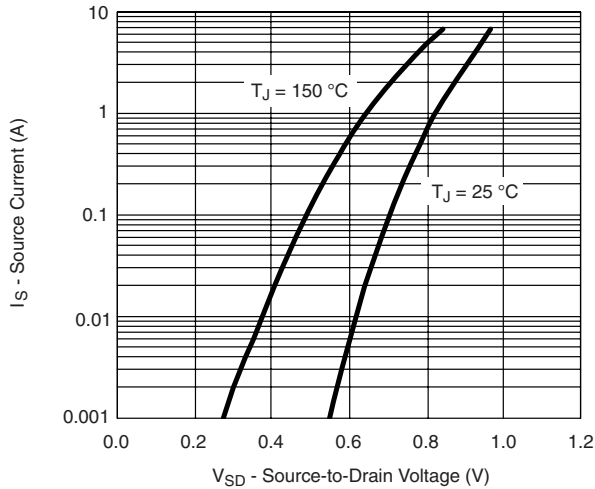
Gate Charge



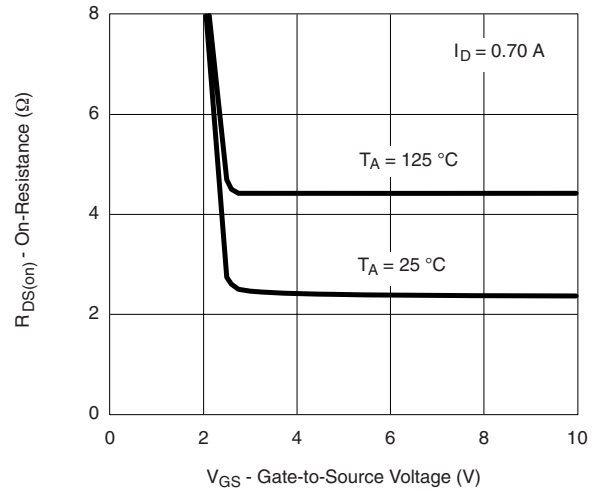
On-Resistance vs. Junction Temperature



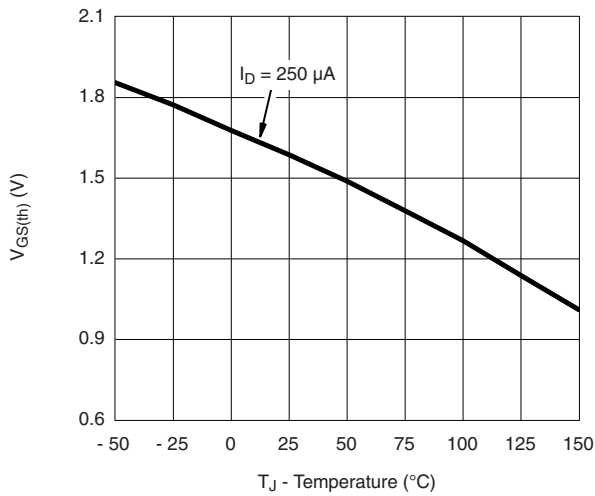
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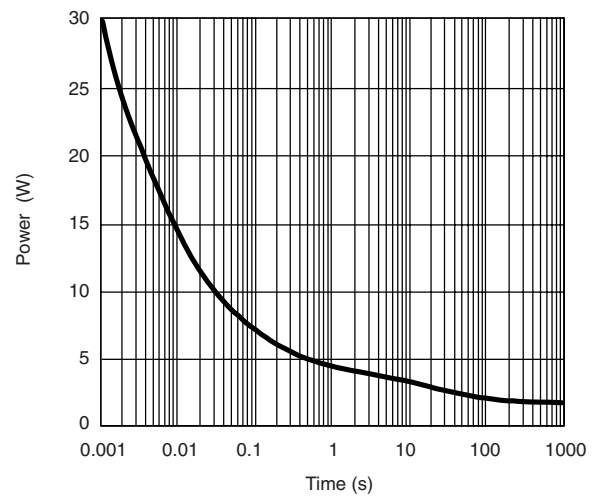
Source-Drain Diode Forward Voltage



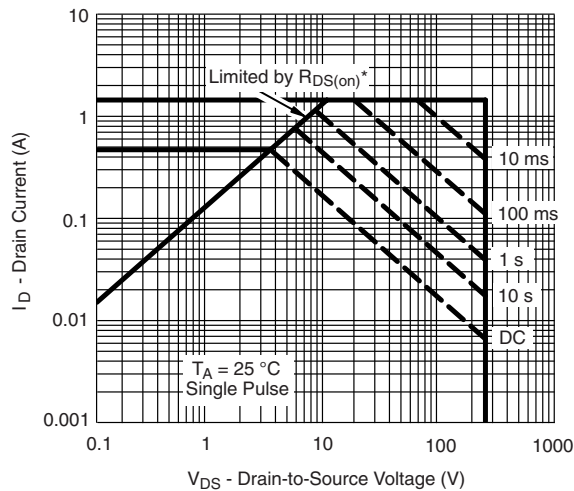
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

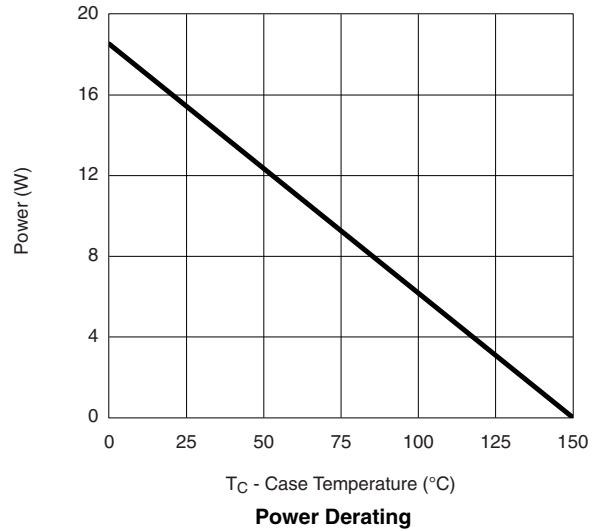
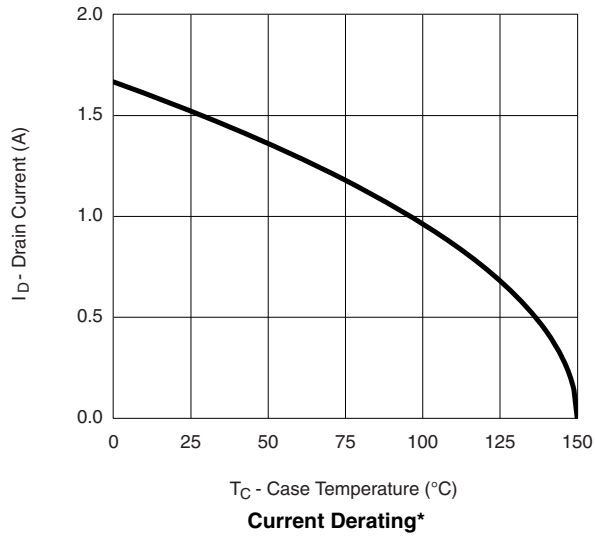


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



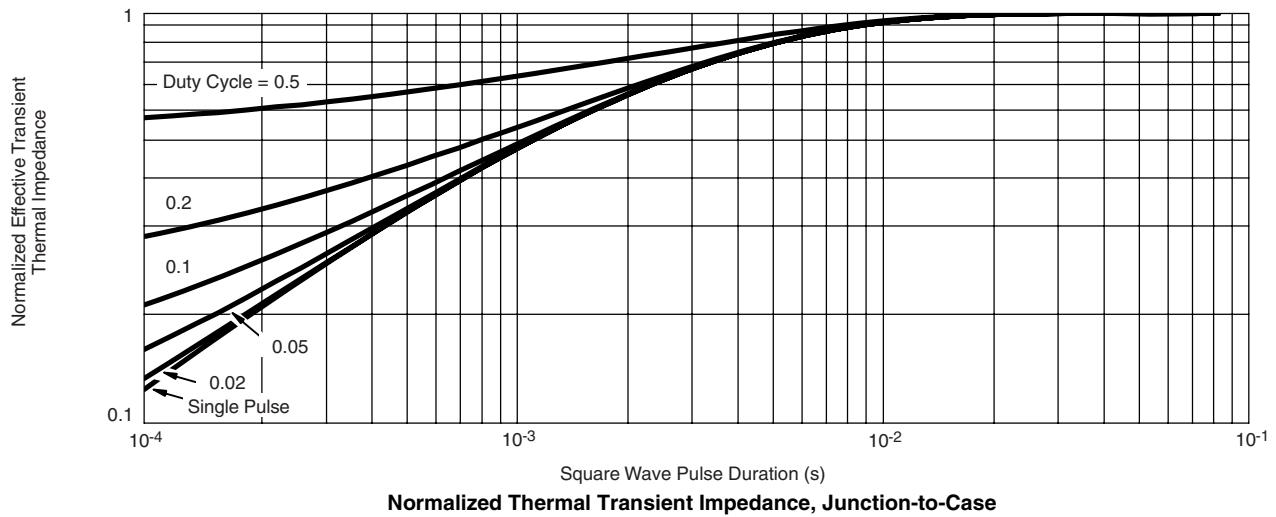
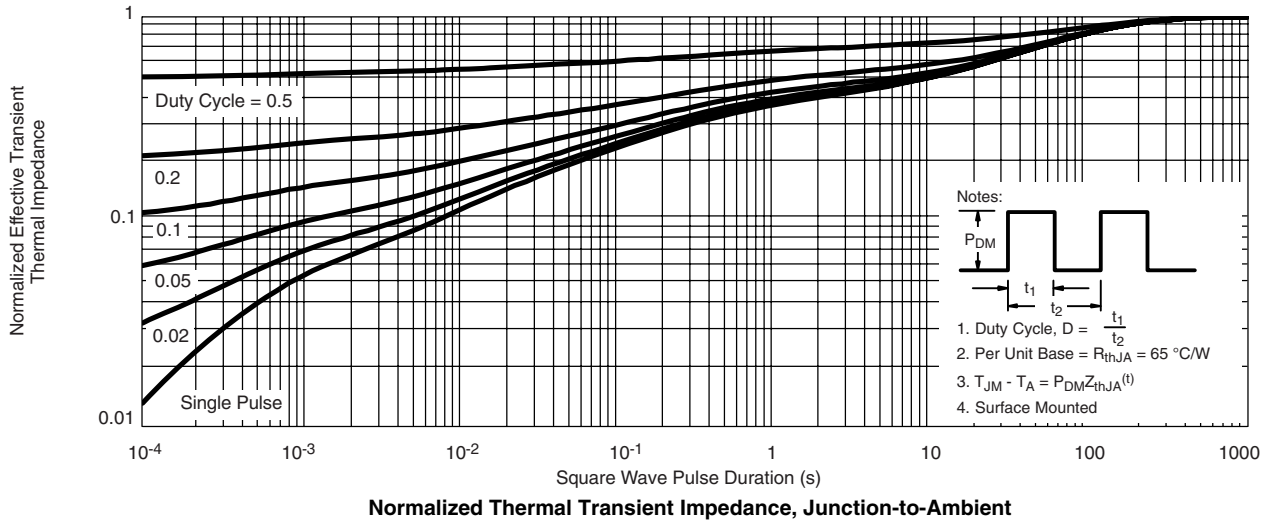
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiA450DJ

Vishay Siliconix



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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