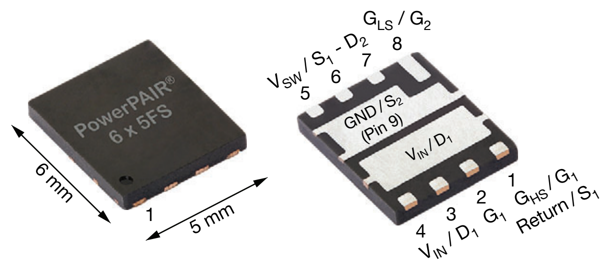
Symmetric Dual N-Channel 40 V (D-S) MOSFET

PowerPAIR® 6 x 5FS



Top View   Bottom View

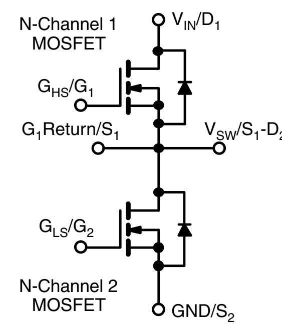
FEATURES

- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Symmetric dual N-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Buck-boost
- Half-bridge synchronous rectification
- Telecom DC/DC
- Motor drive control



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00137
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00240
Q_g typ. (nC)	30
I_D (A) [a]	159
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5FS
Lead (Pb)-free and halogen-free	SiZF640DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	+20, -16	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	159	A
	T_C = 70 °C		127	
	T_A = 25 °C		41 [b, c]	
	T_A = 70 °C		33 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	300	
Continuous source-drain diode current	T_C = 25 °C	I_S	57	
	T_A = 25 °C		3.8 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	40	
Single pulse avalanche energy		E_{AS}	80	mJ
Maximum power dissipation	T_C = 25 °C	P_D	62.5	W
	T_C = 70 °C		40	
	T_A = 25 °C		4.2 [b, c]	
	T_A = 70 °C		2.7 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient [a, b]	$t \leq 10$ s	R_{thJA}	24	30	°C/W
Maximum junction-to-case (source)	Steady state	R_{thJC}	1.6	2.0	

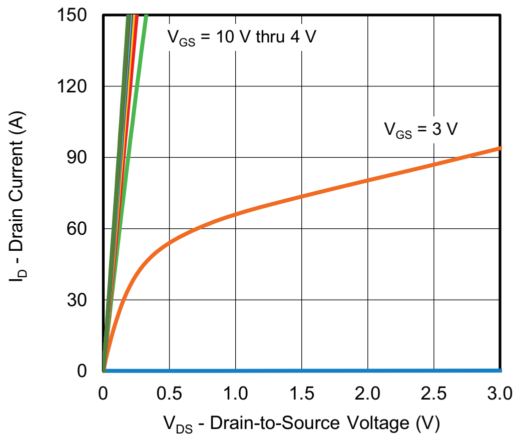
Notes
a. Surface mounted on 1" x 1" FR4 board
b. Maximum under steady state conditions is 60 °C/W for channel-1 and channel-2

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	40	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 10 mA	-	25.3	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 μA	-	-5.5	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1	-	2.4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 70 °C	-	-	10	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	-	0.0010	0.00137	Ω
		V_{GS} = 4.5 V, I_D = 15 A	-	0.0016	0.00240	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 45 A	-	175	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	-	5750	-	pF
Output capacitance	C_{oss}		-	960	-	
Reverse transfer capacitance	C_{rss}		-	55	-	
Total gate charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 15 A	-	69	106	nC
		V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 15 A	-	30	45	
Gate-source charge	Q_{gs}		-	21	-	
Gate-drain charge	Q_{gd}		-	1.5	-	
Output charge	Q_{oss}	V_{DS} = 20 V, V_{GS} = 0 V	-	46	-	
Gate resistance	R_g	f = 1 MHz	0.4	1.7	3.4	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω, $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	-	18	40	ns
Rise time	t_r		-	45	90	
Turn-off delay time	$t_{d(off)}$		-	45	90	
Fall time	t_f		-	6	12	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω, $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	50	100	
Rise time	t_r		-	115	230	
Turn-off delay time	$t_{d(off)}$		-	40	80	
Fall time	t_f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	57	A
Pulse diode forward current	I_{SM}		-	-	300	
Body diode voltage	V_{SD}	I_S = 10 A, V_{GS} = 0 V	-	0.75	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 10 A, di/dt = 100 A/μs, T_J = 25 °C	-	40	80	ns
Body diode reverse recovery charge	Q_{rr}		-	36	75	nC
Reverse recovery fall time	t_a		-	25	-	ns
Reverse recovery rise time	t_b		-	15	-	

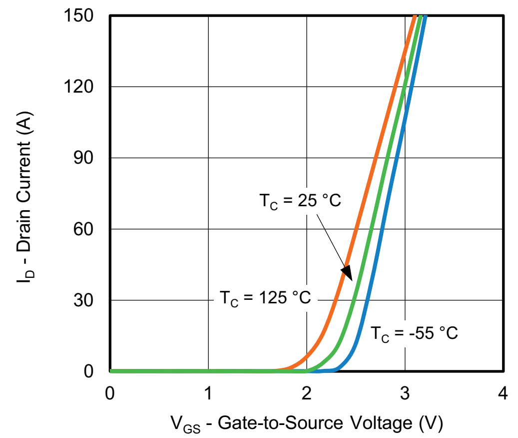
Notes
c. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
d. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

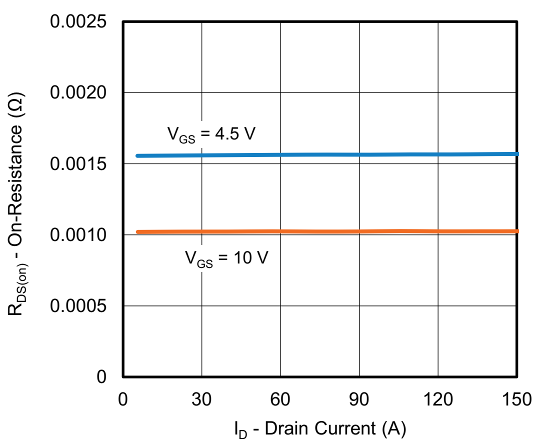
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



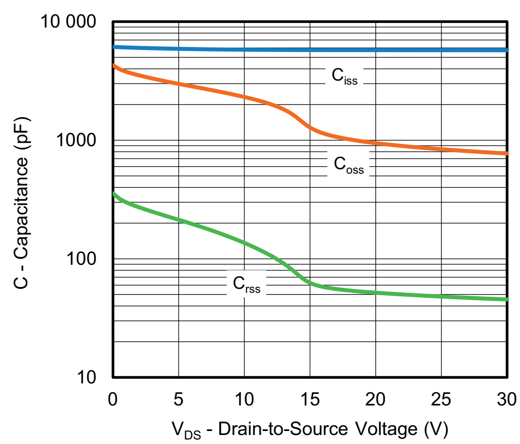
Output Characteristics



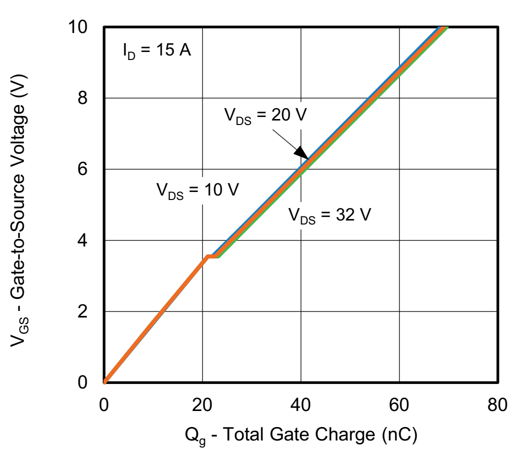
Transfer Characteristics



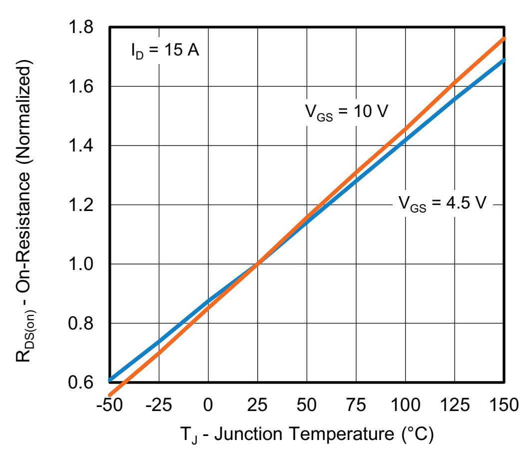
On-Resistance vs. Drain Current



Capacitance

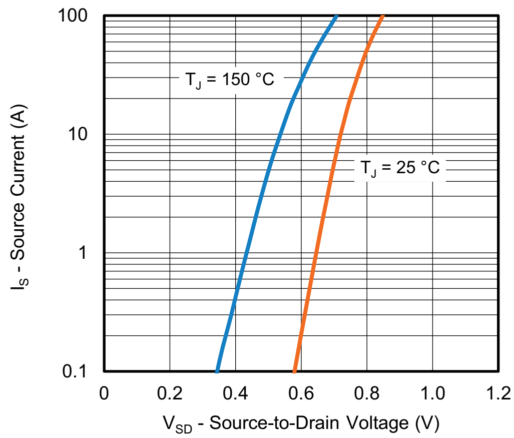


Gate Charge

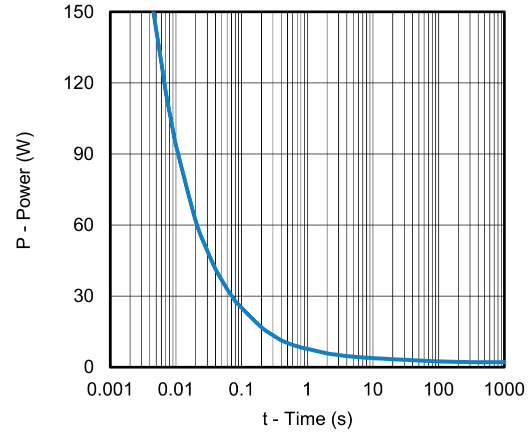


On-Resistance vs. Junction Temperature

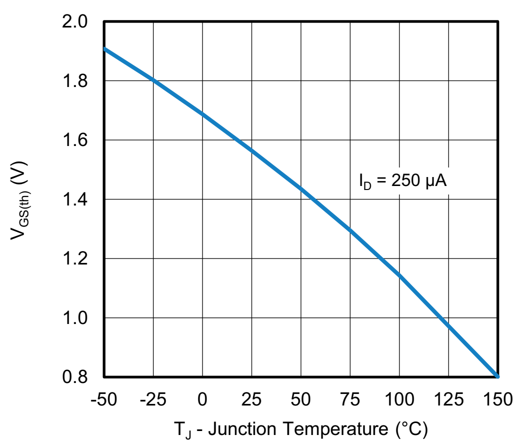
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



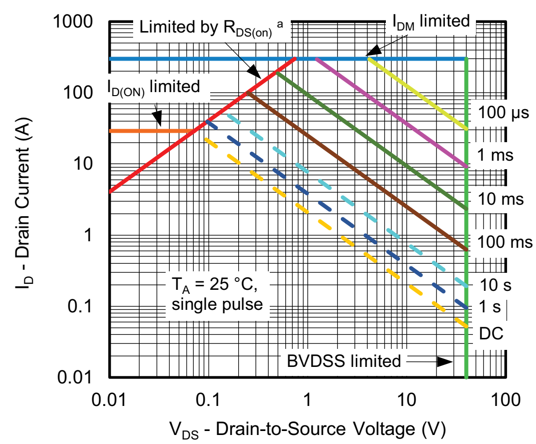
Source-Drain Diode Forward Voltage



Single Pulse Power, Junction-to-Ambient



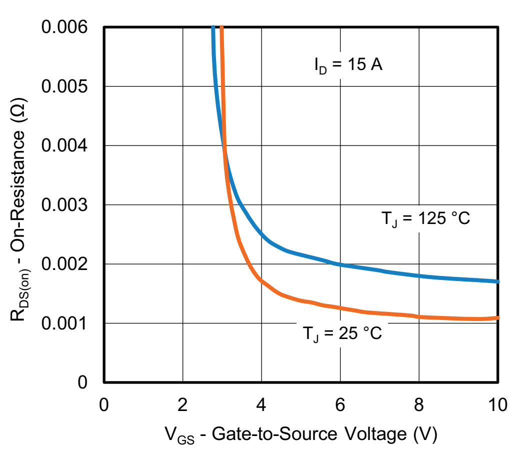
Threshold Voltage



Safe Operating Area, Junction-to-Ambient

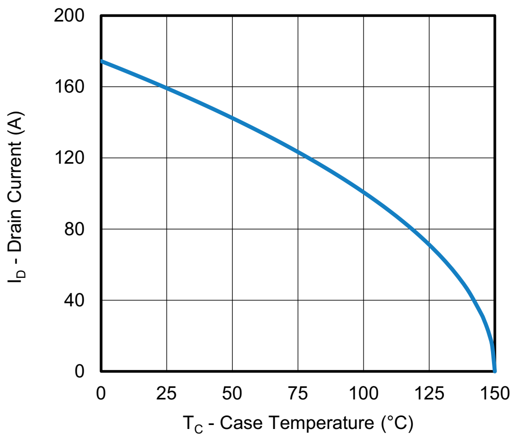
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

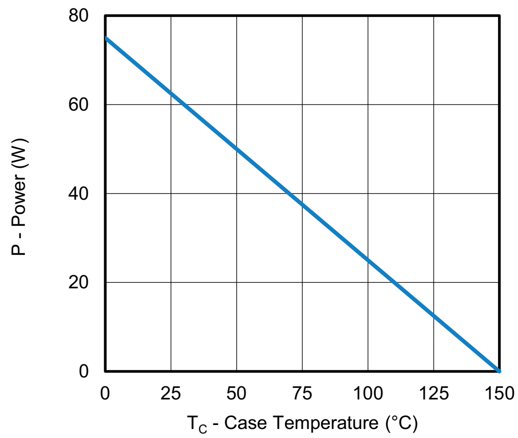


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

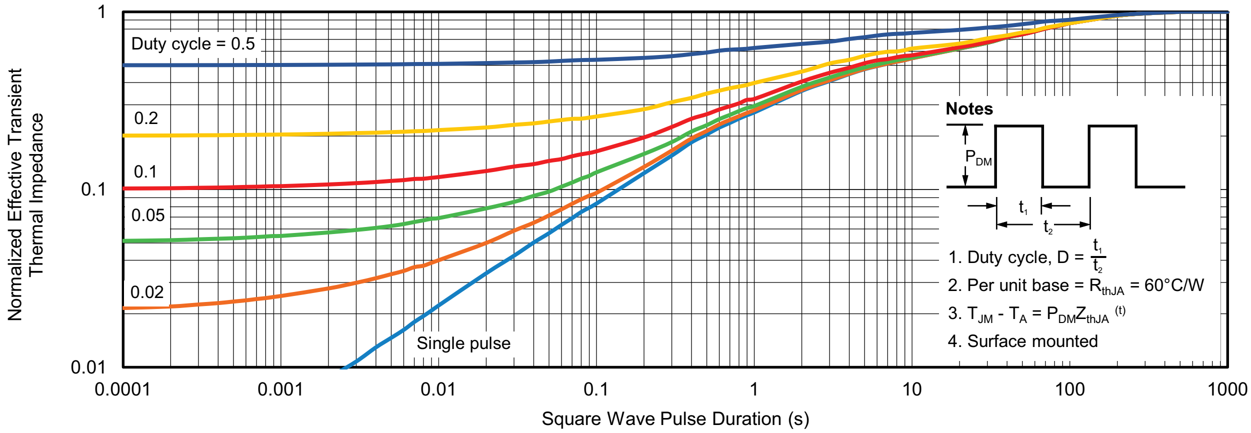


Power, Junction-to-Case

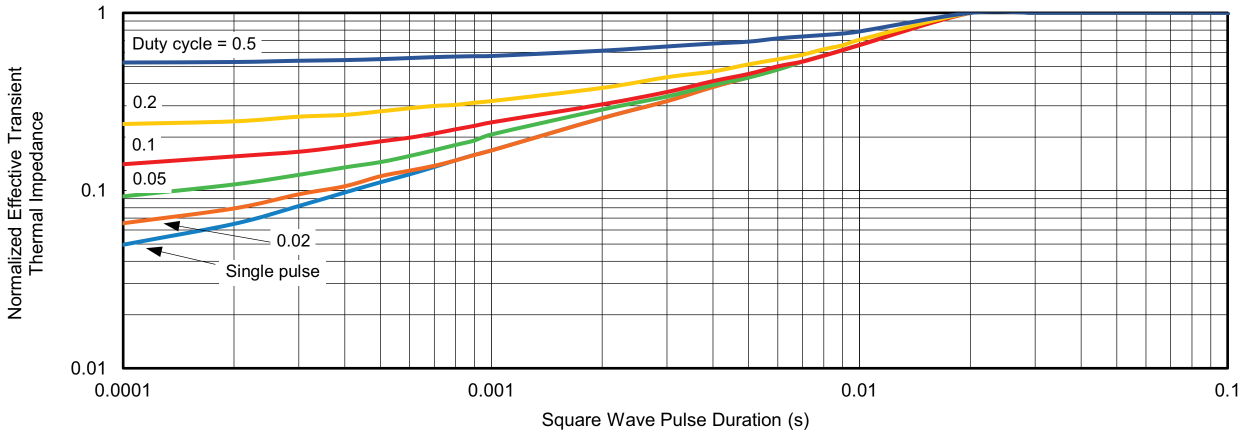
Note

b. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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