



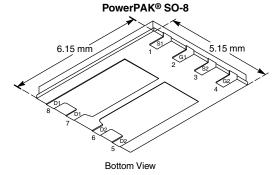
Dual N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
30	0.022 at V _{GS} = 10 V	10		
	0.030 at V _{GS} = 4.5 V	8.5		

FEATURES

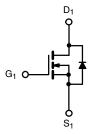
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



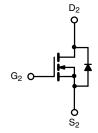


Ordering Information: Si7844DP-T1-E3 (Lead (Pb)-free)

Si7844DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		v
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	- I _D	10	6.4	Α
	T _A = 70 °C		8.0	5.1	
Pulsed Drain Current		I _{DM}	20		^
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.1	I
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.5	1.4	W
Waximum Fower Dissipation	T _A = 70 °C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana harding to Antiquia	t ≤ 10 s	R _{thJA}	26	35	°C/W
Maximum Junction-to-Ambient ^a	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State		3.9	5.5	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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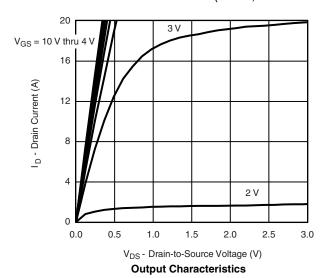
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.8		2.4	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	,	V _{DS} = 30 V, V _{GS} = 0 V			1	
	IDSS	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α
Drain-Source On-State Resistance ^a	Б	V _{GS} = 10 V, I _D = 10 A		0.018	0.022	-
	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 8.5 A		0.024	0.030	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A		22		S
Diode Forward Voltage ^a	V_{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.75	1.2	V
Dynamic ^b						
Total Gate Charge	Q_g			13	20	
Gate-Source Charge	Q _{gs} Q _{gd}	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		2		nC
Gate-Drain Charge				2.7		İ
Gate Resistance	R_g		0.5		3.2	Ω
Turn-On Delay Time	t _{d(on)}			8	16	
Rise Time	$ \begin{array}{c c} & t_r & V_{DD} = 15 \text{ V, } R_L = 15\Omega \\ \hline t_{d(off)} & I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 6 \Omega \\ \end{array} $		10	20		
Turn-Off Delay Time		$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		21	40	ns
Fall Time	t _f			10	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, dI/dt = 100 A/μs		40	80	

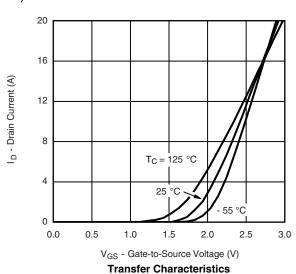
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

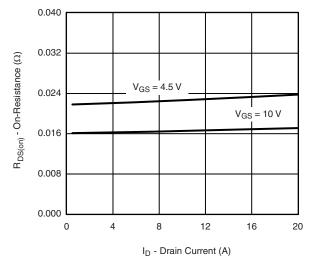




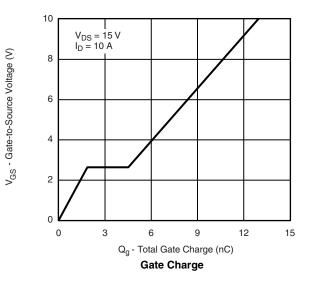


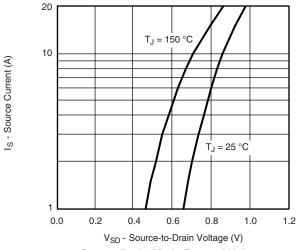


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

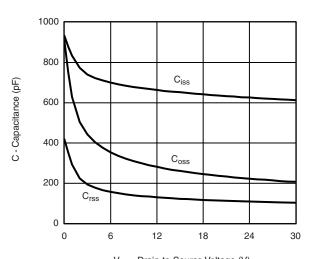


On-Resistance vs. Drain Current

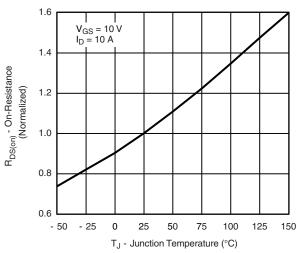




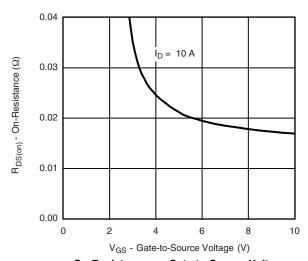
Source-Drain Diode Forward Voltage



V_{DS} - Drain-to-Source Voltage (V) Capacitance



On-Resistance vs. Junction Temperature

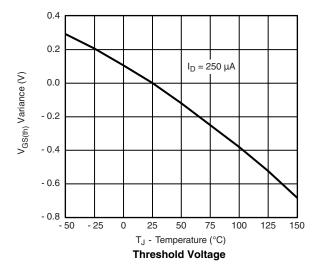


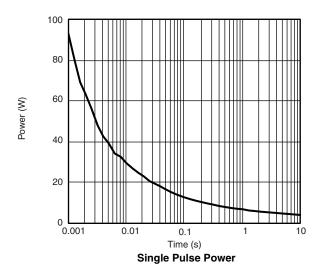
On-Resistance vs. Gate-to-Source Voltage

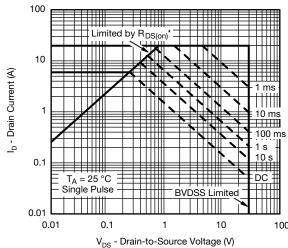
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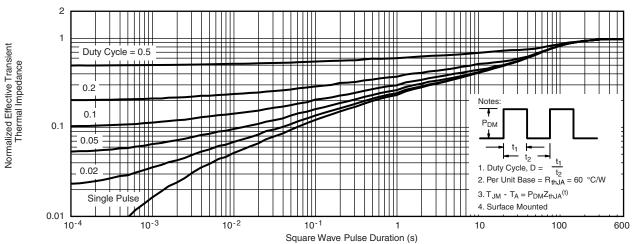
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)







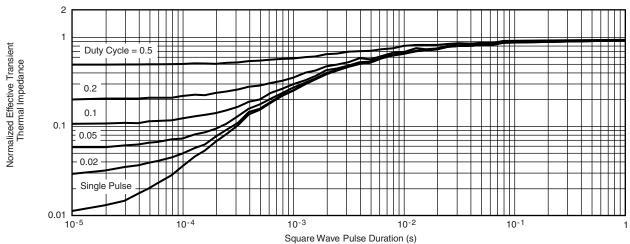
 * V $_{GS}$ > minimum V $_{GS}$ at which R $_{DS(on)}$ is specified **Safe Operating Area**



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

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