

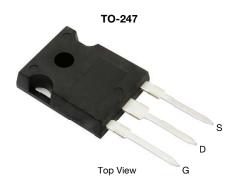
Vishay Siliconix

COMPLIANT

HALOGEN

**FREE** 

# N-Channel 150 V (D-S) 175 °C MOSFET



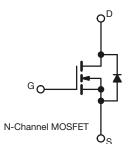
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	150		
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0054		
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.0060		
Q <sub>g</sub> typ. (nC)	110		
I <sub>D</sub> (A)	100 d		
Configuration	Single		

#### **FEATURES**

- ThunderFET® power MOSFET
- Low R<sub>DS</sub> Q<sub>g</sub> figure-of-merit (FOM)
- Maximum 175 °C junction temperature
- 100 % R<sub>a</sub> and UIS tested
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>

#### **APPLICATIONS**

- Synchronous rectification
- · Power supplies
- DC/AC inverter
- DC/DC converter
- Solar micro inverter
- · Motor drive switch



ORDERING INFORMATION		
Package	TO-247	
Lead (Pb)-free and halogen-free	SUG80050E-GE3	

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	150	.,
Gate-source voltage		$V_{GS}$	± 20	V
Continuous dunin automat	T <sub>C</sub> = 25 °C		100 <sup>d</sup>	
Continuous drain current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	100 <sup>d</sup>	
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	300	Α
Continuous source-drain diode current		I <sub>S</sub>	100 <sup>d</sup>	
Single pulse avalanche current a	ngle pulse avalanche current a		100	
Single pulse avalanche energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	500	mJ
T <sub>C</sub> = 25 °C			500 <sup>b</sup>	10/
Maximum power dissipation	T <sub>C</sub> = 125 °C	P <sub>D</sub>	167 <sup>b</sup>	W
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	
Soldering recommendations (peak temperature) <sup>c</sup>			260	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	MAXIMUM	UNIT
Maximum junction-to-ambient (PCB mount) °		R <sub>thJA</sub>	40	°C/W
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	0.3	]

#### Notes

- a. Duty cycle ≤ 1 %
- b. See SOA curve for voltage derating
- c. When mounted on 1" square PCB (FR4 material)
- d. Package limited



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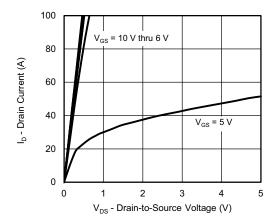
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	150	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	-	4	V	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	250	nA	
		$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125 ^{\circ}\text{C}$	-	-	150	μΑ	
		$V_{DS}$ = 150 V, $V_{GS}$ = 0 V, $T_J$ = 175 °C	-	-	5	mA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	Α	
Drain-source on-state resistance a	D	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	0.0045	0.0054	0	
Dialii-Source oii-state resistance "	R <sub>DS(on)</sub>	$V_{GS} = 7.5 \text{ V}, I_D = 15 \text{ A}$	-	0.0050	0.0063	Ω	
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 20 \text{ A}$	-	60	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	6250	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	1100	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	65	-		
Total gate charge	Qg		-	110	165		
Gate-source charge	$Q_{gs}$	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	33	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	28	-		
Gate resistance	Rg	f = 1 MHz	0.6	3.1	6.2	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	18	27		
Rise time	t <sub>r</sub>	$V_{DD} = 75 \text{ V}, \text{ R}_{L} = 5 \Omega, \text{ I}_{D} \cong 15 \text{ A},$	-	44	66		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$	-	72	108	ns	
Fall time	t <sub>f</sub>		-	55	83		
<b>Drain-Source Body Diode Characteristi</b>	cs						
Pulse diode forward current (t = 100 μs)	I <sub>SM</sub>		-	-	100	Α	
Body diode voltage	V <sub>SD</sub>	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V	-	0.85	1.5	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	130	195	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	L = 15 A dl/dt = 100 A/vo	-	0.71	1.07	μC	
Reverse recovery fall time	t <sub>a</sub>	I <sub>F</sub> = 15 A, dl/dt = 100 A/μs	-	97	-		
Reverse recovery rise time	t <sub>b</sub>		-	33	-	ns	
Body diode peak reverse recovery charge	I <sub>RM(REC)</sub>		-	12	18	Α	

## Notes

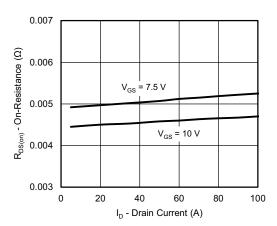
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

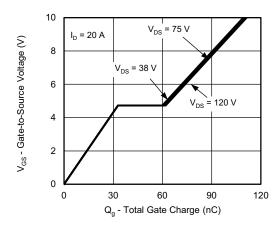




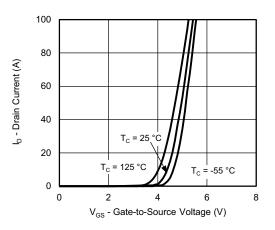
### **Output Characteristics**



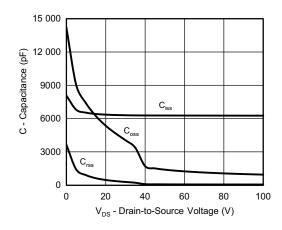
On-Resistance vs. Drain Current and Gate Voltage



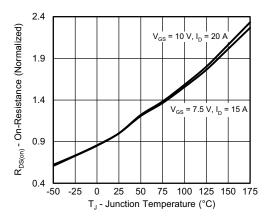
**Gate Charge** 



**Transfer Characteristics** 

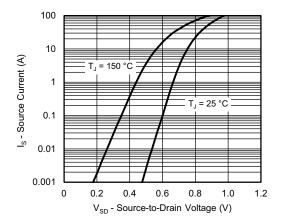


Capacitance

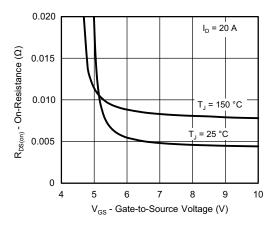


**On-Resistance vs. Junction Temperature** 

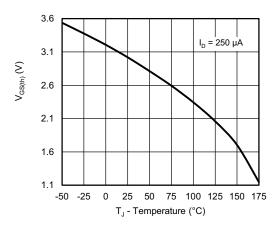




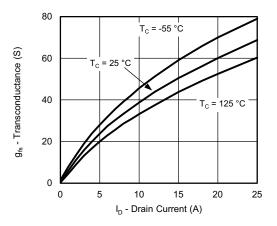
Source-Drain Diode Forward Voltage



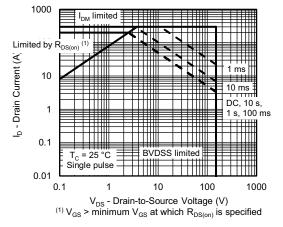
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

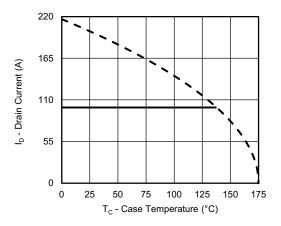


Transconductance

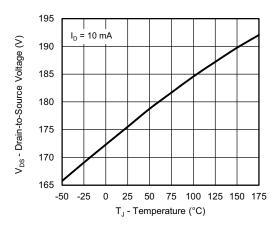


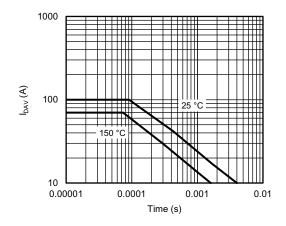
Safe Operating Area, Junction-to-Ambient





## Current Derating a



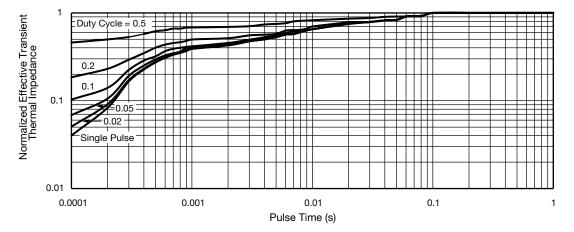


Drain Source Breakdown vs. Junction Temperature

 $I_{\text{DAV}}$  vs. Time

#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75186.

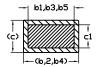


# **TO-247AC (High Voltage)**

### **VERSION 1: FACILITY CODE = 9**







Section C--C,D--D,E--E

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
Α	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØΡ	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	
L		I	1

#### Notes

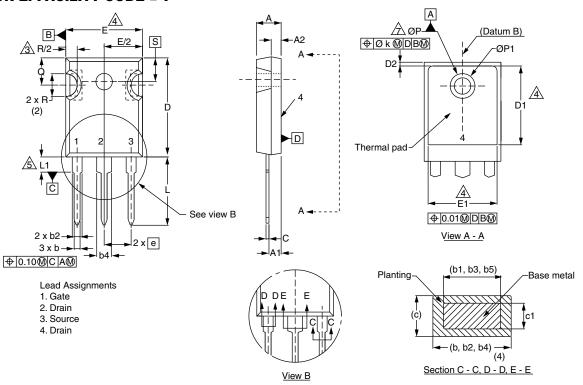
- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

Revision: 19-Oct-2020 1 Document Number: 91360

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### **VERSION 2: FACILITY CODE = Y**



	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
Е	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	0.254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

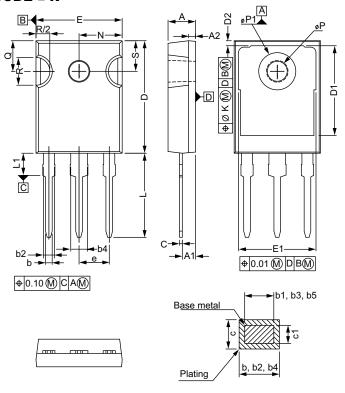
#### **Notes**

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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## **VERSION 3: FACILITY CODE = N**



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	4.65	5.31	
A1	2.21	2.59	
A2	1.17	1.37	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.65	2.39	
b3	1.65	2.34	
b4	2.59	3.43	
b5	2.59	3.38	
С	0.38	0.89	
c1	0.38	0.84	
D	19.71	20.70	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46	BSC	
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62	BSC	
Р	3.56	3.66	
P1	=	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E20-0545-Rev. F, 19-Oct-2020

DWG: 5971

#### Notes

- <sup>(1)</sup> Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")

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