



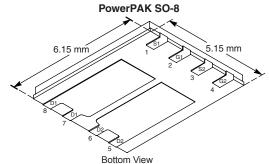
Dual N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
40	$0.0165 \text{ at V}_{GS} = 10 \text{ V}$	11.3		
	0.020 at V _{GS} = 4.5 V	10.3		

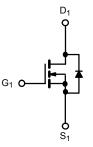
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package
- Dual MOSFET for Space Savings

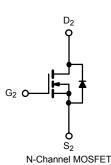




Ordering Information: Si7958DP-T1-E3 (Lead (Pb)-free) Si7958DP-T1-GE3 (Lead (Pb)-free and Halogen-free)







ABSOLUTE MAXIMUM RATINGS T	$A = 25 ^{\circ}C$, unles	ss otherwise n	oted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	40		V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I _D	11.3	7.2	
Continuous Drain Current (1) = 150 °C)	T _A = 70 °C		9.0	5.8	
Pulsed Drain Current		I _{DM}	40		Α
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.2	
Single Avalanche Current	L = 0.1 mH	I _{AS}	35		
Single Avalanche Energy		E _{AS}	61		mJ
Maximum Dawar Dissipation	T _A = 25 °C	P _D	3.5	1.4	w
Maximum Power Dissipation ^a	T _A = 70 °C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150 260		°C
Soldering Recommendations (Peak Temperature)b, c					

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	26	35	°C/W
Maximum Junction-to-Ambient	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.2	2.7	

Notes

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

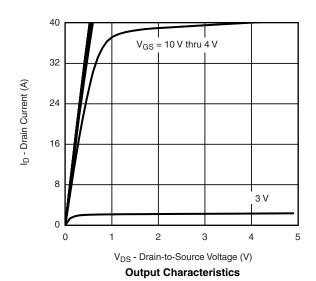
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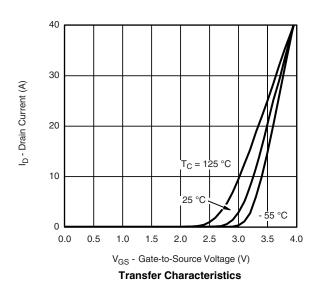


SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.		Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1		
		V_{DS} = 40 V, V_{GS} = 0 V, T_{J} = 55 °C			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a	В	V _{GS} = 10 V, I _D = 11.3 A		0.013	0.0165		
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 10.3 \text{ A}$	0.016		0.020	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 11.3 A		30		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Dynamic ^b			•				
Total Gate Charge	Q_g			50	75		
Gate-Source Charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 11.3 \text{ A}$		8.8		nC	
Gate-Drain Charge	Q_{gd}			10.4			
Gate Resistance	R_{g}	f = 1 MHz		1.9		Ω	
Turn-On Delay Time	t _{d(on)}			17	30		
Rise Time	t _r	V_{DD} = 20 V, R_L = 20 Ω		17	30		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		66	100	ns	
Fall Time	t _f			17	30		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, dI/dt = 100 A/μs		31	60		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



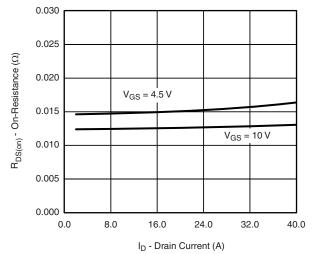


Notes: a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.

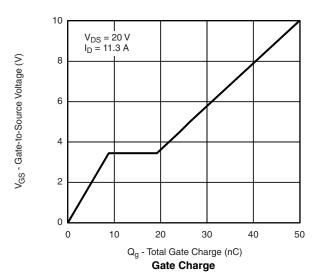


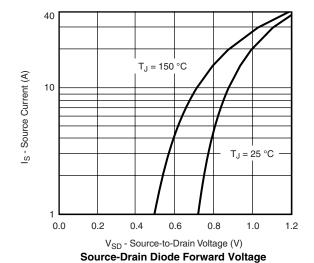


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



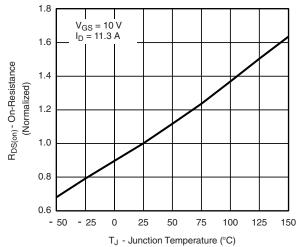
On-Resistance vs. Drain Current



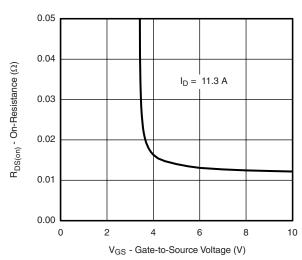


4000 3500 3000 $\mathsf{C}_{\mathsf{iss}}$ C - Capacitance (pF) 2500 2000 1500 1000 Coss C_{rss} 500 0 0 8 16 24 40

V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



On-Resistance vs. Junction Temperature

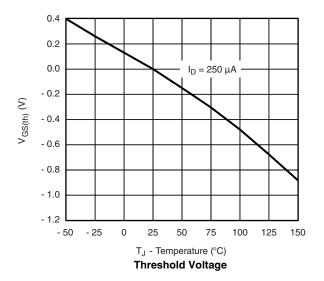


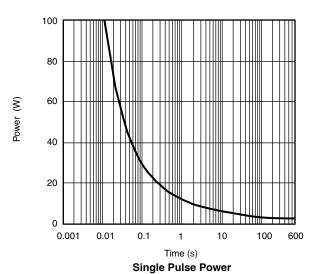
On-Resistance vs. Gate-to-Source Voltage

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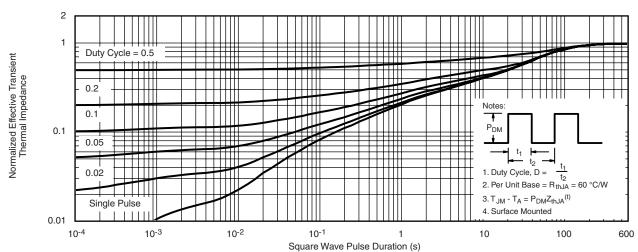
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





100 I_{DM} Limited Limited by R_{DS(on)} 100 μs I_D - Drain Current (A) 10 ms 100 ms 1 s T_A = 25 °C 0.1 Single Pulse 10 s DC **BVDSS Limited** 0.01 0.1 V_{DS} - Drain-to-Source Voltage (V)

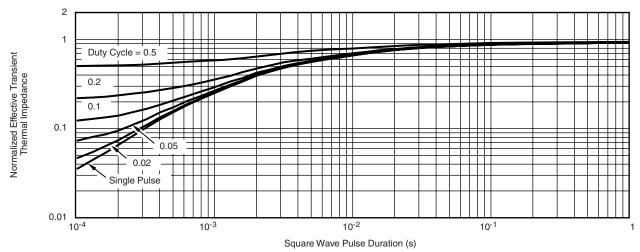
 * V_{GS} > minimum V_{GS} at which R _{DS(on)} is specified **Safe Operating Area, Junction-to-Ambient**



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

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