



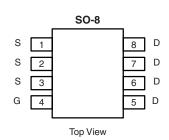
N-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	
80	0.035 at V _{GS} = 10 V	6.0	
	0.040 at V _{GS} = 6.0 V	5.5	

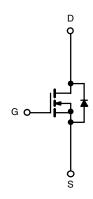
FEATURES

- Halogen-free According to IEC 61249-2-21 Definiton
- Compliant to RoHS Directive 2002/95/EC





Ordering Information: Si4480DY-T1-E3 (Lead (Pb)-free) Si4480DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	80	V	
Gate-Source Voltage		V _{GS}	± 20	 	
Continuous Drain Current /T 150 °C\a	T _A = 25 °C	I _D	6.0		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		4.8		
Pulsed Drain Current		I _{DM}	40	Α Α	
Continuous Source Current (Diode Conduction) ^a		I _S	2.1		
M	T _A = 25 °C	P _D	2.5	w	
Maximum Power Dissipation ^a	T _A = 70 °C	l D	1.6	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	50	°C/W	

a. Surface Mounted on FR4 board, $t \le 10 \text{ s.}$

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Parameter	Symbol	Test Conditions	Min.	Typ. ^b	Max.	Unit	
Static			•	•			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μΑ	
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			20		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 6.0 A		0.026	0.035		
		$V_{GS} = 6.0 \text{ V}, I_D = 5.5 \text{ A}$		0.030	0.040	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 6.0 \text{ A}$		25		S	
Diode Forward Voltage ^a	V _{SD}	$I_S = 2.1 \text{ A}, V_{GS} = 0 \text{ V}$			1.2	V	
Dynamic ^b	L L		·	·			
Total Gate Charge	Qg			30	50		
Gate-Source Charge	Q_{gs}	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 6.0 \text{ A}$		9		nC	
Gate-Drain Charge	Q_{gd}			5.6			
Gate Resistance	R_g		1.5		4.0	Ω	
Turn-On Delay Time	t _{d(on)}			12.5	25		
Rise Time	t _r	V_{DD} = 40 V, R_L = 30 Ω		12.5	25	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		52	80		
Fall Time	t _f			22	40		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.1 A, dI/dt = 100 A/μs		50	80		

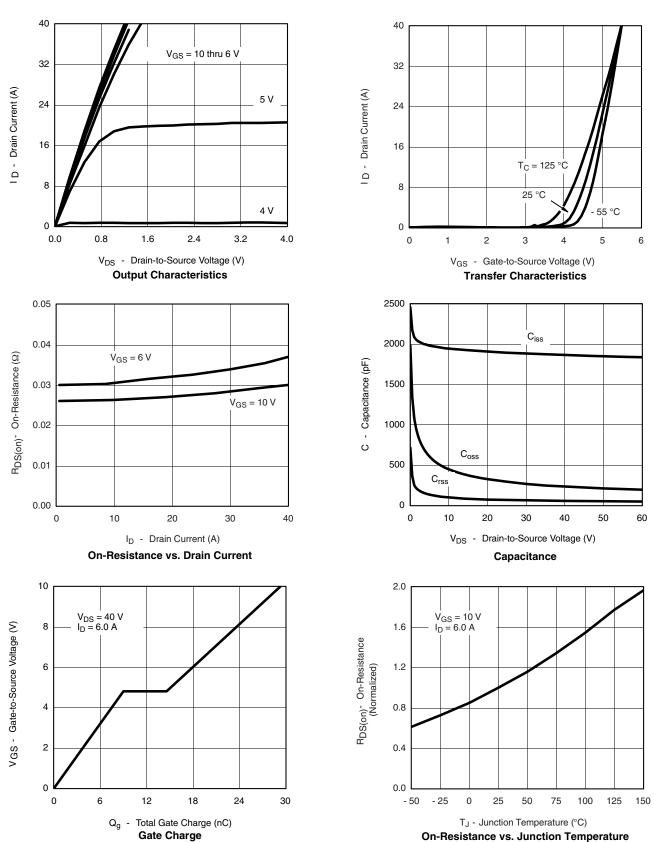
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. For design aid only; not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



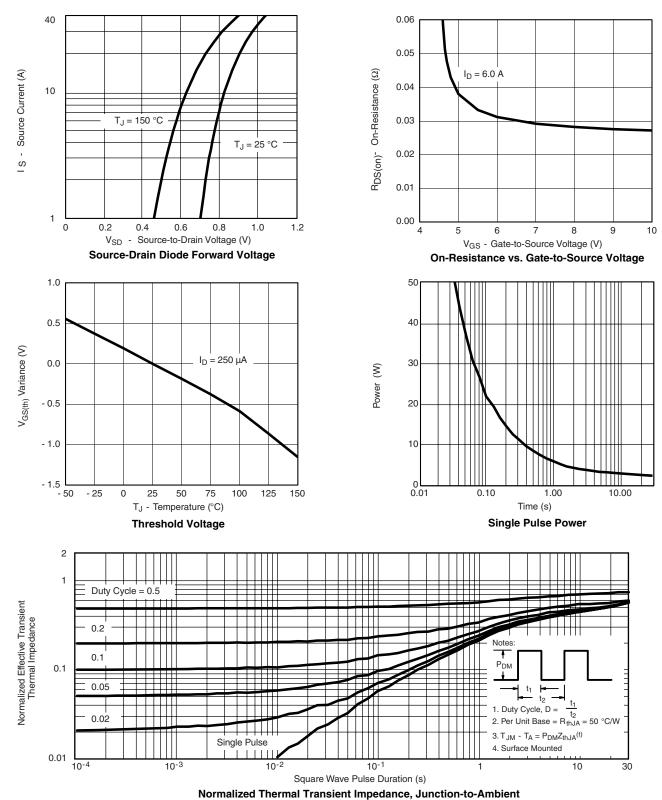
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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