

Power MOSFET



N-Channel MOSFET

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V, V_{GS} rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Extremely high frequency operation
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

This new series of low charge power MOSFETs achieve significantly lower gate charge over conventional Power MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge power MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of power MOSFETs offer the designer a new standard in power transistors for switching applications.

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 1.2
Q_g max. (nC)	39
Q_{gs} (nC)	10
Q_{gd} (nC)	19
Configuration	Single

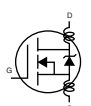

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFBC40LCPbF
Lead (Pb)-free and halogen-free	IRFBC40LCPbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current	I_D	V_{GS} at 10 V $T_C = 25\text{ }^\circ\text{C}$	6.2
		$T_C = 100\text{ }^\circ\text{C}$	3.9
Pulsed drain current ^a	I_{DM}	25	A
Linear derating factor		1.0	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	530	mJ
Repetitive avalanche current ^a	I_{AR}	6.2	A
Repetitive avalanche energy ^a	E_{AR}	13	mJ
Maximum power dissipation	P_D	125	W
Peak diode recovery dV/dt ^c	dV/dt	3.0	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d		300	
Mounting torque	6-32 or M3 screw	For 10 s	10
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Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 25\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 6.2\text{ A}$ (see fig. 12)
- $I_{SD} \leq 6.2\text{ A}$, $dI/dt \leq 80\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.70	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	100	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.7\text{ A}^b$	-	-	1.2	Ω
Forward transconductance	g_{fs}	$V_{DS} = 100\text{ V}, I_D = 3.7\text{ A}^b$	3.7	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	1100	-	pF
Output capacitance	C_{oss}		-	140	-	
Reverse transfer capacitance	C_{rss}		-	15	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 6.2\text{ A}, V_{DS} = 360\text{ V}$, see fig. 6 and 13 ^b	-	-	39	nC
Gate-source charge	Q_{gs}		-	-	10	
Gate-drain charge	Q_{gd}		-	-	19	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 6.2\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 47\text{ }\Omega$, see fig. 10 ^b	-	12	-	ns
Rise time	t_r		-	20	-	
Turn-off delay time	$t_{d(off)}$		-	27	-	
Fall time	t_f		-	17	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain	0.6	-	3.9	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.2	A
Pulsed diode forward current ^a	I_{SM}		-	-	25	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 6.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 6.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	440	680	ns
Body diode reverse recovery charge	Q_{rr}		-	2.1	3.2	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

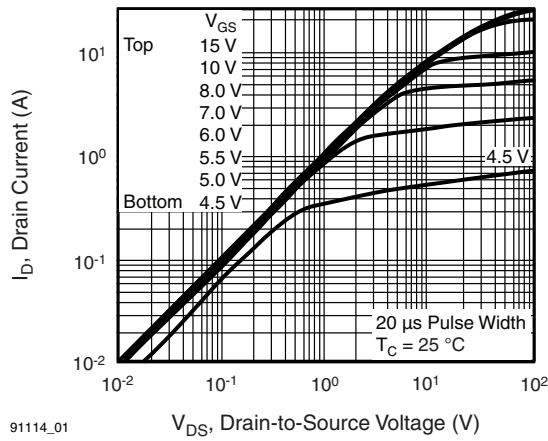


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

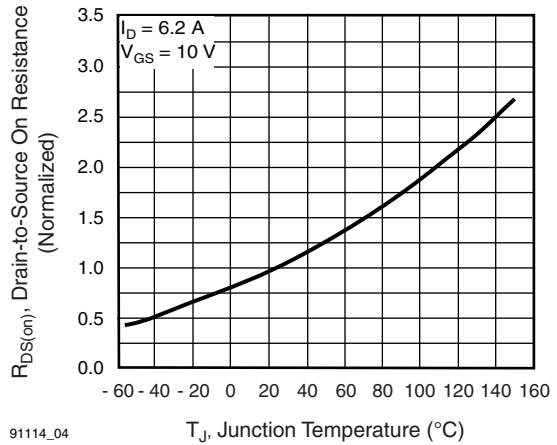


Fig. 4 - Normalized On-Resistance vs. Temperature

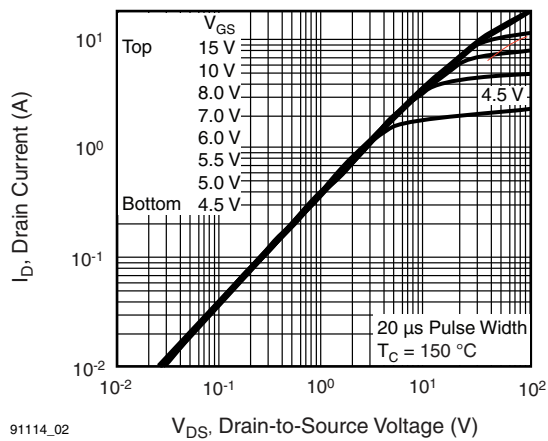


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

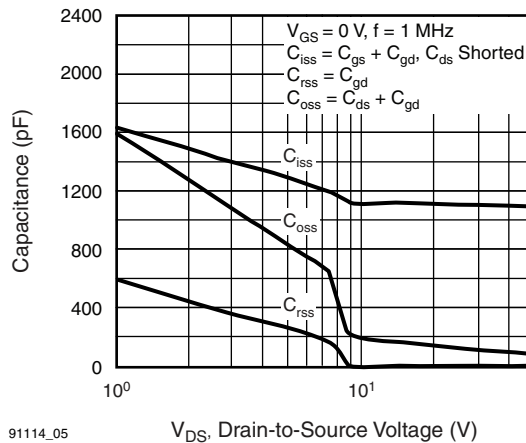


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

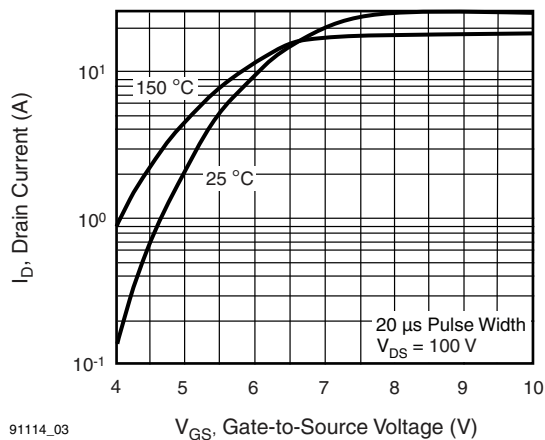


Fig. 3 - Typical Transfer Characteristics

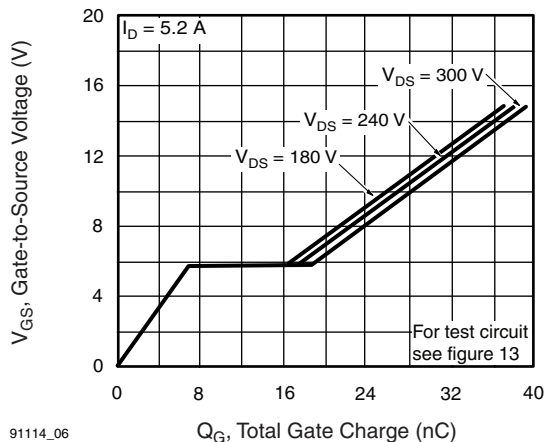
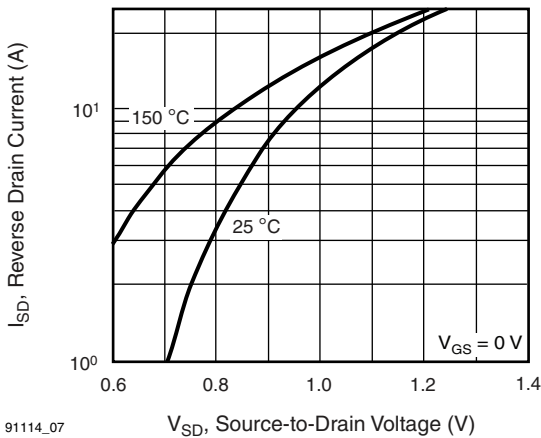
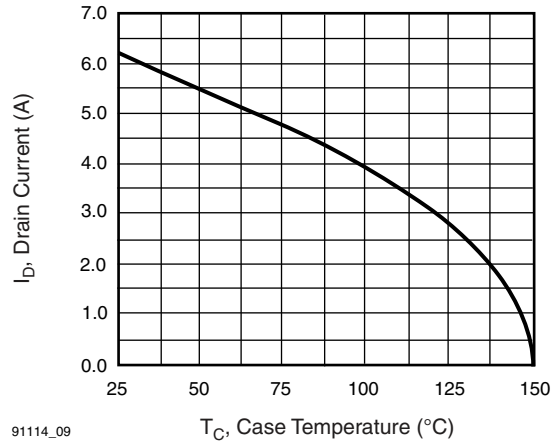


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



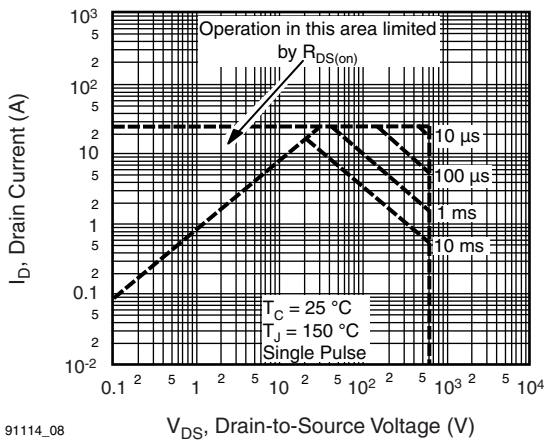
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

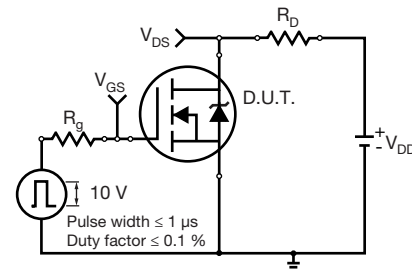


Fig. 10a - Switching Time Test Circuit

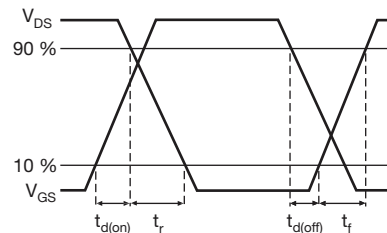
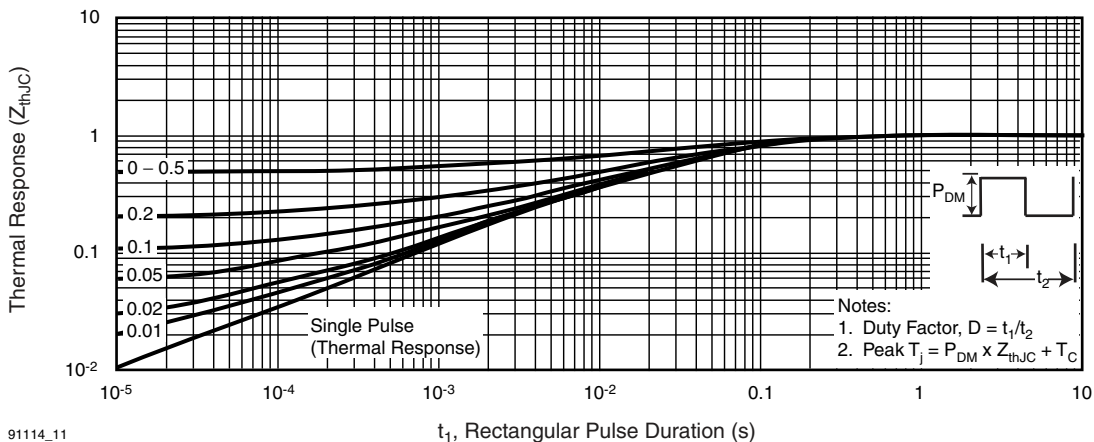


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

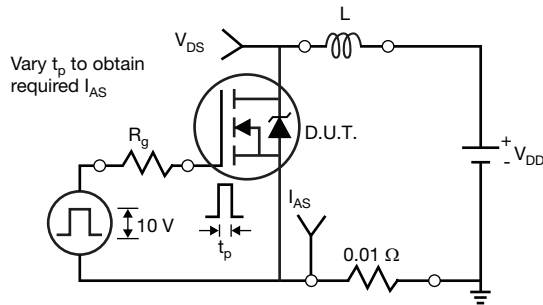


Fig. 12a - Unclamped Inductive Test Circuit

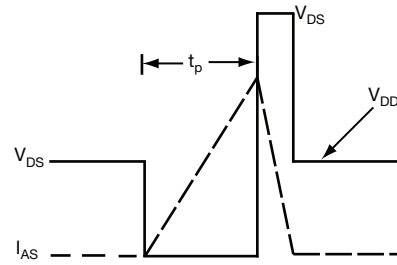


Fig. 12b - Unclamped Inductive Waveforms

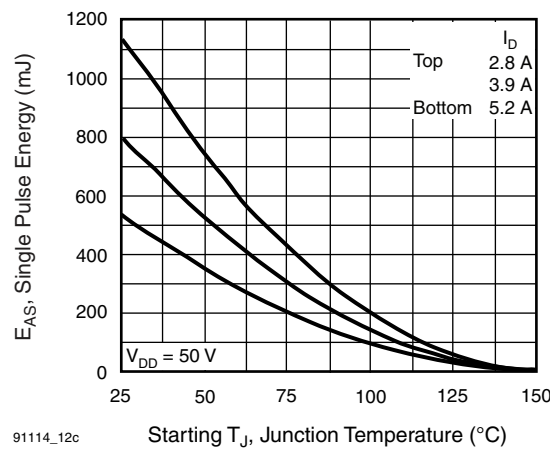


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

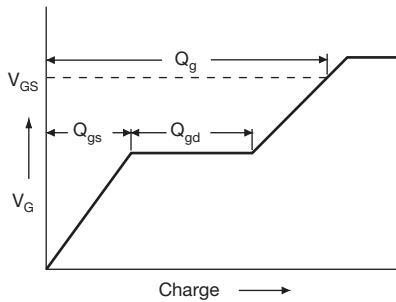


Fig. 13a - Basic Gate Charge Waveform

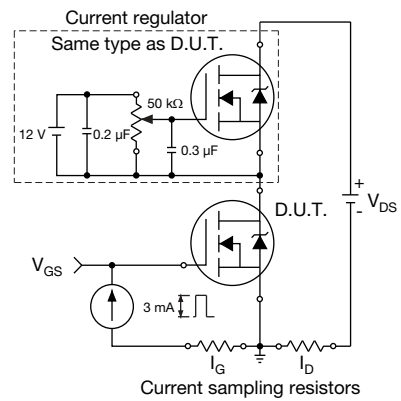


Fig. 13b - Gate Charge Test Circuit

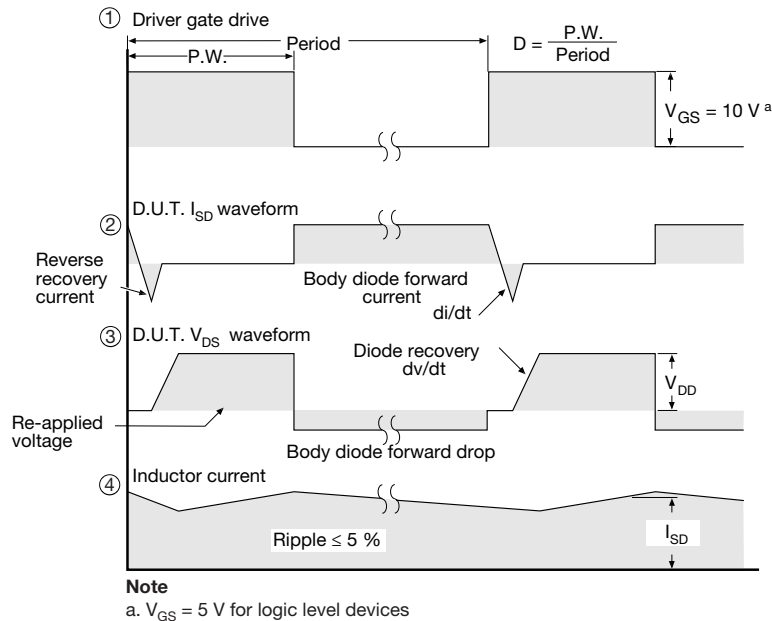
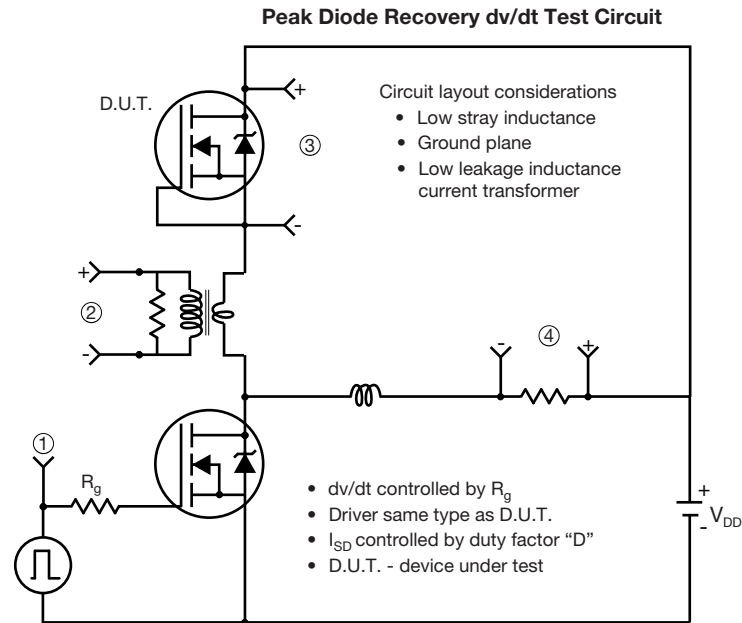


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M^* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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