

Complementary 30 V (D-S) MOSFET

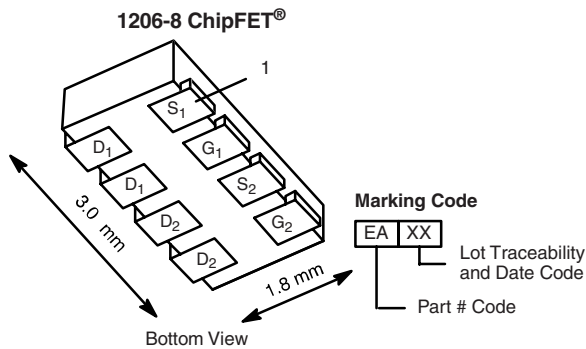
| PRODUCT SUMMARY | | | |
|-----------------|---------------------|------------------------------------|--------------------|
| | V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) |
| N-Channel | 30 | 0.085 at V _{GS} = 10 V | ± 3.9 |
| | | 0.143 at V _{GS} = 4.5 V | ± 3.0 |
| P-Channel | - 30 | 0.165 at V _{GS} = - 10 V | ± 2.8 |
| | | 0.290 at V _{GS} = - 4.5 V | ± 2.1 |

FEATURES

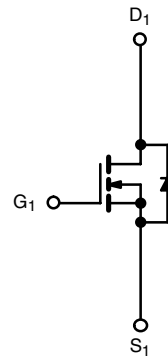
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC



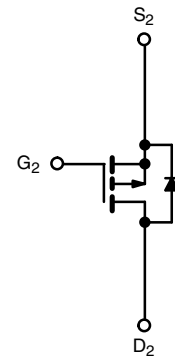
RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si5504DC-T1-E3 (Lead (Pb)-free)
Si5504DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



P-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | | | | |
|---|-----------------------------------|------------------------|--------------|-----------|--------------|-------|---|
| Parameter | Symbol | N-Channel | | P-Channel | | Unit | |
| | | 5 s | Steady State | 5 s | Steady State | | |
| Drain-Source Voltage | V _{DS} | 30 | | - 30 | | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | | | | |
| Continuous Drain Current (T _J = 150 °C) ^a | I _D | T _A = 25 °C | ± 3.9 | ± 2.9 | ± 2.8 | ± 2.1 | A |
| | | T _A = 85 °C | ± 2.8 | ± 2.1 | ± 2.0 | ± 1.5 | |
| Pulsed Drain Current | I _{DM} | ± 10 | | | | A | |
| Continuous Source Current (Diode Conduction) ^a | I _S | 1.8 | 0.9 | - 1.8 | - 0.9 | | |
| Maximum Power Dissipation ^a | P _D | T _A = 25 °C | 2.1 | 1.1 | 2.1 | 1.1 | W |
| | | T _A = 85 °C | 1.1 | 0.6 | 1.1 | 0.6 | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | | | | °C | |
| Soldering Recommendations (Peak Temperature) ^{b, c} | | 260 | | | | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|--------------|-------------------|---------|---------|------|
| Parameter | | Symbol | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient ^a | t ≤ 5 s | R _{thJA} | 50 | 60 | °C/W |
| | Steady State | | 90 | 110 | |
| Maximum Junction-to-Foot (Drain) | Steady State | R _{thJF} | 30 | 40 | |

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See reliability manual for profile. The ChipFET/PowerPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

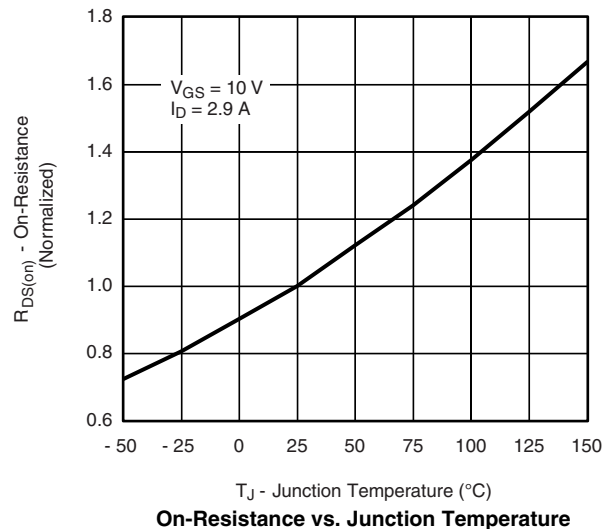
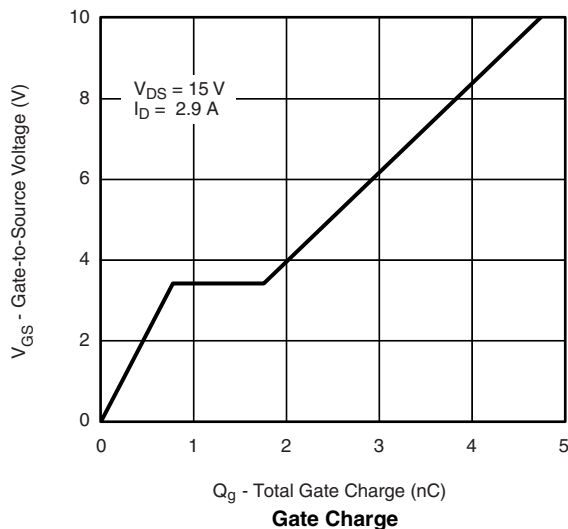
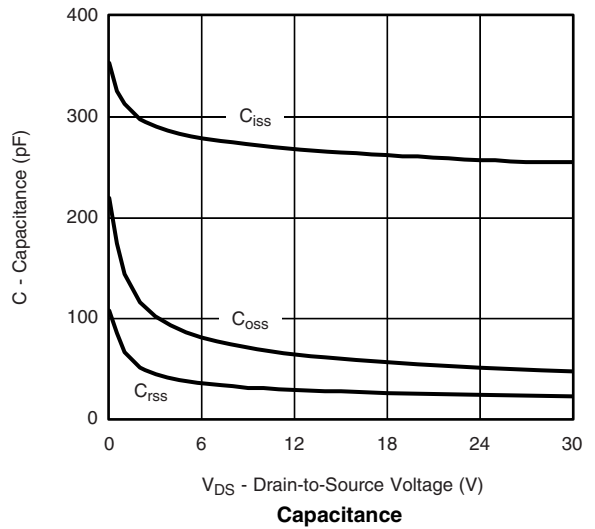
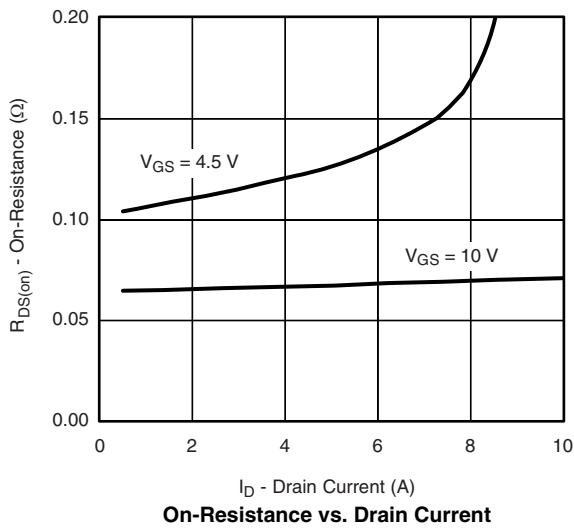
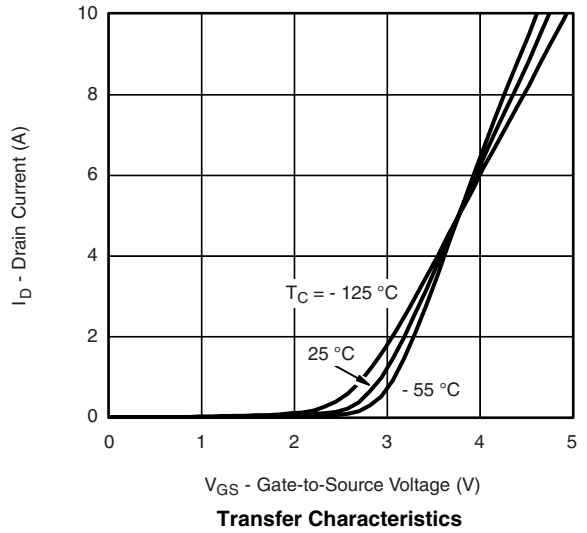
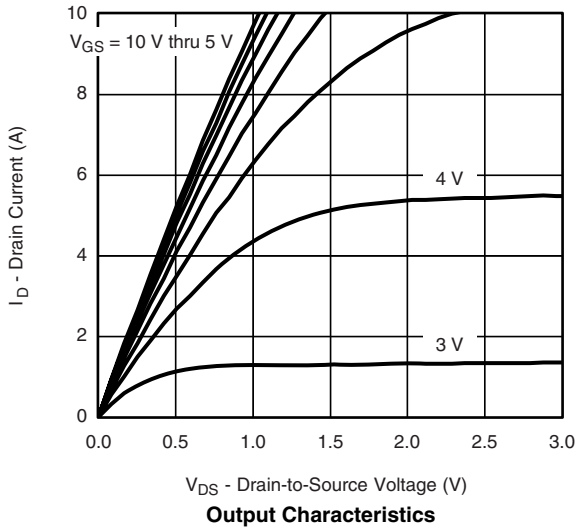
| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | | |
|--|--------------|--|--------------|------|-------|------------------------|---------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit | |
| Static | | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | N-Ch | 1.0 | | | V |
| | | $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$ | P-Ch | -1.0 | | | |
| Gate-Body Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | N-Ch P-Ch | | | ± 100 ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ | N-Ch | | | 1 | μA |
| | | $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$ | P-Ch | | | -1 | |
| | | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$ | N-Ch | | | 5 | |
| | | $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$ | P-Ch | | | -5 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$ | N-Ch | 10 | | | A |
| | | $V_{DS} \leq -5\text{ V}, V_{GS} = -10\text{ V}$ | P-Ch | -10 | | | |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 2.9\text{ A}$ | N-Ch | | 0.072 | 0.085 | Ω |
| | | $V_{GS} = -10\text{ V}, I_D = -2.1\text{ A}$ | P-Ch | | 0.137 | 0.165 | |
| | | $V_{GS} = 4.5\text{ V}, I_D = 2.2\text{ A}$ | N-Ch | | 0.120 | 0.143 | |
| | | $V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}$ | P-Ch | | 0.240 | 0.290 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 2.9\text{ A}$ | N-Ch | | 6 | | S |
| | | $V_{DS} = -15\text{ V}, I_D = -2.1\text{ A}$ | P-Ch | | 3 | | |
| Diode Forward Voltage ^a | V_{SD} | $I_S = 0.9\text{ A}, V_{GS} = 0\text{ V}$ | N-Ch | | 0.8 | 1.2 | V |
| | | $I_S = -0.9\text{ A}, V_{GS} = 0\text{ V}$ | P-Ch | | -0.8 | -1.2 | |
| Dynamic^b | | | | | | | |
| Total Gate Charge | Q_g | N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 2.9\text{ A}$ | N-Ch | | 5 | 7.5 | nC |
| Gate-Source Charge | Q_{gs} | | P-Ch | | 5.5 | 6.6 | |
| Gate-Drain Charge | Q_{gd} | P-Channel $V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -2.1\text{ A}$ | N-Ch | | 0.8 | | |
| | | | P-Ch | | 1.2 | | |
| Turn-On Delay Time | $t_{d(on)}$ | N-Channel $V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$ | N-Ch | | 7 | 11 | ns |
| | | | P-Ch | | 8 | 12 | |
| Rise Time | t_r | P-Channel $V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 6\text{ }\Omega$ | N-Ch | | 12 | 18 | |
| | | | P-Ch | | 11 | 18 | |
| Turn-Off Delay Time | $t_{d(off)}$ | N-Channel $V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 6\text{ }\Omega$ | N-Ch | | 12 | 18 | |
| | | | P-Ch | | 14 | 21 | |
| Fall Time | t_f | P-Channel $V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 6\text{ }\Omega$ | N-Ch | | 7 | 11 | |
| | | | P-Ch | | 8 | 12 | |
| Source-Drain Reverse Recovery Time | t_{rr} | $I_F = 0.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch | | 40 | 80 | |
| | | $I_F = -0.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | P-Ch | | 40 | 80 | |

Notes:

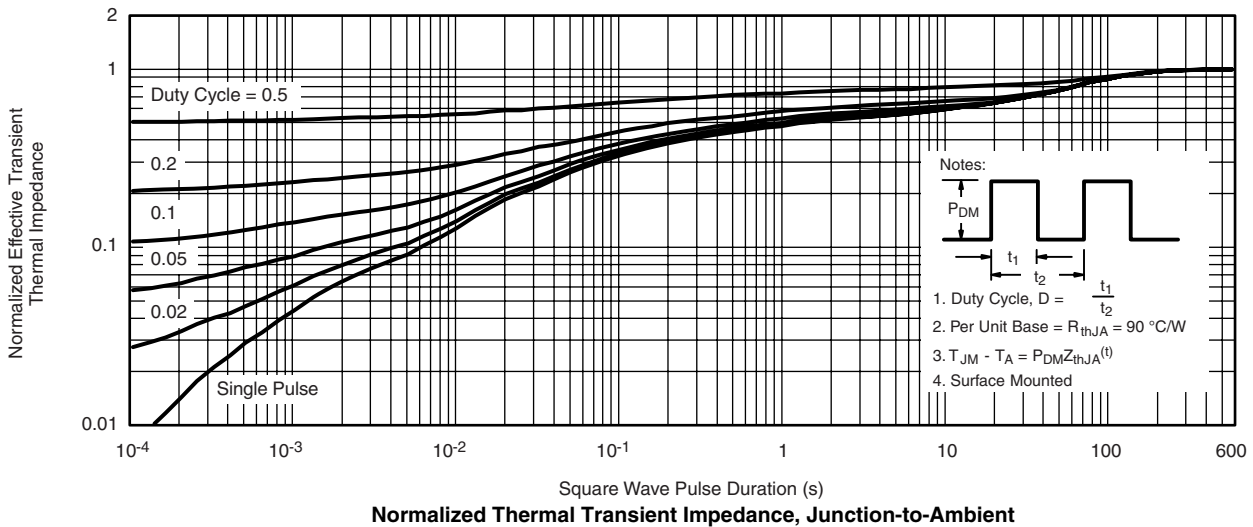
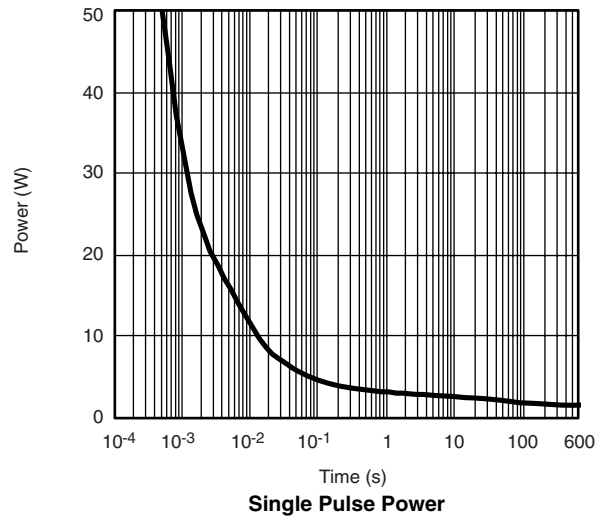
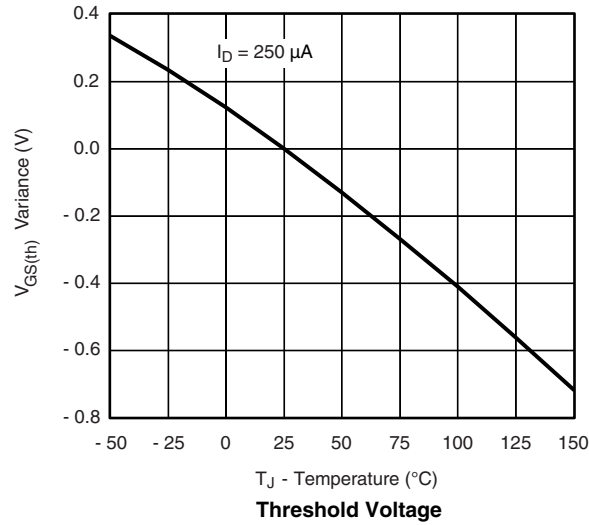
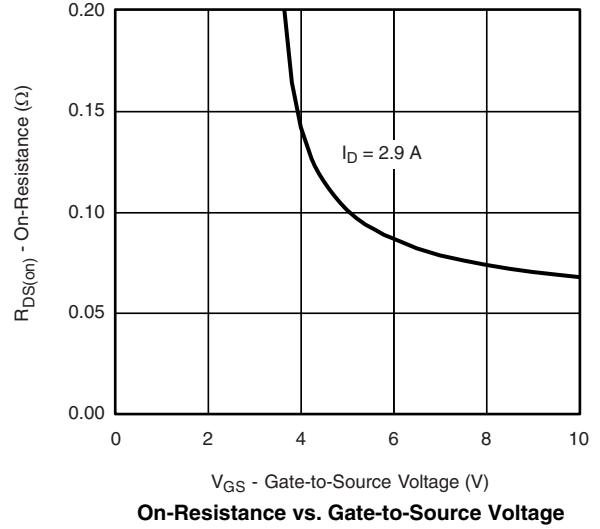
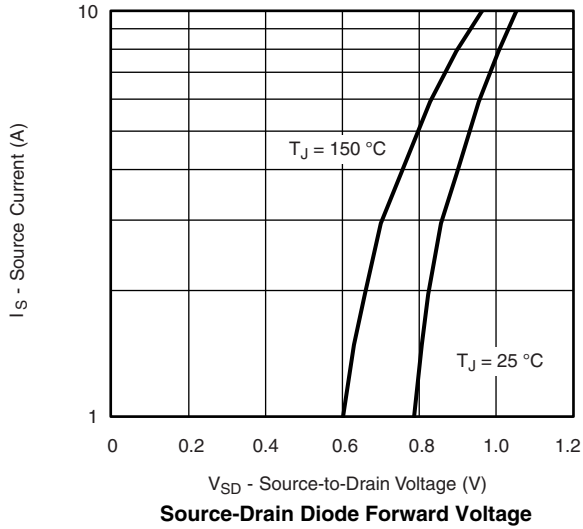
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

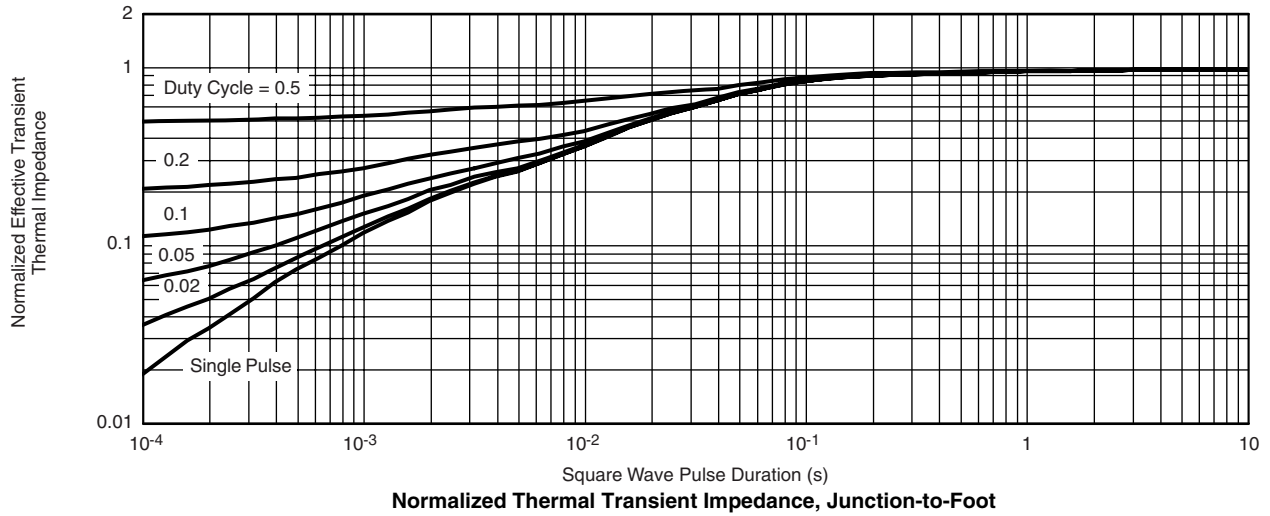
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



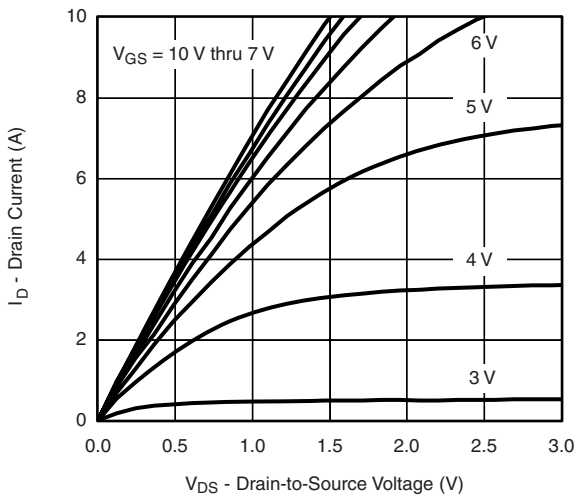
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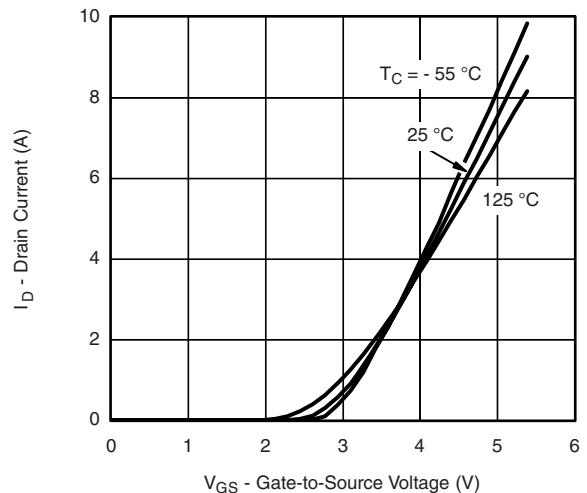
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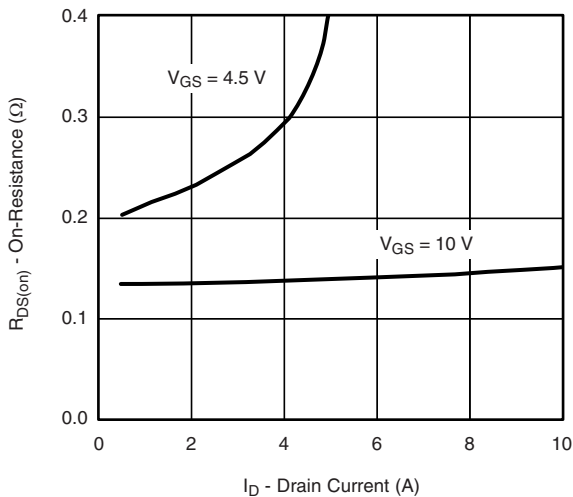
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



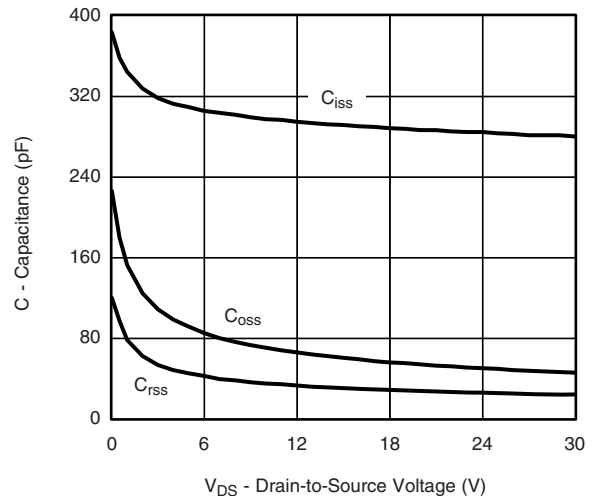
Output Characteristics



Transfer Characteristics

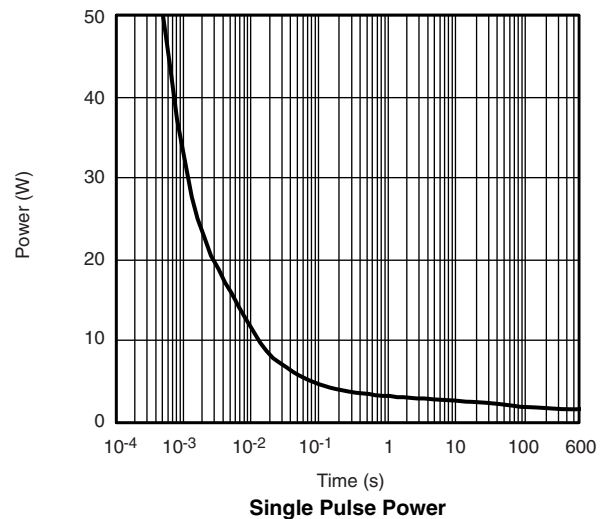
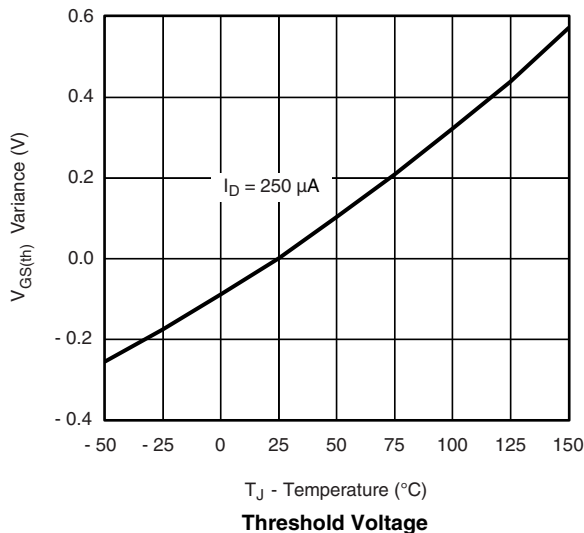
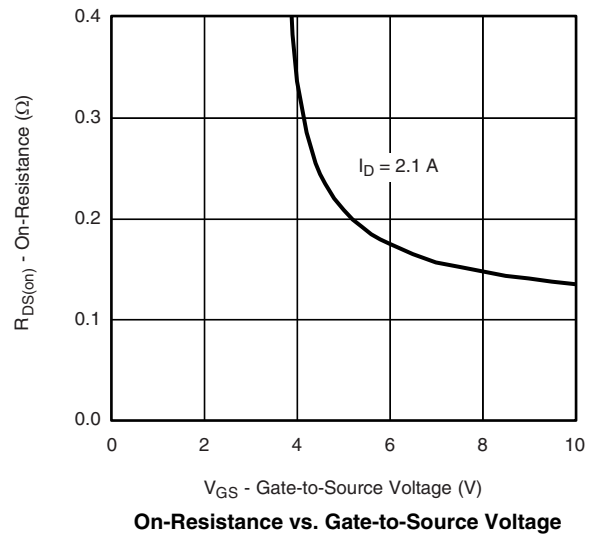
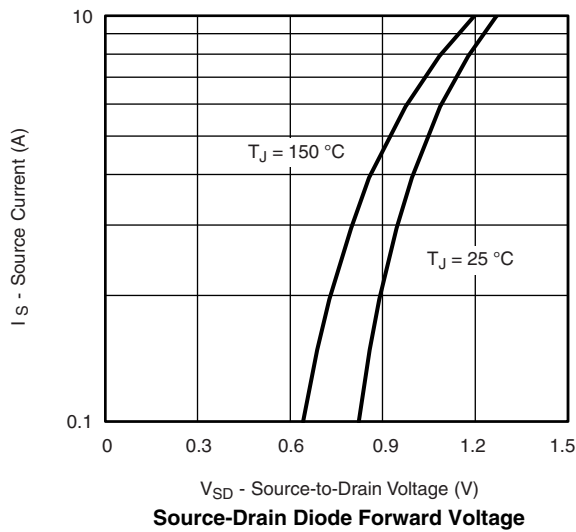
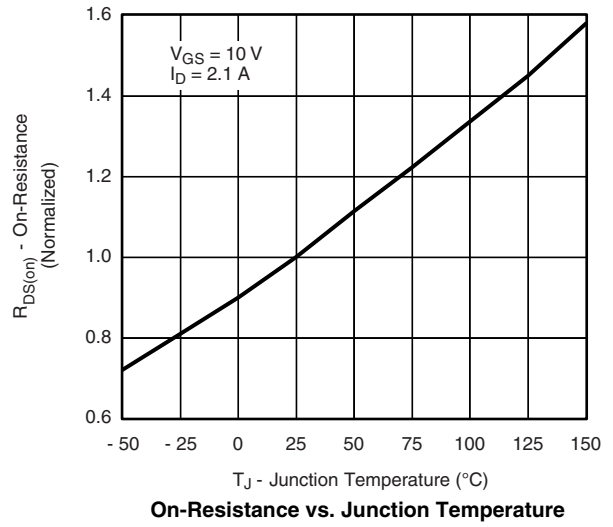
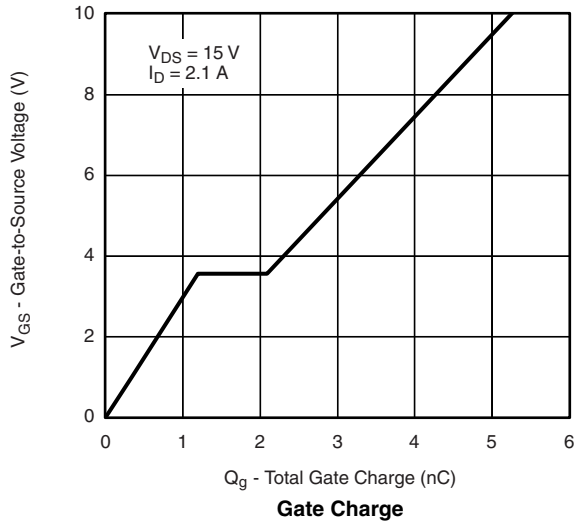


On-Resistance vs. Drain Current

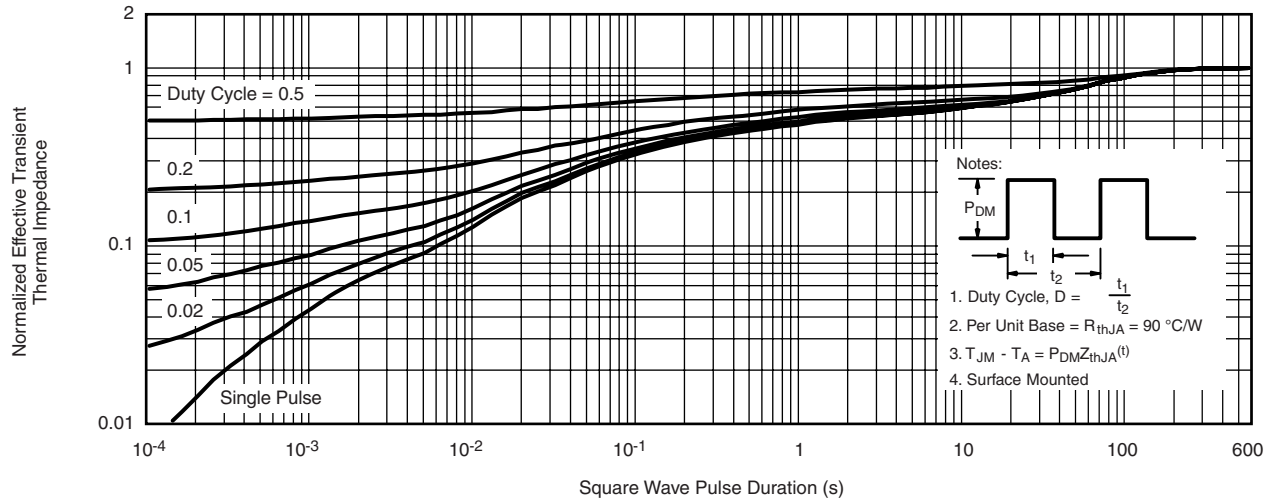


Capacitance

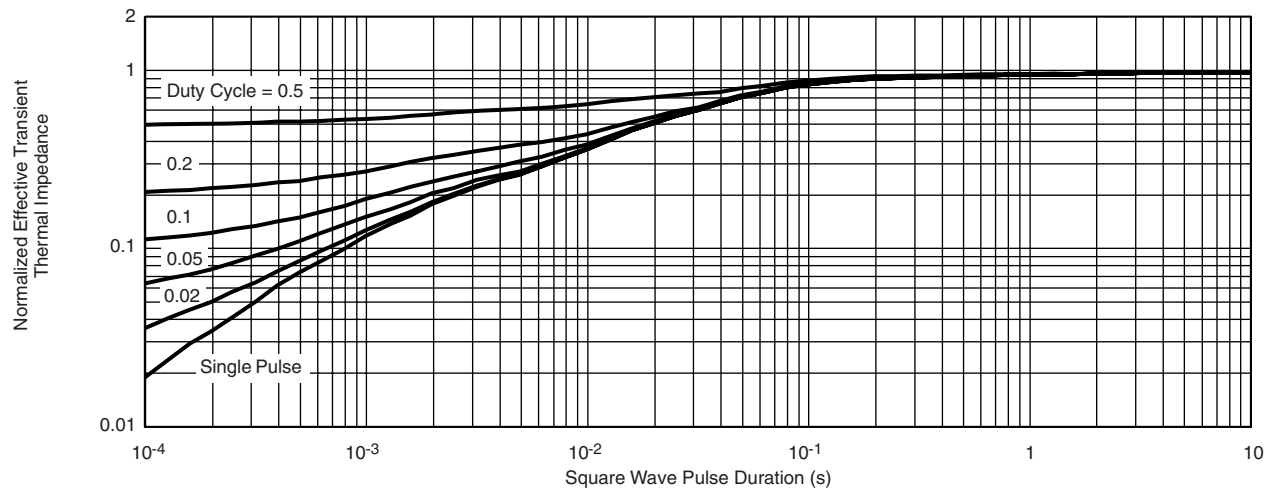
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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