

Vishay Siliconix

# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)		
30	0.050 at V <sub>GS</sub> = 10 V	3.4		
	0.085 at V <sub>GS</sub> = 4.5 V	2.6		

## **FEATURES**

- Halogen-free Option Available
- TrenchFET<sup>®</sup> Power MOSFET

### **APPLICATIONS**

· Battery Switch



COMPLIANT

## **TO-236** (SOT-23) G 1 3 D S 2 Top View

Si2316DS (C6)\* \* Marking Code

Ordering Information: Si2316DS-T1 Si2316DS-T1-E3 (Lead (Pb)-free) Si2316DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	Γ <sub>A</sub> = 25 °C, unles	ss otherwise n	oted		
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		
	T <sub>A</sub> = 25 °C	– I <sub>D</sub>	3.4	2.9	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a, b</sup>	T <sub>A</sub> = 70 °C		2.7	2.3	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	16		A
Continuous Source Current (Diode Conduction) <sup>a, b</sup>		۱ <sub>S</sub>	0.8		
Dura Dia ing ing h	T <sub>A</sub> = 25 °C	P	0.96 0.7		W
Power Dissipation <sup>a, b</sup>	T <sub>A</sub> = 70 °C	P <sub>D</sub>	0.6	0.45	vv
Operating Junction and Storage Temperature Rang	T <sub>J</sub> , T <sub>stg</sub>	- 55	to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
	t ≤ 5 s	R <sub>thJA</sub>	100	130	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	' 'thJA	140	175	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	60	75	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Pulse width limited by maximum junction temperature.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

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	Symbol		Limits				
Parameter		Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS}$ = 0 V, $I_D$ = 250 $\mu$ A	30			v	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	0.8			v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zaus Oata Maltana Dusin Ouwant	1	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	= 0 V		0.5		
Zero Gate Voltage Drain Current	DSS	$V_{DS}$ = 30 V, $V_{GS}$ = 0 V, $T_{J}$ = 55 °C			10	μΑ	
		$V_{DS} \geq 4.5$ V, $V_{GS}$ = 10 V	6			A	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 4.5$ V, $V_{GS} = 4.5$ V	4				
	Р	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 3.4 \text{ A}$		0.042	0.050	Ω	
Drain-Source On-Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 2.6 \text{ A}$		0.068	0.085		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 4.5 \text{ V}, I_{D} = 3.4 \text{ A}$		6.0		S	
Diode Forward Voltage	V <sub>SD</sub>	$I_{S} = 0.8 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Dynamic <sup>b</sup>			•	•			
Total Gate Charge	Qg			4.3	7	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_{D}$ = 3.4 A		0.65			
Gate-Drain Charge	Q <sub>gd</sub>			1.2		1	
Input Capacitance	C <sub>iss</sub>			215			
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz		90		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			55		1	
Switching							
Turn-On Delay Time	t <sub>d(on)</sub>			9	15	-	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		9	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ 1.0 A, $V_{GEN}$ = 10 V, $R_G$ = 6 $\Omega$		14	20	ns	
Fall Time	t <sub>f</sub>			6	12		

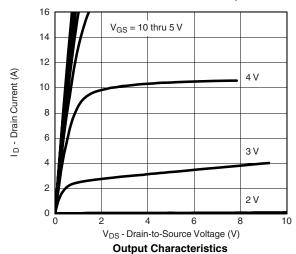
Notes:

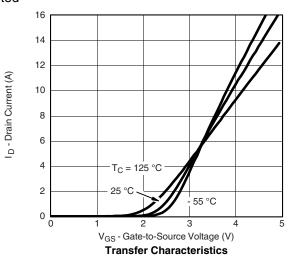
a. Pulse test; PW  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

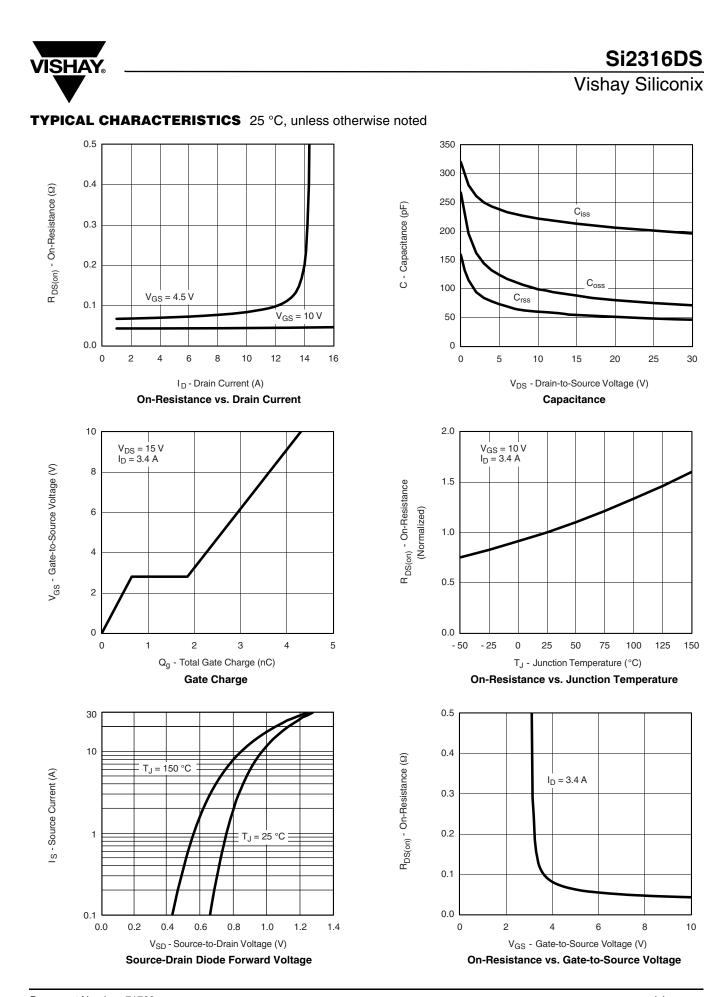
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





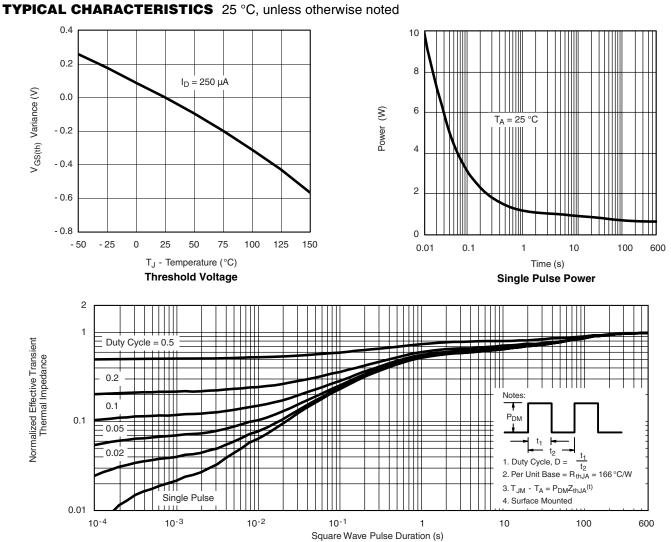
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# Si2316DS

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#### Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71798.

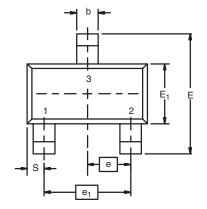
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# Package Information

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## SOT-23 (TO-236): 3-LEAD







Dim	MILLIM	IETERS	INCHES			
	Min	Мах	Min	Мах		
Α	0.89	1.12	0.035	0.044		
A <sub>1</sub>	0.01	0.10	0.0004	0.004		
A <sub>2</sub>	0.88	1.02	0.0346	0.040		
b	0.35	0.50	0.014	0.020		
С	0.085	0.18	0.003	0.007		
D	2.80	3.04	0.110	0.120		
E	2.10	2.64	0.083	0.104		
E <sub>1</sub>	1.20	1.40	0.047	0.055		
е	0.95 BSC		0.0374 Ref			
e <sub>1</sub>	1.90 BSC		0.0748 Ref			
L	0.40	0.60	0.016	0.024		
L <sub>1</sub>	0.64 Ref		0.025 Ref			
S	0.50 Ref		0.020	0.020 Ref		
q	3°	8°	3°	8°		
ECN: S-03946-Rev. K, 09- DWG: 5479	Jul-01					



# Application Note 826

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## **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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