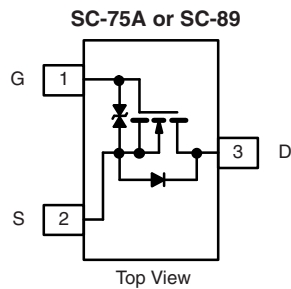


N-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (mA)
20	0.70 at $V_{GS} = 4.5$ V	600
	0.85 at $V_{GS} = 2.5$ V	500
	1.25 at $V_{GS} = 1.8$ V	350



ORDERING INFORMATION		
Part Number	Package	Marking Code
Si1012R-T1-GE3 (Lead (Pb)-free and Halogen-free)	SC-75A (SOT-416)	C
Si1012X-T1-GE3 (Lead (Pb)-free and Halogen-free)	SC-89 (SOT-490)	A

FEATURES

- TrenchFET[®] Power MOSFET: 1.8 V Rated
- Gate-Source ESD Protected: 2000 V
- High-Side Switching
- Low On-Resistance: 0.7 Ω
- Low Threshold: 0.8 V (typ.)
- Fast Switching Speed: 10 ns
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 6			
Continuous Drain Current ($T_J = 150$ °C) ^b	I_D	$T_A = 25$ °C	600	500	mA
		$T_A = 85$ °C	400	350	
Pulsed Drain Current ^a	I_{DM}	1000			
Continuous Source Current (Diode Conduction) ^b	I_S	275	250		
Maximum Power Dissipation ^b for SC-75	P_D	$T_A = 25$ °C	175	150	mW
		$T_A = 85$ °C	90	80	
Maximum Power Dissipation ^b for SC-89	P_D	$T_A = 25$ °C	275	250	
		$T_A = 85$ °C	160	140	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000		V	

Notes:

- Pulse width limited by maximum junction temperature.
- Surface mounted on FR4 board.

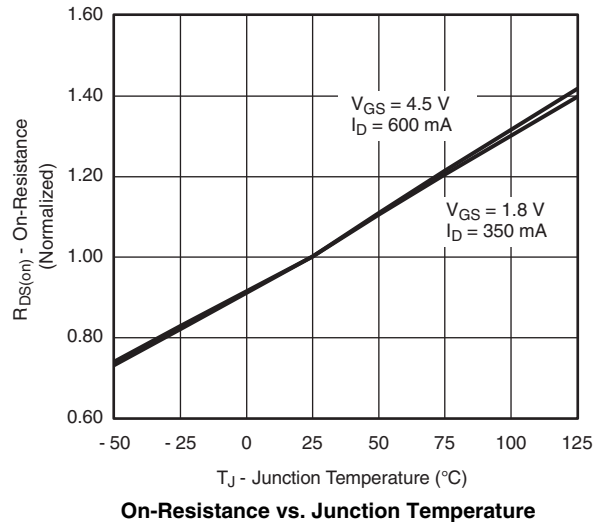
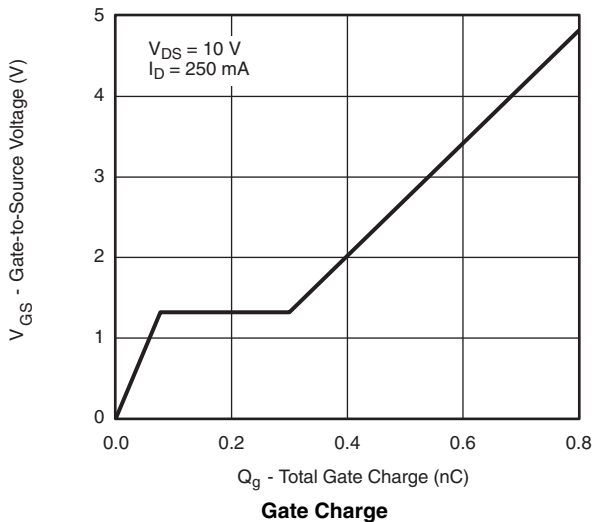
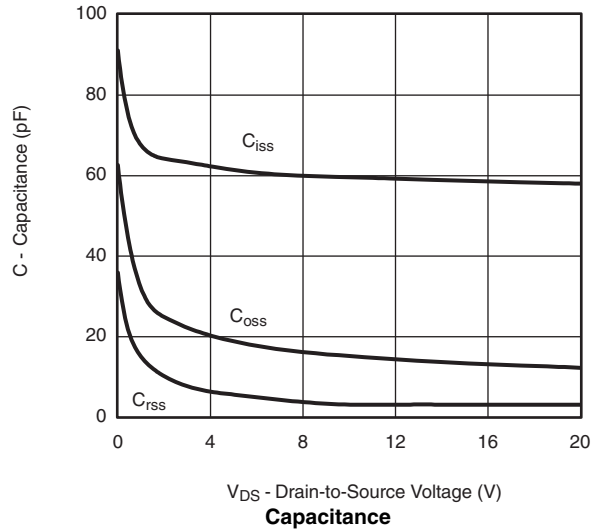
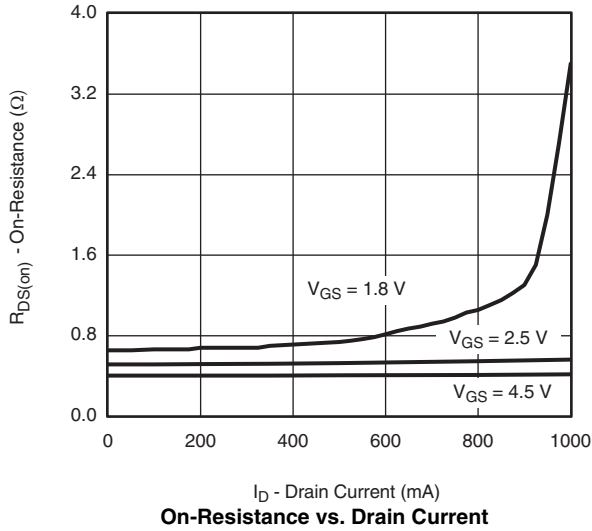
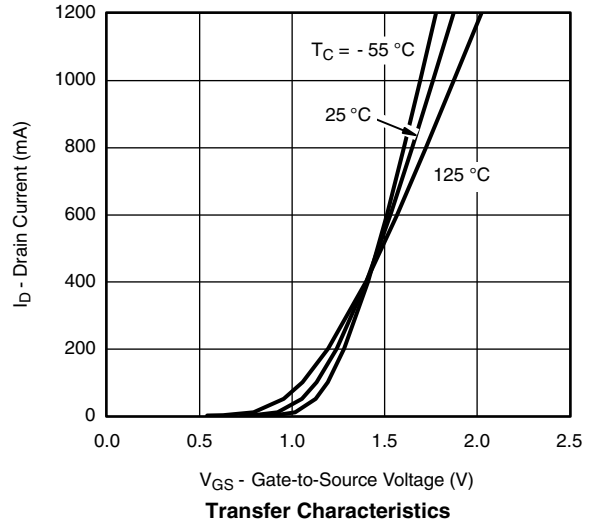
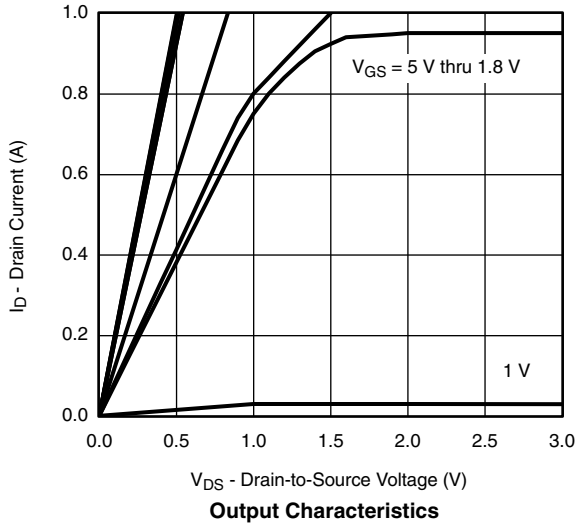
SPECIFICATIONS (T _A = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.45		0.9	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V		± 0.5	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V		0.3	100	nA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85 °C			5	μA
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	700			mA
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 600 mA		0.41	0.70	Ω
		V _{GS} = 2.5 V, I _D = 500 mA		0.53	0.85	
		V _{GS} = 1.8 V, I _D = 350 mA		0.70	1.25	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 400 mA		1		S
Diode Forward Voltage ^a	V _{SD}	I _S = 150 mA, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 250 mA		750		pC
Gate-Source Charge	Q _{gs}			75		
Gate-Drain Charge	Q _{gd}			225		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 47 Ω I _D ≅ 200 mA, V _{GEN} = 4.5 V, R _g = 10 Ω		5		ns
Rise Time	t _r			5		
Turn-Off Delay Time	t _{d(off)}			25		
Fall Time	t _f			11		

Notes:

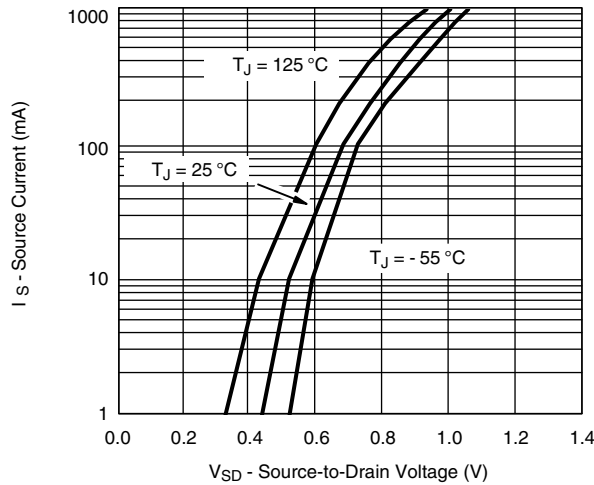
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

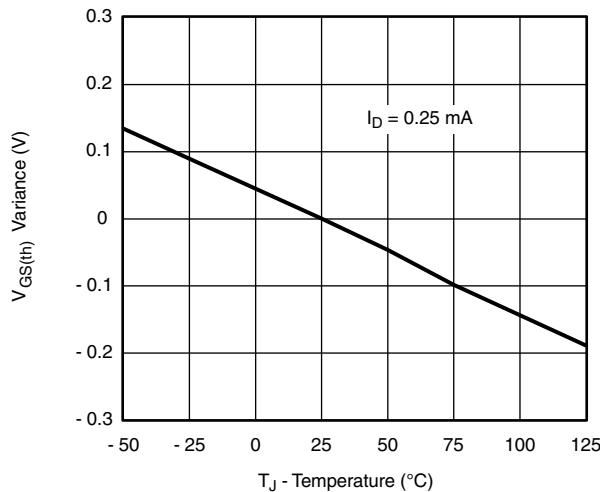
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



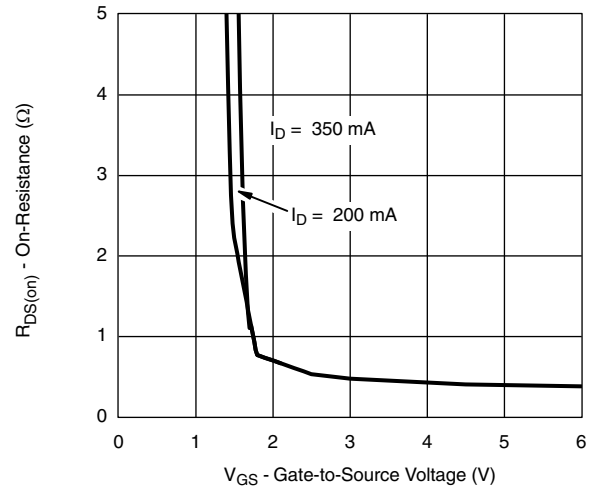
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



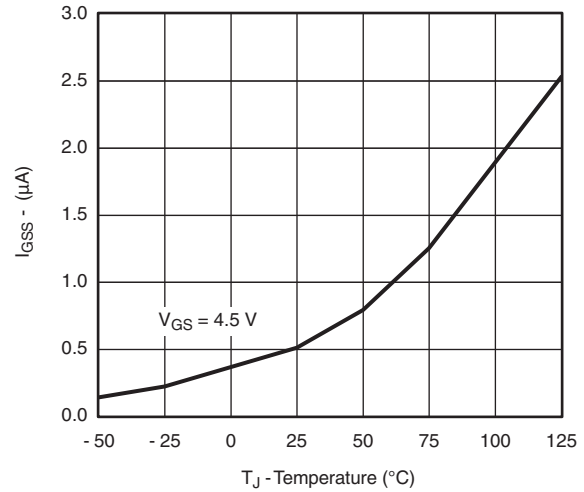
Source-Drain Diode Forward Voltage



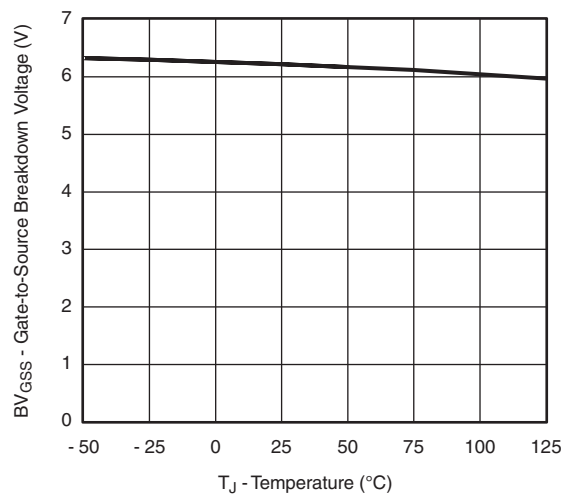
Threshold Voltage Variance vs. Temperature



On-Resistance vs. Gate-to-Source Voltage

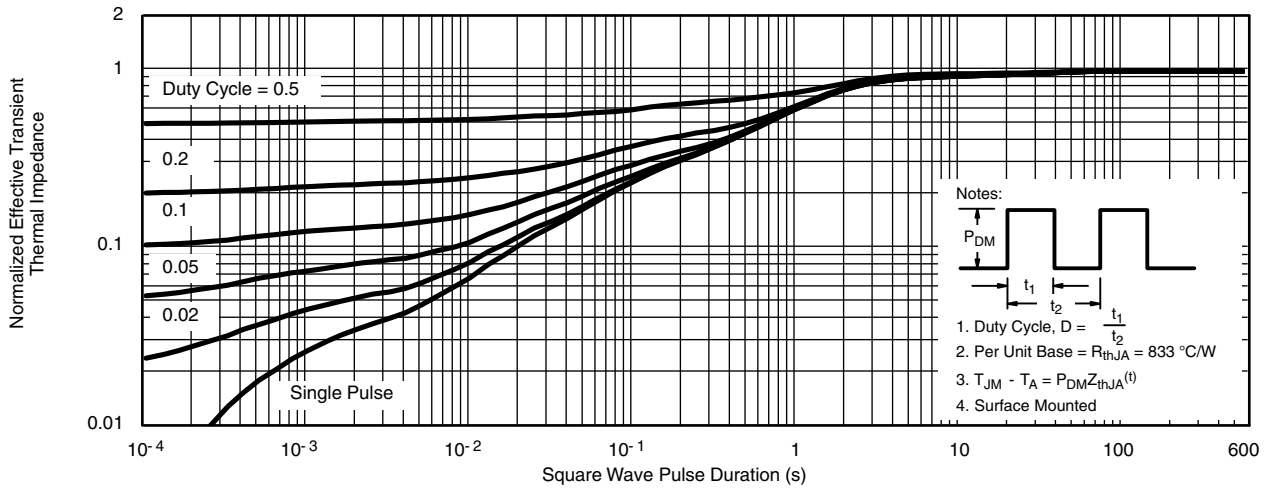


I_{GSS} vs. Temperature

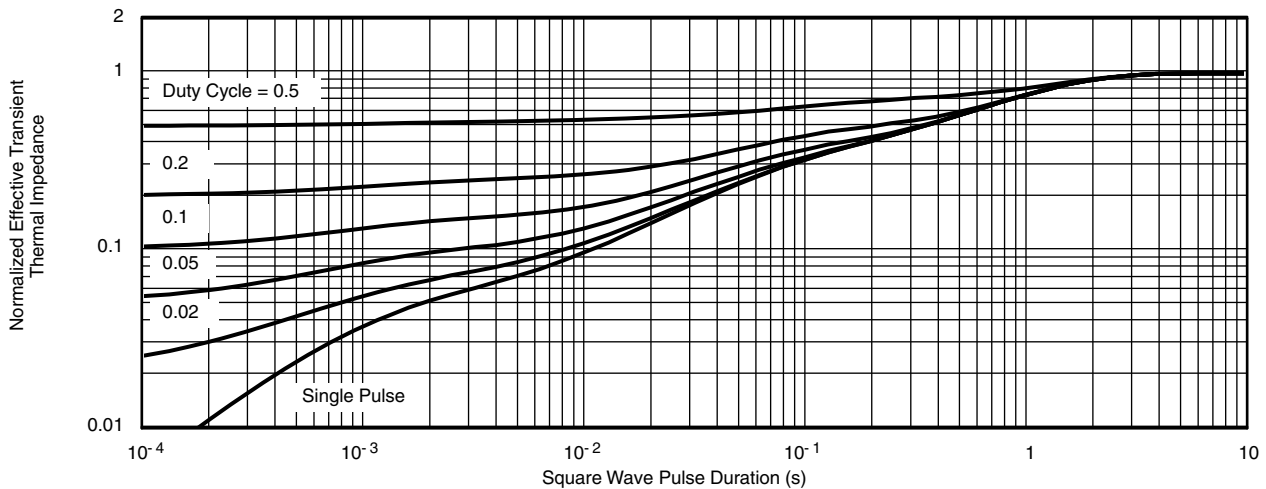


BV_{GSS} vs. Temperature

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



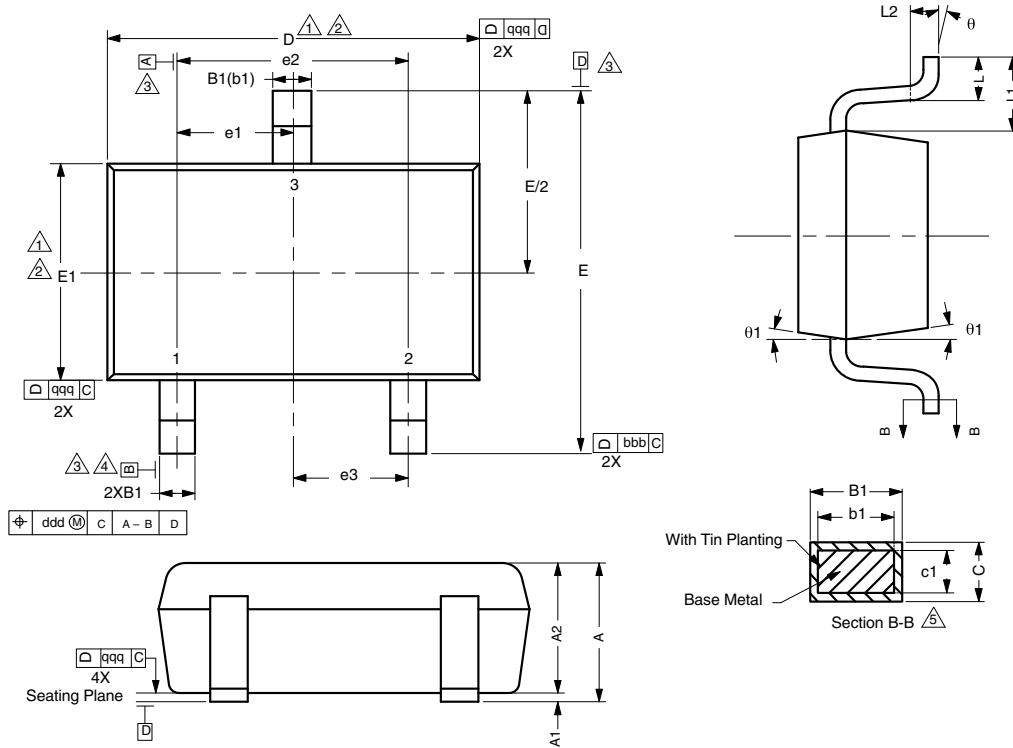
Normalized Thermal Transient Impedance, Junction-to-Ambient (SC-75A)



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71166.

SC-75A: 3 Leads



DWG: 5868

Notes

Dimensions in millimeters will govern.

- 1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
- 2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- 3. Datums A, B and D to be determined 0.10 mm from the lead tip.
- 4. Terminal positions are shown for reference only.
- 5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	-	0.80	
A1	0.00	-	0.10	
A2	0.65	0.70	0.80	
B1	0.19	-	0.24	5
b1	0.17	-	0.21	
c	0.13	-	0.15	5
c1	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E1	0.66	0.76	0.86	1, 2
e1	0.50 BSC			
e2	1.00 BSC			
e3	0.50 BSC			
L	0.15	0.205	0.30	
L1	0.40 ref.			
L2	0.15 BSC			
q	0°	-	8°	
q1	4°	-	10°	

RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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