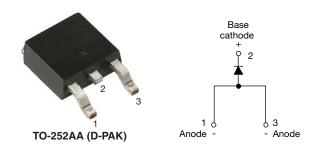
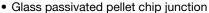


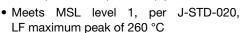
High Voltage Surface Mount Input Rectifier Diode, 8 A



PRODUCT SUMMARY				
Package	TO-252AA (D-PAK)			
I _{F(AV)}	8 A			
V_{R}	800 V, 1200 V			
V _F at I _F	1.1 V			
I _{FSM}	150 A			
T _J max.	150 °C			
Diode variation	Single die			

FEATURES











APPLICATIONS

- · Input rectification
- Vishay Semiconductors switches and output rectifiers which are available in identical package outlines

DESCRIPTION

The 8EWS..SPbF rectifier high voltage series has been optimized for very low forward voltage drop, with moderate leakage. The glass passivation technology used has reliable operation up to 150 °C junction temperature.

The **high reverse voltage** range available allows design of input stage primary rectification with **outstanding voltage surge** capability.

OUTPUT CURRENT IN TYPICAL APPLICATIONS						
APPLICATIONS SINGLE-PHASE BRIDGE THREE-PHASE BRIDGE						
NEMA FR-4 or G10 glass fabric-based epoxy with 4 oz. (140 μm) copper	1.2	1.6				
Aluminum IMS, R _{thCA} = 15 °C/W	2.5	2.8	Α			
Aluminum IMS with heatsink, R _{thCA} = 5 °C/W	5.5	6.5				

Note

T_A = 55 °C, T_J = 125 °C, footprint 300 mm²

MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL CHARACTERISTICS VALUES UN						
I _{F(AV)}	Sinusoidal waveform at T _C = 116 °C	8	Α			
V _{RRM}		800/1200	V			
I _{FSM}		150	А			
V _F	8 A, T _J = 25 °C	1.10	V			
TJ		-55 to +150	°C			

VOLTAGE RATINGS						
PART NUMBER	V _{RRM} , MAXIMUM PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I _{RRM} AT 150 °C mA			
8EWS08SPbF	800	900	0.5			
8EWS12SPbF	1200	1300	0.5			



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	SYMBOL TEST CONDITIONS		UNITS	
Maximum average forward current	I _{F(AV)}	T _C = 105 °C, 180° conduction half sine wave	8		
Maximum peak one cycle		10 ms sine pulse, rated V _{RRM} applied	125	Α	
non-repetitive surge current	I _{FSM}	10 ms sine pulse, no voltage reapplied	150		
Maximum I ² t for fusing	l ² t	10 ms sine pulse, rated V _{RRM} applied	78	A ² s	
Maximum I-t for fusing	i-r	10 ms sine pulse, no voltage reapplied	110	A-S	
Maximum I ² √t for fusing	I²√t	t = 0.1 ms to 10 ms, no voltage reapplied	1100	A²√s	

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CO	VALUES	UNITS		
Maximum forward voltage drop	V_{FM}	8 A, T _J = 25 °C		1.1	V	
Forward slope resistance	r _t	T _{.1} = 150 °C	20	mΩ		
Threshold voltage	V _{F(TO)}	1j=150 C	0.82	V		
Maximum reverse leake as surrent		T _J = 25 °C		0.05	m۸	
Maximum reverse leakage current	IRM	T _J = 150 °C	V _R = Rated V _{RRM}	0.50	mA	

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction and storage temperature range	T _J , T _{Stg}		-55 to +150	°C	
Maximum thermal resistance, junction to case	R _{thJC}	DC operation	2.5	°C/W	
Typical thermal resistance, junction to ambient (PCB mount)	R _{thJA (1)}		62	C/VV	
Approximate weight			1	g	
Approximate weight			0.03	oz.	
Marking device		Case style TO-252AA (D-PAK)	8EW	S12S	

Note

 $^{^{(1)}}$ When mounted on 1" square (650 mm²) PCB of FR-4 or G-10 material 4 oz. (140 µm) copper 40 °C/W For recommended footprint and soldering techniques refer to application note #AN-994

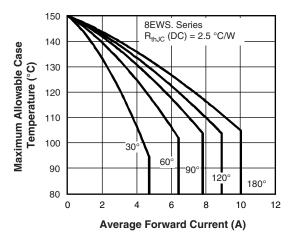


Fig. 1 - Current Rating Characteristics

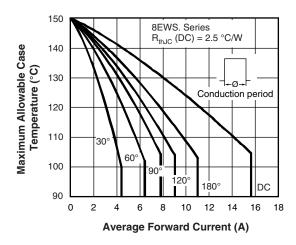


Fig. 2 - Current Rating Characteristics

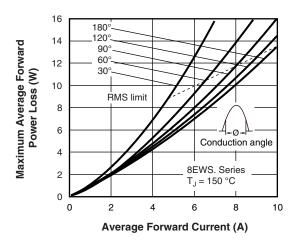


Fig. 3 - Forward Power Loss Characteristics

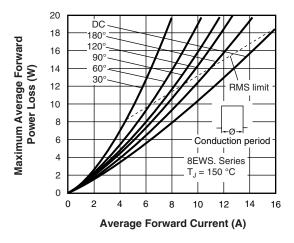


Fig. 4 - Forward Power Loss Characteristics

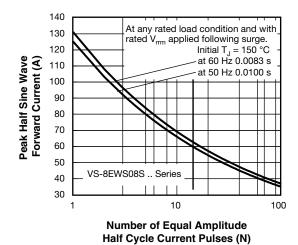


Fig. 5 - Maximum Non-Repetitive Surge Current

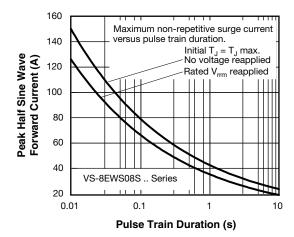


Fig. 6 - Maximum Non-Repetitive Surge Current

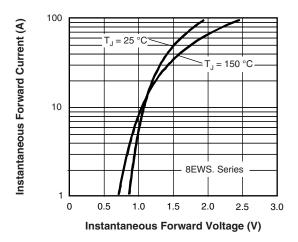


Fig. 7 - Forward Voltage Drop Characteristics

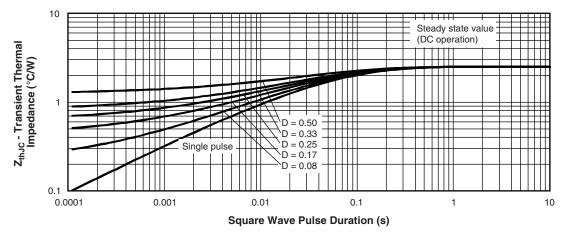
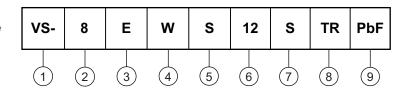


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics



ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product

2 - Current rating (8 = 8 A)

3 - Circuit configuration:

E = single diode

4 - Package:

W = D-PAK

5 - Type of silicon:

S = standard recovery rectifier

08 = 800 V

6 - Voltage ratings —

12 = 1200 V

7 - S = surface mountable

8 - • TR = tape and reel

• TRR = tape and reel (right oriented)

• TRL = tape and reel (left oriented)

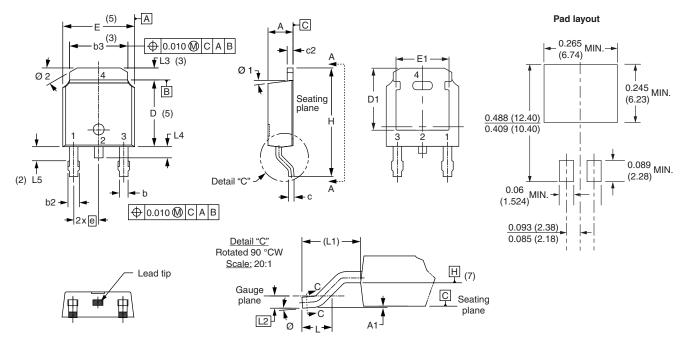
9 - PbF = lead (Pb)-free

LINKS TO RELATED DOCUMENTS				
Dimensions <u>www.vishay.com/doc?95016</u>				
Part marking information	www.vishay.com/doc?95059			
Packaging information	www.vishay.com/doc?95033			



D-PAK (TO-252AA)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIN	IETERS	INCHES		NOTES
STIVIBUL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	2.18	2.39	0.086	0.094	
A1	-	0.13	-	0.005	
b	0.64	0.89	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	3
С	0.46	0.61	0.018	0.024	
c2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	5
D1	5.21	-	0.205	-	3
E	6.35	6.73	0.250	0.265	5
E1	4.32	-	0.170	-	3

SYMBOL	MILLIN	IETERS	INCHES		NOTES
STIMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
е	2.29	BSC	0.090	BSC	
Н	9.40	10.41	0.370	0.410	
L	1.40	1.78	0.055	0.070	
L1	2.74	BSC	0.108	REF.	
L2	0.51 BSC		0.020 BSC		
L3	0.89	1.27	0.035	0.050	3
L4	-	1.02	-	0.040	
L5	1.14	1.52	0.045	0.060	2
Ø	0°	10°	0°	10°	
Ø1	0°	15°	0°	15°	
Ø2	25°	35°	25°	35°	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension uncontrolled in L5
- (3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip
- (5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (6) Dimension b1 and c1 applied to base metal only
- (7) Datum A and B to be determined at datum plane H
- (8) Outline conforms to JEDEC outline TO-252AA

Revision: 05-Dec-12 1 Document Number: 95016

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Vishay

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