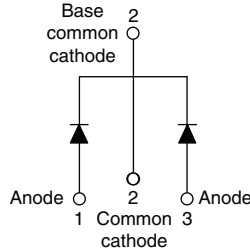


Schottky Rectifier, 2 x 8 A


TO-220AB


FEATURES

- 175 °C T_J operation
- Center tap configuration
- Low forward voltage drop
- High frequency operation
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- Guard ring for enhanced ruggedness and long term reliability
- Lead (Pb)-free ("PbF" suffix)
- Designed and qualified for industrial level


RoHS*
COMPLIANT

PRODUCT SUMMARY

$I_{F(AV)}$	2 x 8 A
V_R	60 to 100 V

DESCRIPTION

This center tap Schottky rectifier series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in switching power supplies, converters, freewheeling diodes, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	16	A
V_{RRM}		60 to 100	V
I_{FSM}	$t_p = 5 \mu s$ sine	850	A
V_F	8 Apk, $T_J = 125 \text{ }^\circ\text{C}$ (per leg)	0.58	V
T_J	Range	- 55 to 175	$^\circ\text{C}$

VOLTAGE RATINGS

PARAMETER	SYMBOL	16CTQ060PbF	16CTQ080PbF	16CTQ100PbF	UNITS
Maximum DC reverse voltage	V_R	60	80	100	V
Maximum working peak reverse voltage	V_{RWM}				

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current per leg See fig. 5 per device	$I_{F(AV)}$	50 % duty cycle at $T_C = 148 \text{ }^\circ\text{C}$, rectangular waveform	8	A
			16	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7	I_{FSM}	5 μs sine or 3 μs rect. pulse	850	A
		10 ms sine or 6 ms rect. pulse		
Non-repetitive avalanche energy per leg	E_{AS}	$T_J = 25 \text{ }^\circ\text{C}$, $I_{AS} = 0.50 \text{ A}$, $L = 60 \text{ mH}$	7.50	mJ
Repetitive avalanche current per leg	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	0.50	A

* Pb containing terminations are not RoHS compliant, exemptions may apply

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop per leg See fig. 1	$V_{FM}^{(1)}$	8 A	$T_J = 25\text{ }^\circ\text{C}$	0.72	V
		16 A		0.88	
		8 A	$T_J = 125\text{ }^\circ\text{C}$	0.58	
		16 A		0.69	
Maximum reverse leakage current per leg See fig. 2	$I_{RM}^{(1)}$	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{rated } V_R$	0.55	mA
		$T_J = 125\text{ }^\circ\text{C}$		7.0	
Threshold voltage	$V_{F(TO)}$	$T_J = T_J \text{ maximum}$		0.415	V
Forward slope resistance	r_t			11.07	m Ω
Maximum junction capacitance per leg	C_T	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz) 25 $^\circ\text{C}$		500	pF
Typical series inductance per leg	L_S	Measured lead to lead 5 mm from package body		8.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R		10 000	V/ μs

Note

(1) Pulse width < 300 μs , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}			- 55 to 175	$^\circ\text{C}$
Maximum thermal resistance, junction to case per leg	R_{thJC}	DC operation		3.25	$^\circ\text{C/W}$
Maximum thermal resistance junction to case per package	R_{thJC}			1.63	
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth and greased		0.50	
Approximate weight				2	g
				0.07	oz.
Mounting torque	minimum			6 (5)	kgf · cm (lbf · in)
	maximum			12 (10)	
Marking device		Case style TO-220AB		16CTQ100	

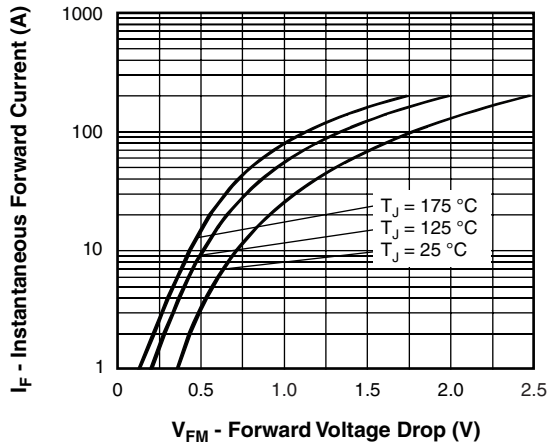


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

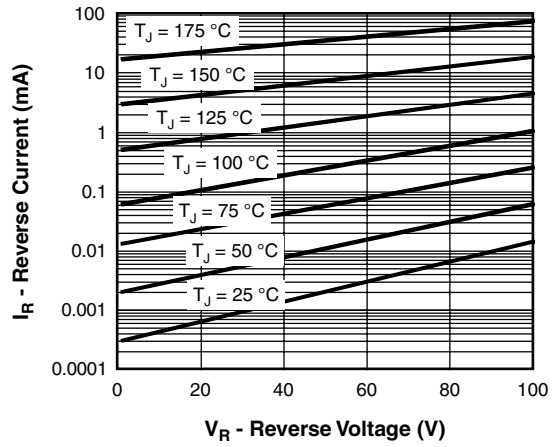


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

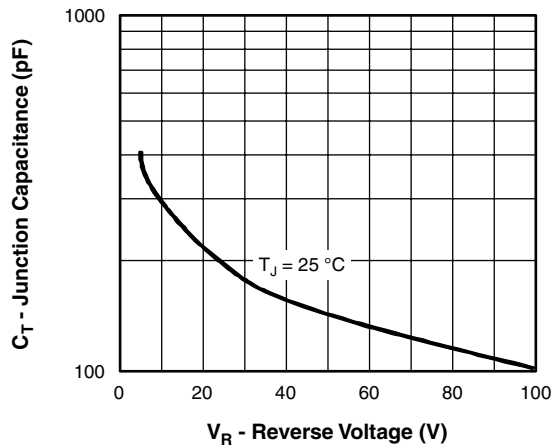


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

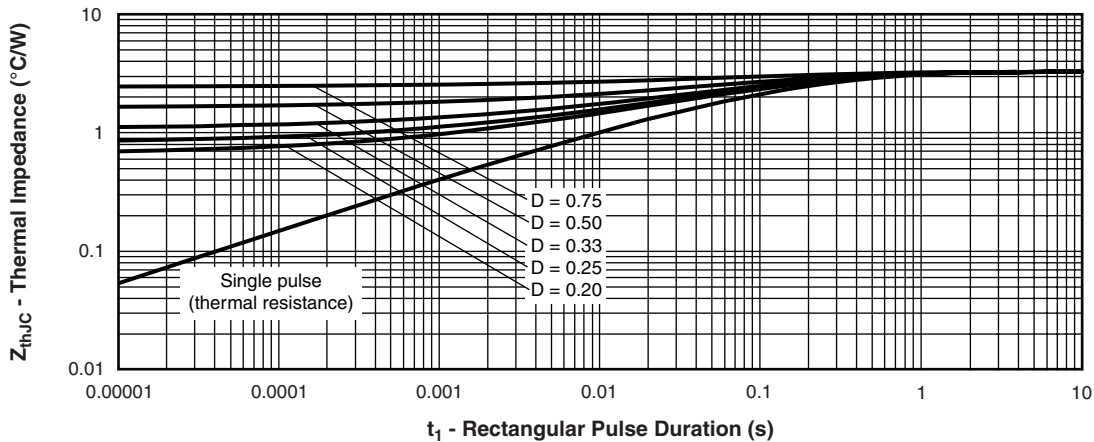


Fig. 4 - Maximum Thermal Impedance Z_{ThJC} Characteristics (Per Leg)

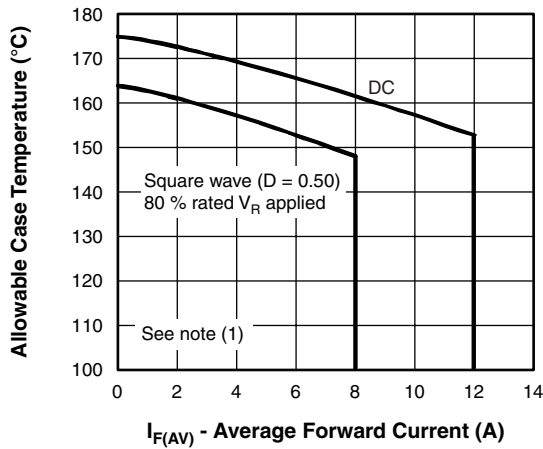


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

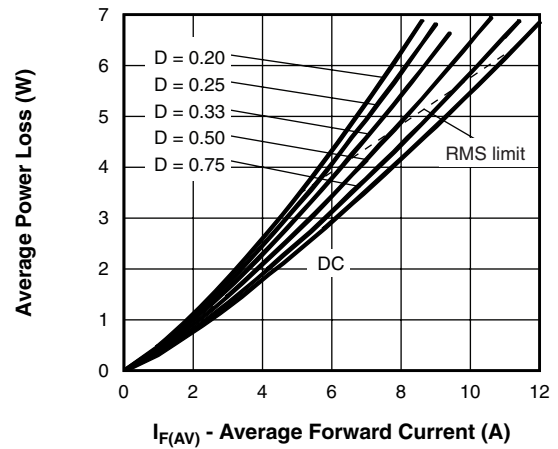


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

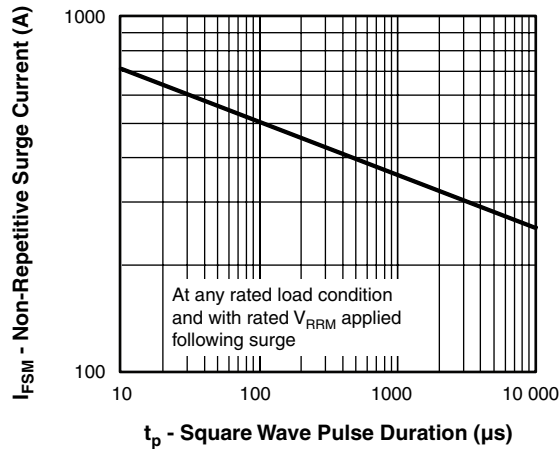


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)



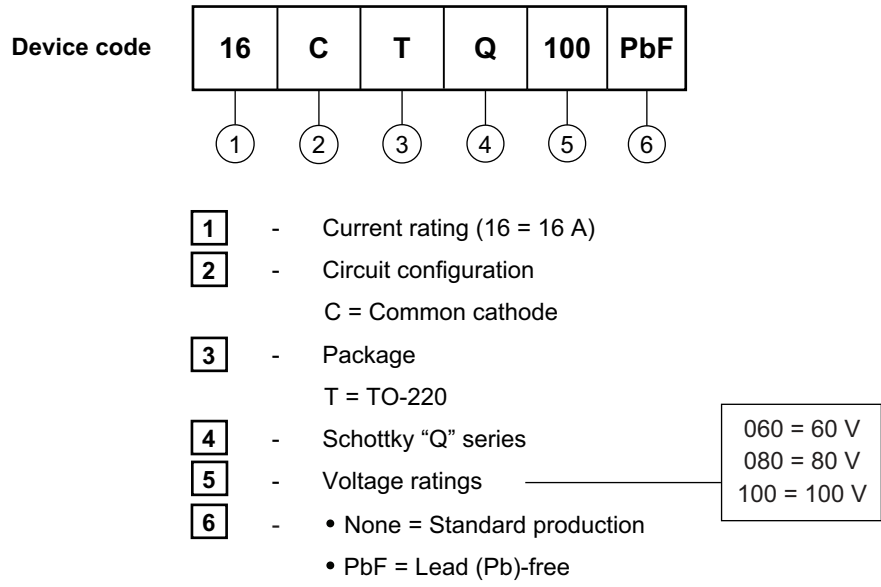
Fig. 8 - Unclamped Inductive Test Circuit

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;
 P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R applied



ORDERING INFORMATION TABLE



Tube standard pack quantity: 50 pieces

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95222
Part marking information	http://www.vishay.com/doc?95225
SPICE model	http://www.vishay.com/doc?95279

TO-220AB

DIMENSIONS in millimeters and inches



Lead assignments

Diodes

1. - Anode/open
2. - Cathode
3. - Anode

Conforms to JEDEC outline TO-220AB

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, except A2 (maximum) and D2 (minimum) where dimensions are derived from the actual package outline



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