

20V P-CHANNEL ENHANCEMENT MODE MOSFET

Summary

V _{DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
-20V	$24m\Omega @V_{GS} = -4.5V$	-6.6 A
200	$31m\Omega @V_{GS} = -2.5V$	-5.8 A

Features and Benefits

- Typical Off Board Profile of 0.575mm Ideally Suited for Thin Applications
- Low R_{DS(ON)} Minimizes Conduction Losses
- PCB Footprint of 2.56mm²
- ESD Protected Gate 2kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Power Management Functions
- Analog Switches

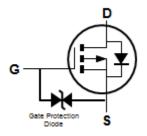
Mechanical Data

- Case: U-DFN1616-6
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Lead Free Plating (NiPdAu Finish over Copper Leadframe).
- Terminals: Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.04 grams (Approximate)

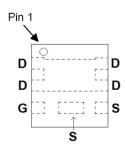


Top View

Bottom View



Device Symbol



Top View Pin-Out

Ordering Information (Note 4)

Product	Case	Packaging
DMP2035UFCL-7	U-DFN1616-6	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com.

Marking Information



25P = Product Type Marking Code YM = Date Code Marking Y = Year (ex: C = 2015) M = Month (ex: 9 = September)

Date Code Key

Year	201	5	2016		2017	20	18	2019		2020	2	021
Code	С		D		Е	l l	=	G		Н		
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic		Symbol	Value	Units	
Drain-Source Voltage		V_{DSS}	-20	V	
Gate-Source Voltage		V _{GSS}	±8	V	
Continuous Drain Current (Note 6)	Steady State	$T_A = +25$ °C $T_A = +70$ °C	l _D	-6.6 -5.3	Α
Pulsed Drain Current (380µs Pulse, 1% Duty Cyc	cle)(Note 7)	I _{DM}	-40	А	
Maximum Continuous Body Diode Forward Curre	ent (Note 6)	Is	-1.7	Α	

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P _D	0.74	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	$R_{\theta JA}$	169	°C/W
Power Dissipation (Note 6)	P _D	1.6	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 6)	$R_{\theta JA}$	79	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

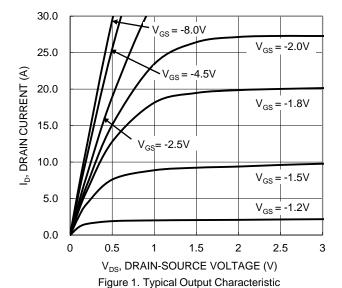
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	-20	-	-	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	-	-	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
Zero Gate Voltage Drain Current T _J = +150°C (Note 8)	I _{DSS}	-	-	-100	μA	V _{DS} = -16V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	-	-	±10	μA	$V_{GS} = \pm 8V$, $V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	-0.4	-	-1.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
			19	24		$V_{GS} = -4.5V$, $I_D = -8.0A$
Static Drain-Source On-Resistance	R _{DS(ON)}	-	24	31	$m\Omega$	$V_{GS} = -2.5V, I_D = -7.0A$
			31	45		$V_{GS} = -1.8V, I_D = -6.0A$
Diode Forward Voltage	V_{SD}	-0.5	-0.7	-1.2	V	$V_{GS} = 0V, I_{S} = -1A$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	•	1,610	2,200	pF	101/11/
Output Capacitance	Coss	-	157	240	pF	$V_{DS} = -10V, V_{GS} = 0V$ - f = 1.0MHz
Reverse Transfer Capacitance	Crss	-	145	220	pF	1 = 1.0WI 12
Gate Resistance	R_g	-	9.45	14.5	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge (V _{GS} = -8V)	Q_{g}	-	29	44	nC	
Total Gate Charge (V _{GS} = -4.5V)	Qq	-	15.4	21	nC	V _{DS} = -10V,
Gate-Source Charge	Q_{gs}	-	2.5	3.8	nC	$I_D = -4A$
Gate-Drain Charge	Q_{gd}	-	3.3	5	nC	
Turn-On Delay Time	t _{D(ON)}	1	16.8	34	ns	
Turn-On Rise Time	t _R	-	12.4	25	ns	$V_{DS} = -20V, V_{GS} = -10V,$
Turn-Off Delay Time	t _{D(OFF)}	-	94.1	188	ns	$R_G = 6.0\Omega, I_D = -6A$
Turn-Off Fall Time	t _F	-	42.4	85	ns	

 Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 Repetitive rating, pulse width limited by junction temperature. Notes:

^{8.} Short duration pulse test used to minimize self-heating effect.

^{9.} Guaranteed by design. Not subject to product testing.





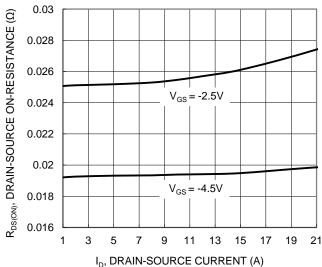


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

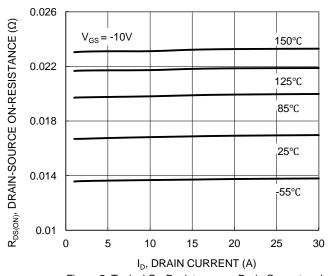


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

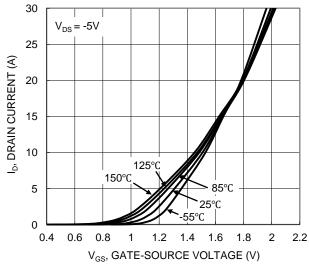


Figure 2. Typical Transfer Characteristic

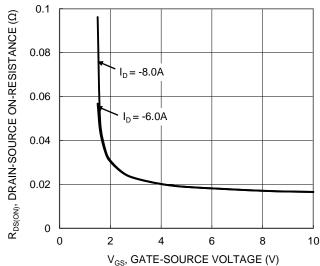


Figure 4. Typical Transfer Characteristic

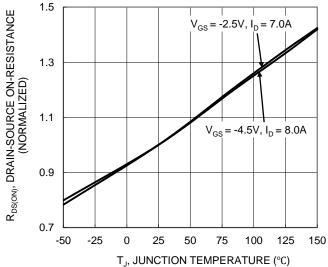


Figure 6. On-Resistance Variation with Junction Temperature





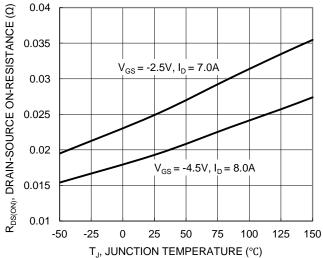


Figure 7. On-Resistance Variation with Junction Temperature

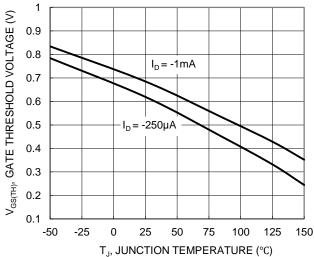


Figure 8. Gate Threshold Variation vs. Junction Temperature

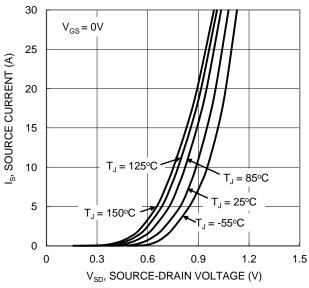
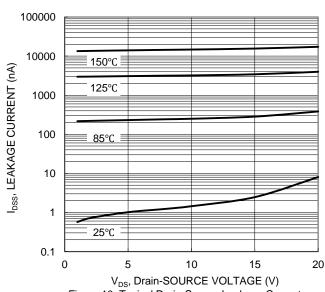


Figure 9. Diode Forward Voltage vs. Current



V_{DS}, Drain-SOURCE VOLTAGE (V) Figure 10. Typical Drain-Source Leakage Current vs. Voltage

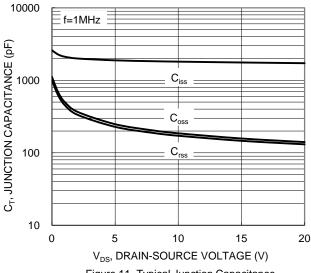


Figure 11. Typical Junction Capacitance

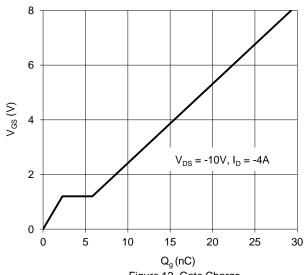
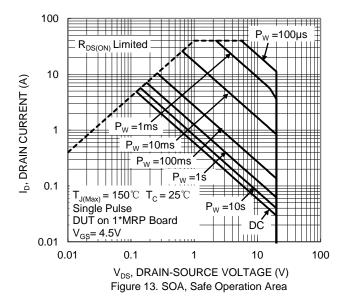


Figure 12. Gate Charge





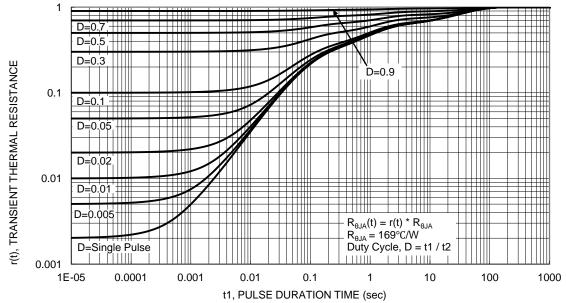
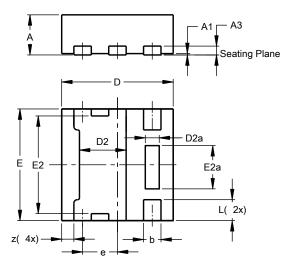


Figure 14. Transient Thermal Resistance



Package Outline Dimensions

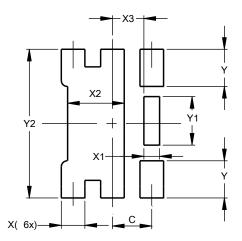
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



U-DFN1616-6 (Type K)						
Dim	Min	Max	Тур			
Α	0.55	0.60	0.575			
A1	0.00	0.05	0.02			
A3			0.13			
b	0.20	0.30	0.25			
D	1.55	1.65	1.60			
D2	0.57	0.77	0.67			
D2a	0.10	0.30	0.20			
е			0.50			
Е	1.55	1.65	1.60			
E2	1.30	1.50	1.40			
E2a	0.52	0.72	0.62			
L	0.25	0.35	0.30			
Z	1		0.175			
All Dimensions in mm						

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value		
Dilliensions	(in mm)		
С	0.500		
Х	0.300		
X1	0.200		
X2	0.720		
Х3	0.400		
Y	0.475		
Y1	0.620		
Y2	1.900		



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