

**Applications**

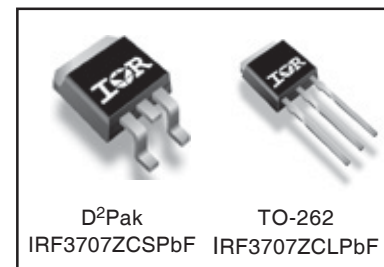
- High Frequency Synchronous Buck Converters for Computer Processor Power
- Lead-Free

HEXFET® Power MOSFET

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>Qg</b>
<b>30V</b>	<b>9.5mΩ</b>	<b>9.7nC</b>

**Benefits**

- Low R<sub>DS(on)</sub> at 4.5V V<sub>GS</sub>
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	59 <sup>Ⓞ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	42 <sup>Ⓞ</sup>	
I <sub>DM</sub>	Pulsed Drain Current <sup>Ⓛ</sup>	230	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	57	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation	28	
	Linear Derating Factor	0.38	W/°C
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	2.653	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) <sup>Ⓞ</sup>	—	40	

Notes <sup>Ⓛ</sup> through <sup>Ⓞ</sup> are on page 11

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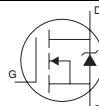
## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

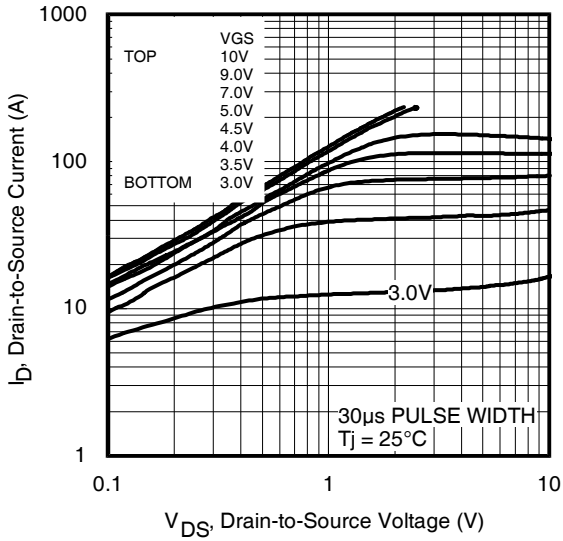
	Parameter	Min.	Typ.	Max.	Units	Conditions
B <sub>VDS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔB <sub>VDS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.023	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	7.5	9.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 21A ③
		—	10	12.5		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.80	2.25	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-5.3	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	81	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 17A
Q <sub>g</sub>	Total Gate Charge	—	9.7	15		
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	2.8	—		V <sub>DS</sub> = 15V
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	1.0	—	nC	V <sub>GS</sub> = 4.5V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	3.4	—		I <sub>D</sub> = 17A
Q <sub>godr</sub>	Gate Charge Overdrive	—	2.5	—		See Fig. 16
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	4.4	—		
Q <sub>oss</sub>	Output Charge	—	6.2	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.8	—		V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V ③
t <sub>r</sub>	Rise Time	—	41	—		I <sub>D</sub> = 17A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	12	—	ns	Clamped Inductive Load
t <sub>f</sub>	Fall Time	—	3.6	—		
C <sub>iss</sub>	Input Capacitance	—	1210	—		V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	260	—	pF	V <sub>DS</sub> = 15V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz

## Avalanche Characteristics

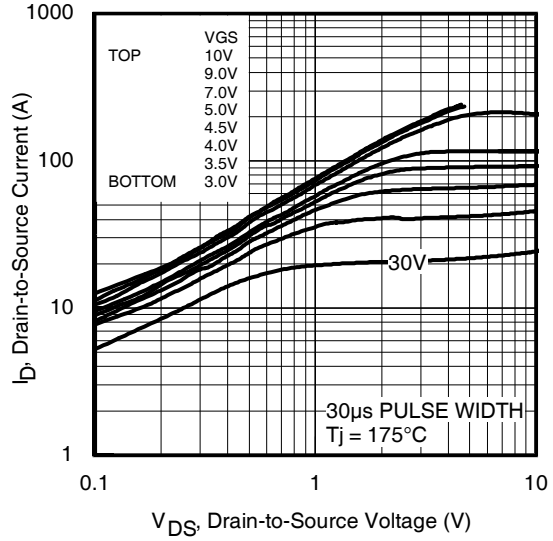
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	40	mJ
I <sub>AR</sub>	Avalanche Current ①	—	23	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	5.7	mJ

## Diode Characteristics

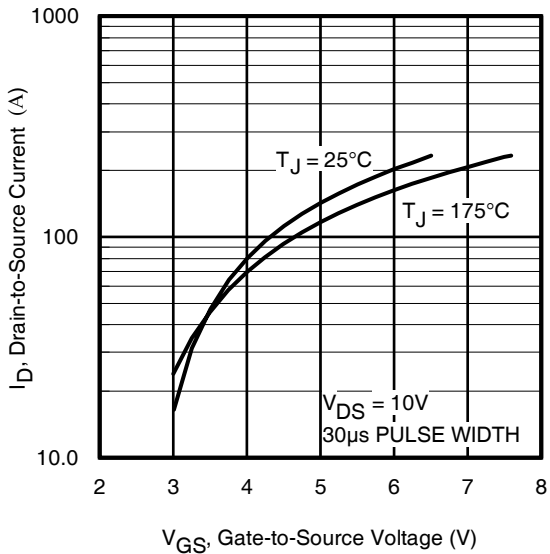
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	59 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	230		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 17A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	14	21	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 17A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	5.2	7.8	nC	di/dt = 100A/μs ③



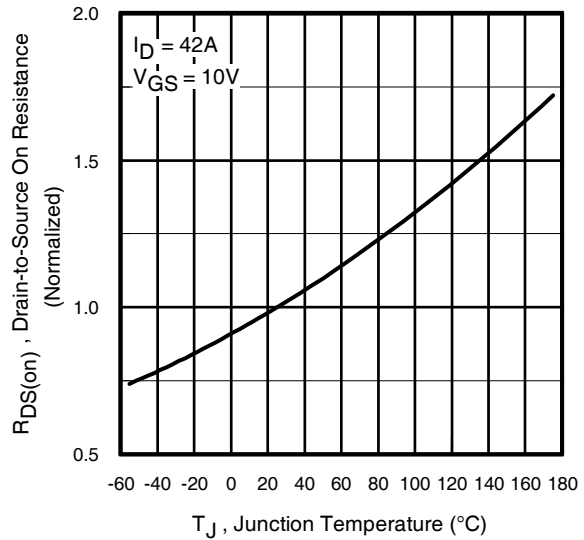
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

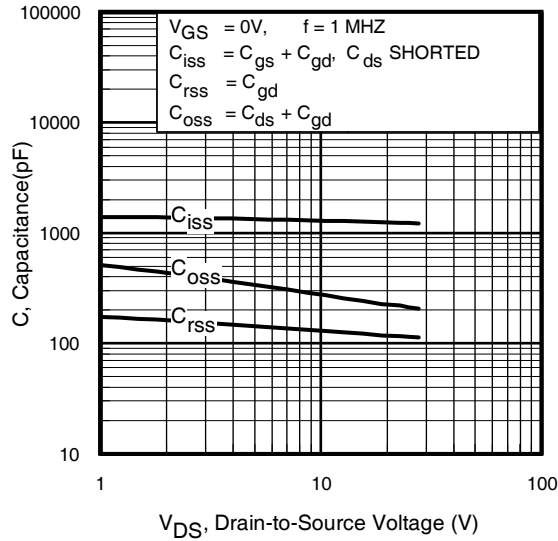


**Fig 3.** Typical Transfer Characteristics

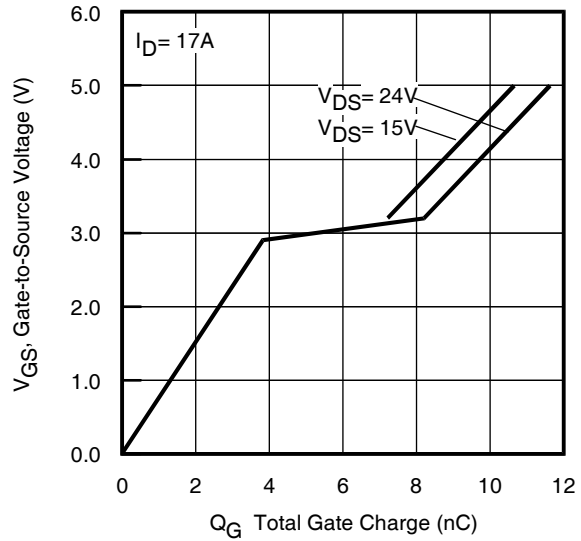


**Fig 4.** Normalized On-Resistance vs. Temperature

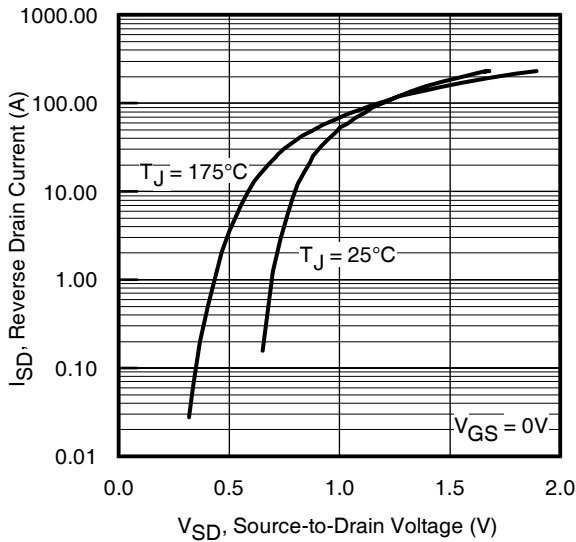
# IRF3707ZCS/LPbF



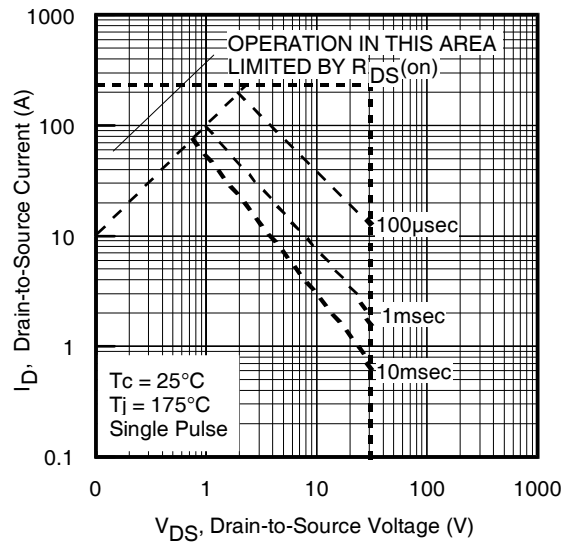
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



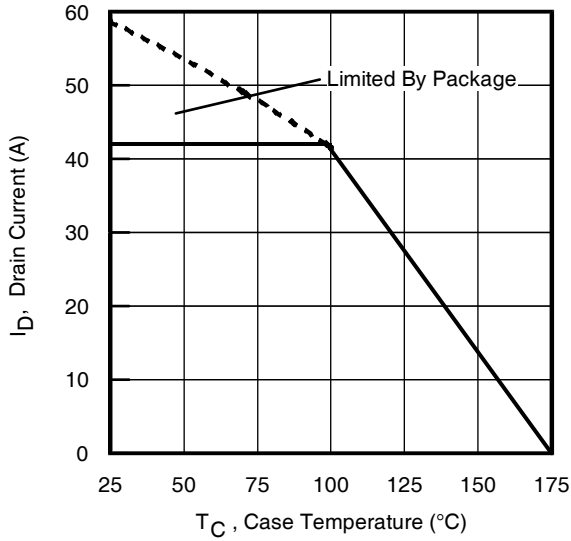
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



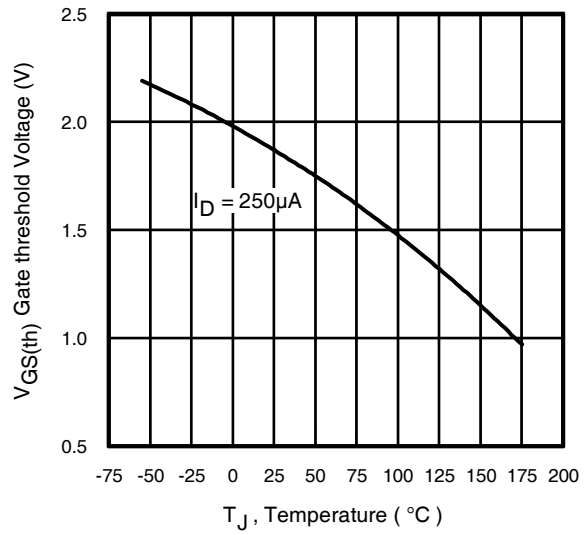
**Fig 7.** Typical Source-Drain Diode Forward Voltage



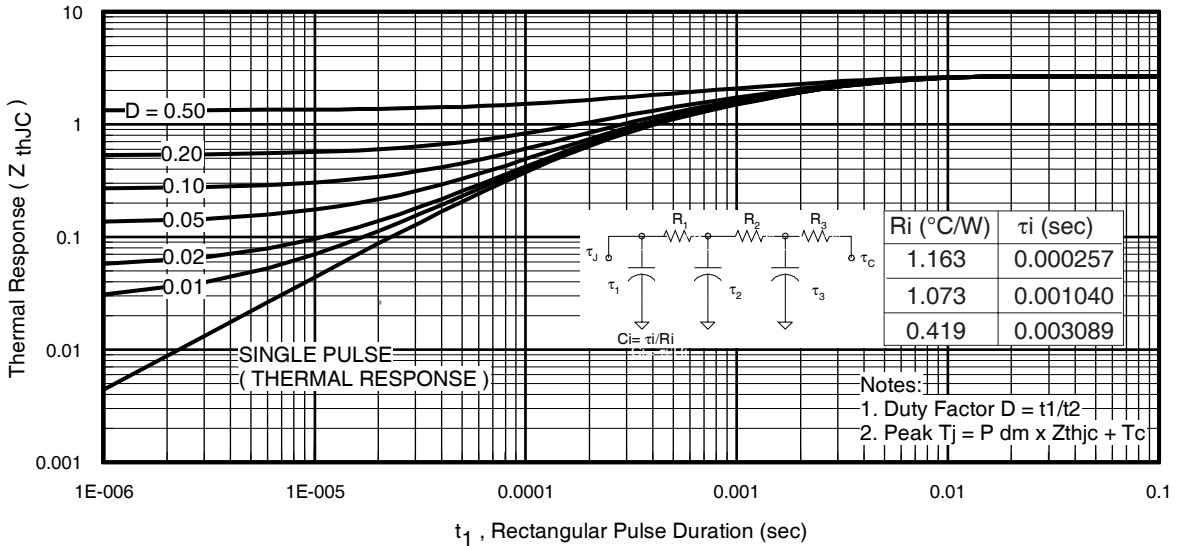
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



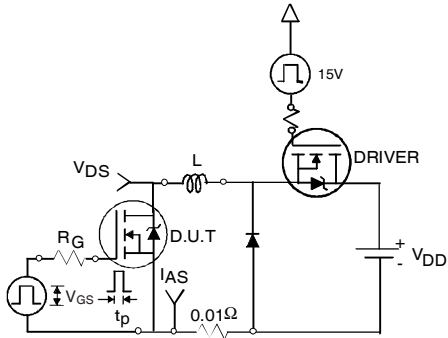
**Fig 10.** Threshold Voltage vs. Temperature



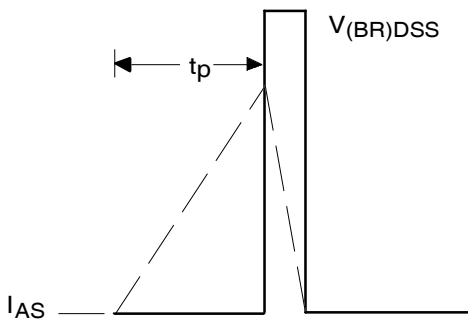
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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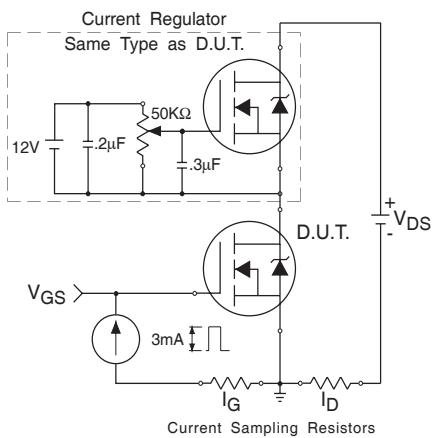
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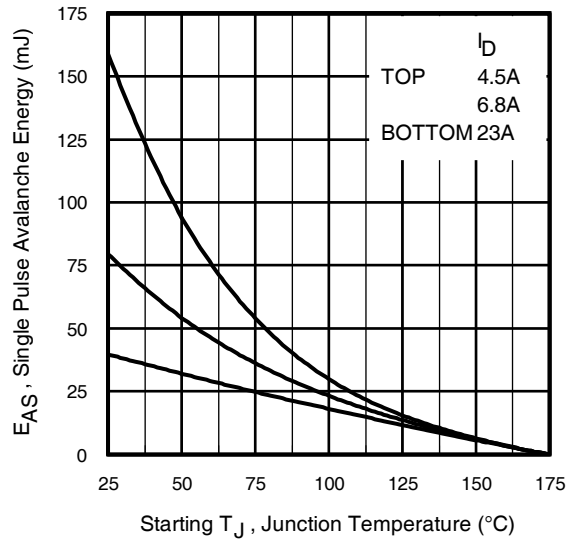
**Fig 12a.** Unclamped Inductive Test Circuit



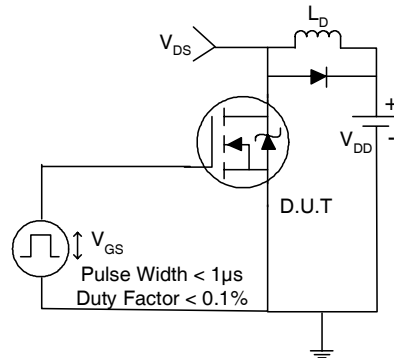
**Fig 12b.** Unclamped Inductive Waveforms



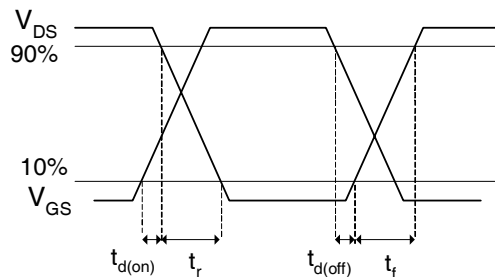
**Fig 13.** Gate Charge Test Circuit



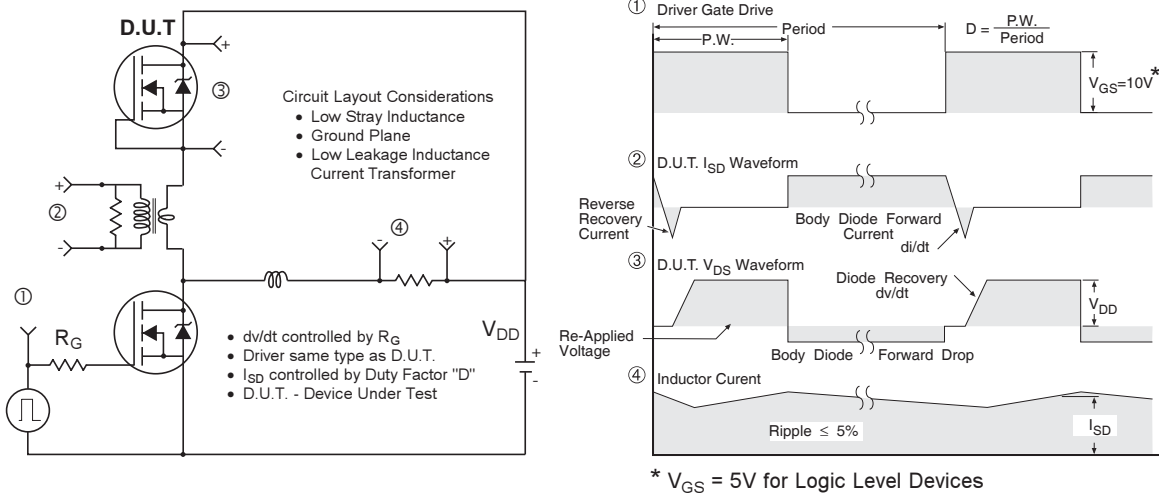
**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



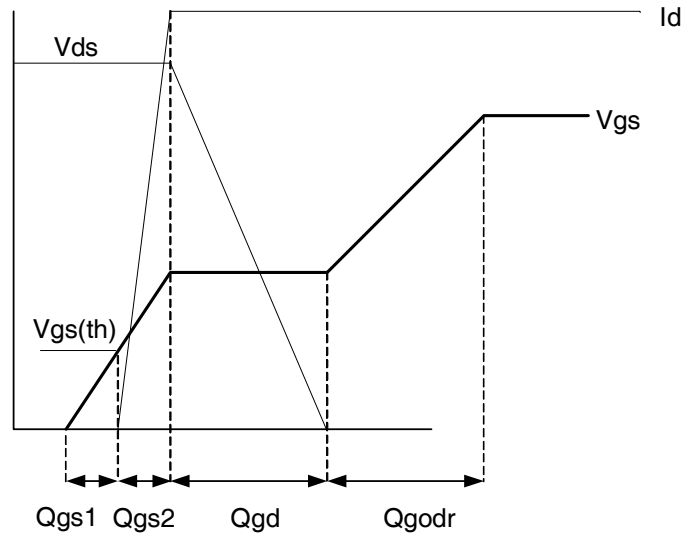
**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms



**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 16. Gate Charge Waveform**

## Power MOSFET Selection for Non-Isolated DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the  $R_{ds(on)}$  of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left( I_{rms}^2 \times R_{ds(on)} \right) + \left( I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left( I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + (Q_g \times V_g \times f) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms  $Q_{gs2}$  and  $Q_{oss}$  which are new to Power MOSFET data sheets.

$Q_{gs2}$  is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements,  $Q_{gs1}$  and  $Q_{gs2}$ , can be seen from Fig 16.

$Q_{gs2}$  indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to  $I_{dmax}$  at which time the drain voltage begins to change. Minimizing  $Q_{gs2}$  is a critical factor in reducing switching losses in Q1.

$Q_{oss}$  is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how  $Q_{oss}$  is formed by the parallel combination of the voltage dependant (non-linear) capacitance's  $C_{ds}$  and  $C_{dg}$  when multiplied by the power supply input buss voltage.

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = \left( I_{rms}^2 \times R_{ds(on)} \right) + (Q_g \times V_g \times f) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right) + (Q_{rr} \times V_{in} \times f)$$

\*dissipated primarily in Q1.

For the synchronous MOSFET Q2,  $R_{ds(on)}$  is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge  $Q_{oss}$  and reverse recovery charge  $Q_{rr}$  both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and  $V_{in}$ . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of  $Q_{gd}/Q_{gs1}$  must be minimized to reduce the potential for Cdv/dt turn on.

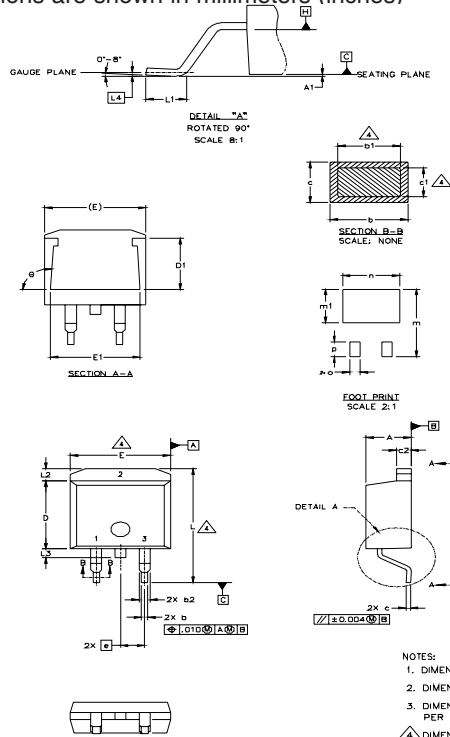


Figure A:  $Q_{oss}$  Characteristic



## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	3
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.576	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

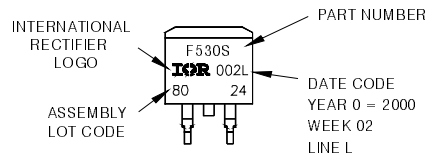
\* PART DEPENDENT.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [ .005" ] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

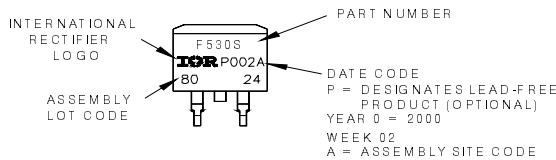
## D<sup>2</sup>Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE 'L'

Note: 'P' in assembly line  
position indicates 'Lead-Free'



**OR**

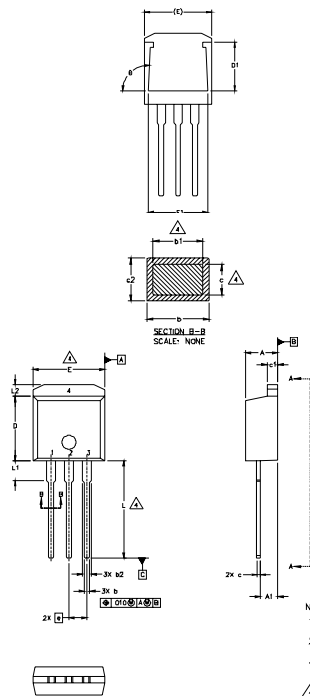


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRF3707ZCS/LPbF

International  
**IR** Rectifier

## TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

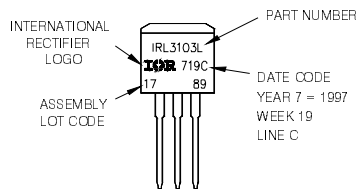
HEXFET	IGBT
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

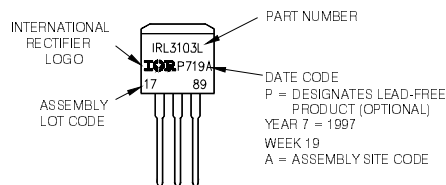
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW19, 1997  
 IN THE ASSEMBLY LINE 'C'

Note: 'P' in assembly line position indicates 'Lead-Free'



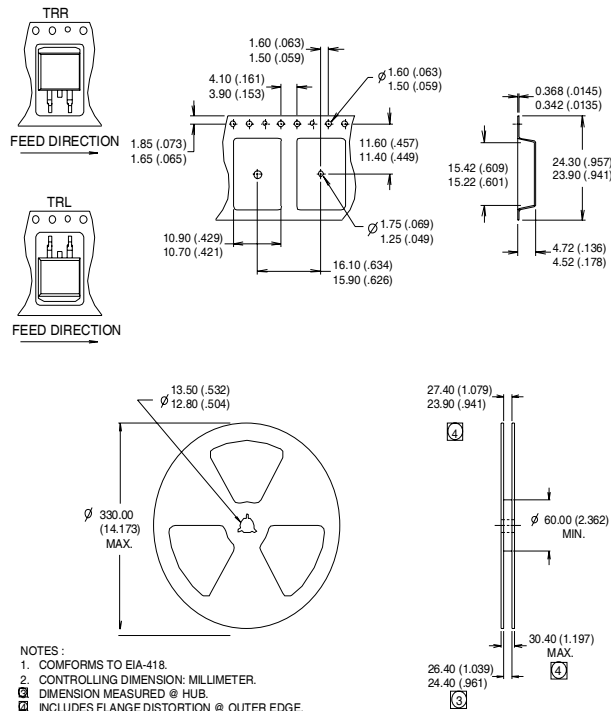
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D<sup>2</sup>Pak Tape & Reel Infomation

Dimensions are shown in millimeters (inches)



**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.15\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 23\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.

Data and specifications subject to change without notice.

This product has been designed and qualified for the Consumer market.

Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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