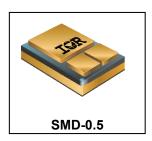


HEXFET® POWER MOSFET SURFACE MOUNT (SMD-0.5)

150V, P-CHANNEL

Product Summary

Part Number	BV _{DSS}	RDS(on)	I _D
IRF5NJ6215	-150V	0.29Ω	-11A



Description

Fifth Generation HEXFET® power MOSFETs from IR HiRel utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

Features

- Low RDS(on)
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units	
I _{D1} @ V _{GS} = -10V, T _C = 25°C	Continuous Drain Current	-11		
I_{D2} @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-7.2	Α	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	-44		
P _D @T _C = 25°C	Maximum Power Dissipation	75	W	
	Linear Derating Factor	0.6	W/°C	
V _{GS}	Gate-to-Source Voltage	±20	V	
E _{AS}	Single Pulse Avalanche Energy ②	130	mJ	
I _{AR}	Avalanche Current ①	-11	Α	
E _{AR}	Repetitive Avalanche Energy ①	7.5	mJ	
dv/dt	Peak Diode Recovery dv/dt ③	10	V/ns	
T _J	Operating Junction and	FF to 1 150		
T _{STG}	Storage Temperature Range	-55 to + 150	°C	
	Package Mounting Surface Temp	300 (for 5s)	-	
	Weight	1.0 (Typical)	g	

For Footnotes, refer to the page 2.



Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-150			V	$V_{GS} = 0V, I_{D} = -250\mu A$		
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		-0.17		V/°C	Reference to 25°C, I _D = -1.0mA		
R _{DS(on)}	Static Drain-to-Source On- Resistance			0.29	Ω	V _{GS} = -10V, I _{D2} = -7.2A ④		
V _{GS(th)}	Gate Threshold Voltage	-2.0		-4.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$		
gfs	Forward Transconductance	2.3			S	V _{DS} = -25V, I _{D2} = -7.2A ④		
I _{DSS}	Zara Cata Valtara Drain Current			-25		$V_{DS} = -120V, V_{GS} = 0V$		
	Zero Gate Voltage Drain Current			-250	μΑ	$V_{DS} = -120V, V_{GS} = 0V, T_{J} = 125$ °C		
I _{GSS}	Gate-to-Source Leakage Forward			-100	nA	$V_{GS} = -20V$		
	Gate-to-Source Leakage Reverse			100	IIA	V _{GS} = 20V		
Q_G	Total Gate Charge			66		$I_{D2} = -7.2A$		
Q_{GS}	Gate-to-Source Charge			13	nC	V _{DS} = -120V		
Q_{GD}	Gate-to-Drain ('Miller') Charge			40		V _{GS} = -10V		
t _{d(on)}	Turn-On Delay Time			25		V _{DD} = -75V		
t _r	Rise Time			65		$I_{D2} = -7.2A$		
t _{d(off)}	Turn-Off Delay Time			75	ns	$R_G = 6.8\Omega$		
t _f	Fall Time			53		$V_{GS} = -10V$		
Ls +L _D	Total Inductance		4.0		nH	Measured from center of Drain pad to center of Source pad		
C _{iss}	Input Capacitance		990			V _{GS} = 0V		
C _{oss}	Output Capacitance		230		pF	V _{DS} = -25V		
C _{rss}	Reverse Transfer Capacitance		120			f = 1.0MHz		

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current (Body Diode)			-11	^	
I _{SM}	Pulsed Source Current (Body Diode) ①			-44	А	
V_{SD}	Diode Forward Voltage			-1.6	V	$T_J=25^{\circ}C$, $I_S=-7.2A$, $V_{GS}=0V$
t _{rr}	Reverse Recovery Time			240	ns	$T_J = 25^{\circ}C$, $I_F = -7.2A$, $V_{DD} \le -25V$
Q _{rr}	Reverse Recovery Charge			1.7	μC	di/dt = -100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case			1.67	°C/W

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- \odot V_{DD} = -50V, starting T_J = 25°C, L = 5.0mH, Peak I_L = -7.2A, V_{GS} = -10V, R_G = 25 Ω



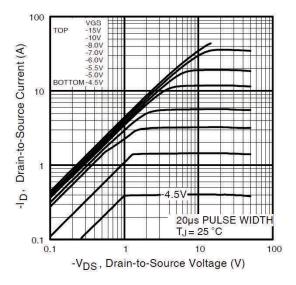


Fig 1. Typical Output Characteristics

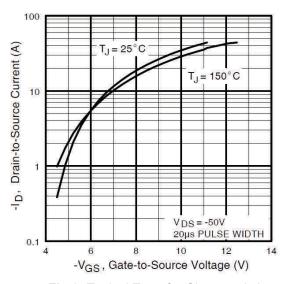


Fig 3. Typical Transfer Characteristics

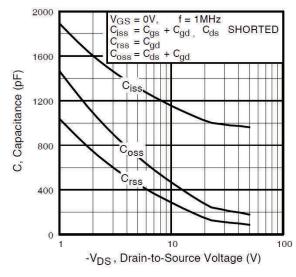


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

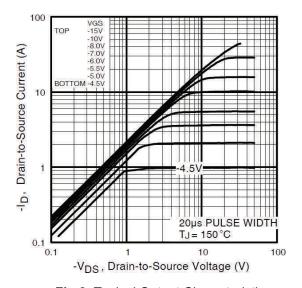


Fig 2. Typical Output Characteristics

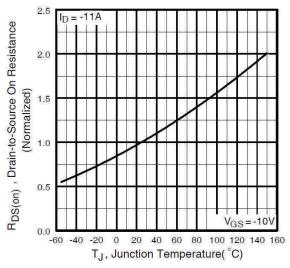


Fig 4. Normalized On-Resistance Vs. Temperature

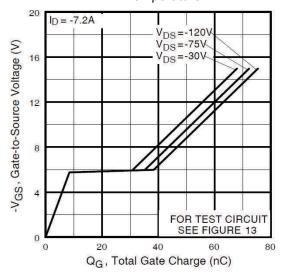


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

3



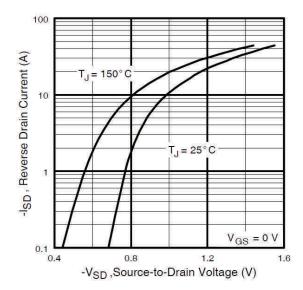


Fig 7. Typical Source-Drain Diode Forward Voltage

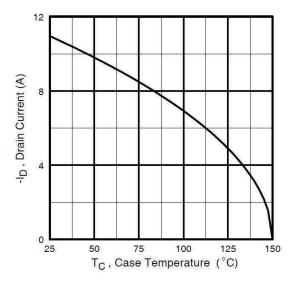


Fig 9. Maximum Drain Current Vs.Case Temperature

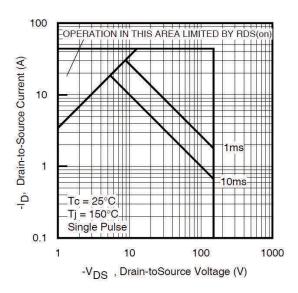


Fig 8. Maximum Safe Operating Area

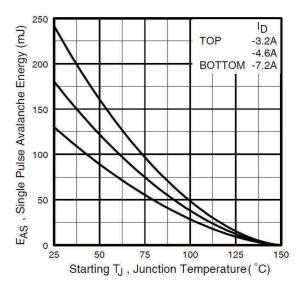


Fig 10. Maximum Avalanche Energy Vs. Drain Current

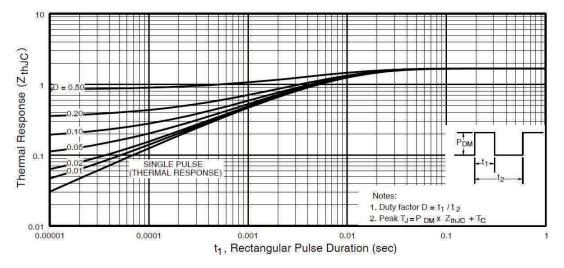


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



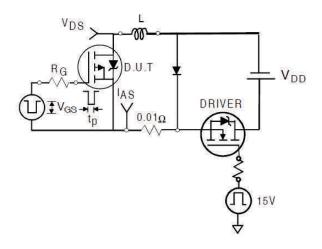


Fig 12a. Unclamped Inductive Test Circuit

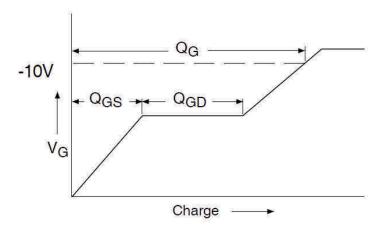


Fig 13a. Gate Charge Waveform

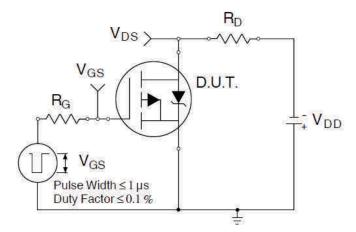


Fig 14a. Switching Time Test Circuit

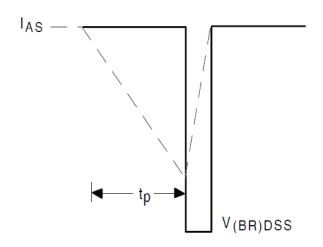


Fig 12b. Unclamped Inductive Waveforms

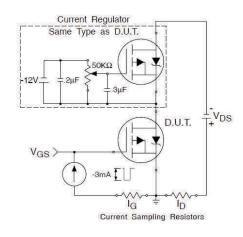


Fig 13b. Gate Charge Test Circuit

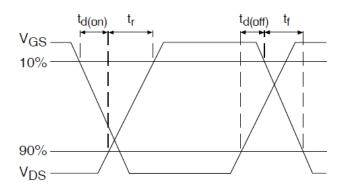
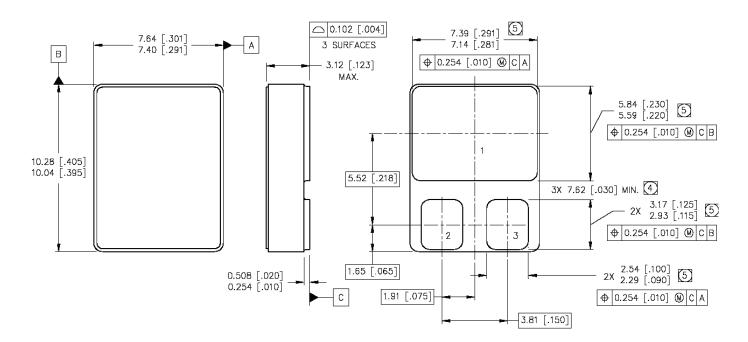


Fig 14b. Switching Time Waveforms

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Case Outline and Dimensions — SMD-0.5



NOTES:

- I. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4) DIMENSION INCLUDES METALLIZATION FLASH.
 - DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

1 = DRAIN

2 = GATE

3 = SOURCE



www.infineon.com/irhirel

Infineon Technologies Service Center: USA Tel: +1 (866) 951-9519 and International Tel: +49 89 234 65555

Leominster, Massachusetts 01453, USA Tel: +1 (978) 534-5776

San Jose, California 95134, USA Tel: +1 (408) 434-5000

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