TVS Diodes

Transient Voltage Suppressor Diodes

ESD3V3U4ULC

Ultra-low Capacitance ESD / Transient Protection Array

ESD3V3U4ULC

Data Sheet

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Final

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Revision History Revision 1.5, 2012-12-05	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.6, 2013-02-20	
6	Small updateds in Table 3

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Last Trademarks Update 2010-06-09

1 Ultra-low Capacitance ESD / Transient Protection Array

1.1 Features

- ESD / transient protection of high speed data lines exceeding:
  - **IEC61000-4-2 (ESD): ±20 kV (air/contact)**
  - **IEC61000-4-4 (EFT): ±2.5 kV (5/50ns)**
  - **IEC61000-4-5 (Surge): ±3 A (8/20µs)**
- Maximum working voltage: V_{RWM} **= 3.3 V**
- Ultra low capacitance C_L **= 0.4 pF** I/O to GND (typical)
- Very low clamping voltage: V_{CL} **= 8 V** (typical) at I_{PP} = 16 A
- Very low dynamic resistance: R_{DYN} **= 0.19 Ω** (typical)
- TSLP-9-1 package with pad pitch 0.5 mm, optimized pad design to simplify PCB layout
- Pb-free and halogen free package (RoHS compliant)

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, etc.

1.3 Product Description

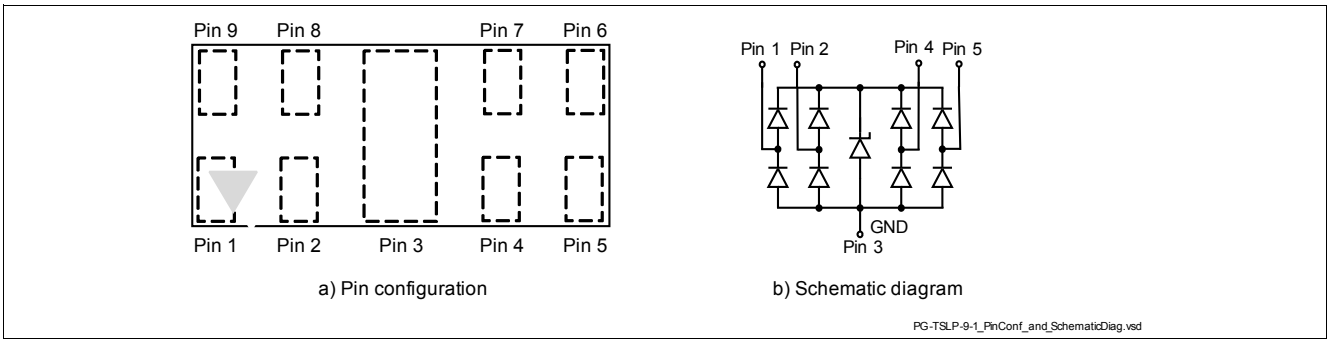

Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD3V3U4ULC	TSLP-9-1	4 lines, uni-directional	Z2

2 Characteristics

Table 2 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge[1)]	V_{ESD}	-20	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3	–	3	A
Operating temperature	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

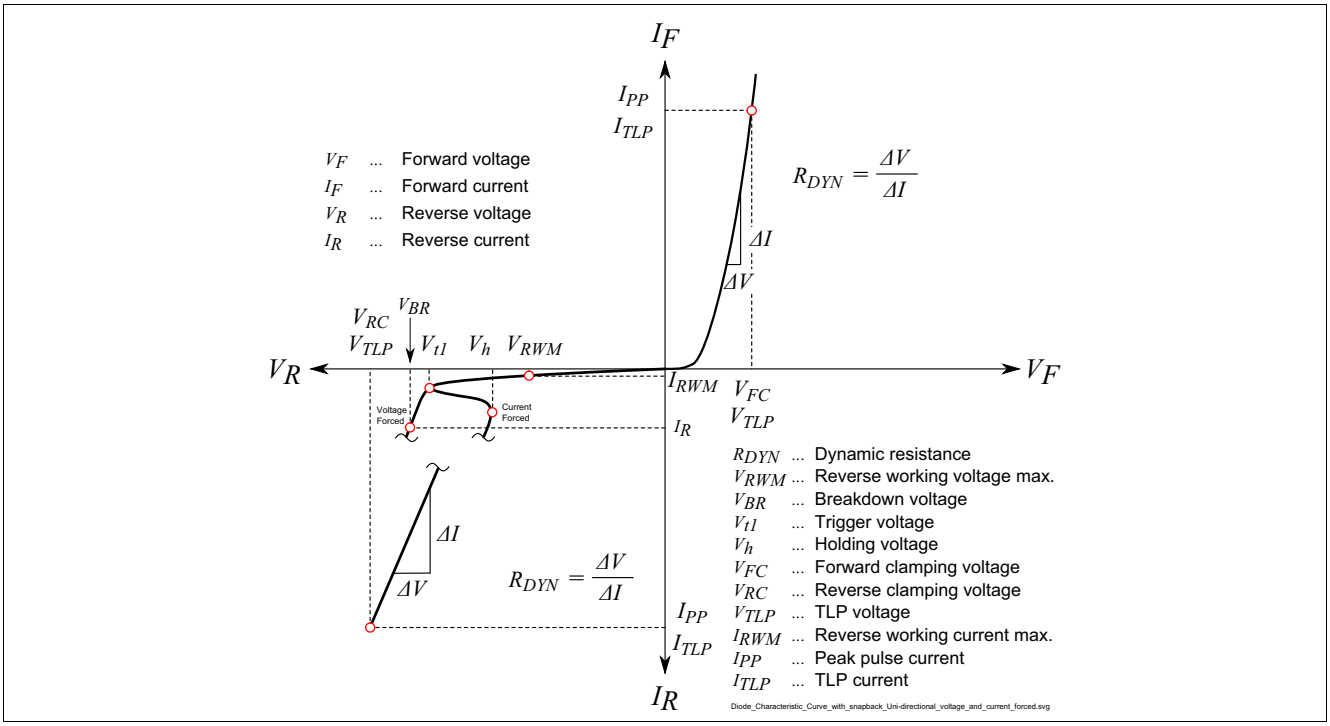

Figure 2 Definitions of electrical characteristics[1]

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage[1]	V_{RWM}	–	–	3.3	V	I/O to GND
Reverse current[1]	I_R	–	1	50	nA	I/O to GND, V_R = 3.3 V
Breakdown voltage[1]	V_{BR}	–	6.2	–	V	I/O to GND,
Reverse trigger voltage[2]	V_{t1}	–	6.2	–	V	I/O to GND,
Reverse holding voltage[2]	V_h	3.35	4	4.4	V	I/O to GND, I_R = 10 mA

1) Voltage forced

2) Current forced

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1]	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz, I/O to GND
		–	0.2	0.35	pF	V_R = 0 V, f = 1 MHz, I/O to I/O
Channel capacitance matching between I/O to GND	$\Delta C_{i/o\text{-}GND}$	–	0.035	–	pF	V_R = 0 V, f = 1 MHz, I/O to GND
Channel capacitance matching between I/O to I/O	$\Delta C_{i/o\text{-}i/o}$	–	0.017	–	pF	V_R = 0 V, f = 1 MHz, I/O to I/O

1) Total capacitance line to ground

Table 5 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping volage[1]	V_{CL}	–	4.8	–	V	I_{PP} = 1 A, t_p = 8/20µs from I/O to GND
		–	6.2	–		I_{PP} = 3 A, t_p = 8/20µs from I/O to GND
Clamping voltage[2]	V_{CL}	–	8	–		I_{TLP} = 16 A, from I/O to GND
		–	11	–		I_{TLP} = 30 A, from I/O to GND
Forward clamping voltage[1]	V_{FC}	–	1.4	–		I_{PP} = 1 A, t_p = 8/20µs from GND to I/O
		–	2.3	–		I_{PP} = 3 A, t_p = 8/20µs from GND to I/O
Forward clamping voltage[2]	V_{FC}	–	6	–		I_{TLP} = 16 A, from GND to I/O
		–	9	–		I_{TLP} = 30 A, from GND to I/O
Dynamic resistance[2]	R_{DYN}	–	0.19	–	Ω	I/O to GND
		–	0.23	–	Ω	GND to any I/O

1) I_{PP} according to IEC61000-4-5

2) Please refer to Application Note AN210. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{PP1} = 10 A and I_{PP2} = 40 A **[2]**.

3 Typical Characteristics at T_A = 25 °C, unless otherwise specified

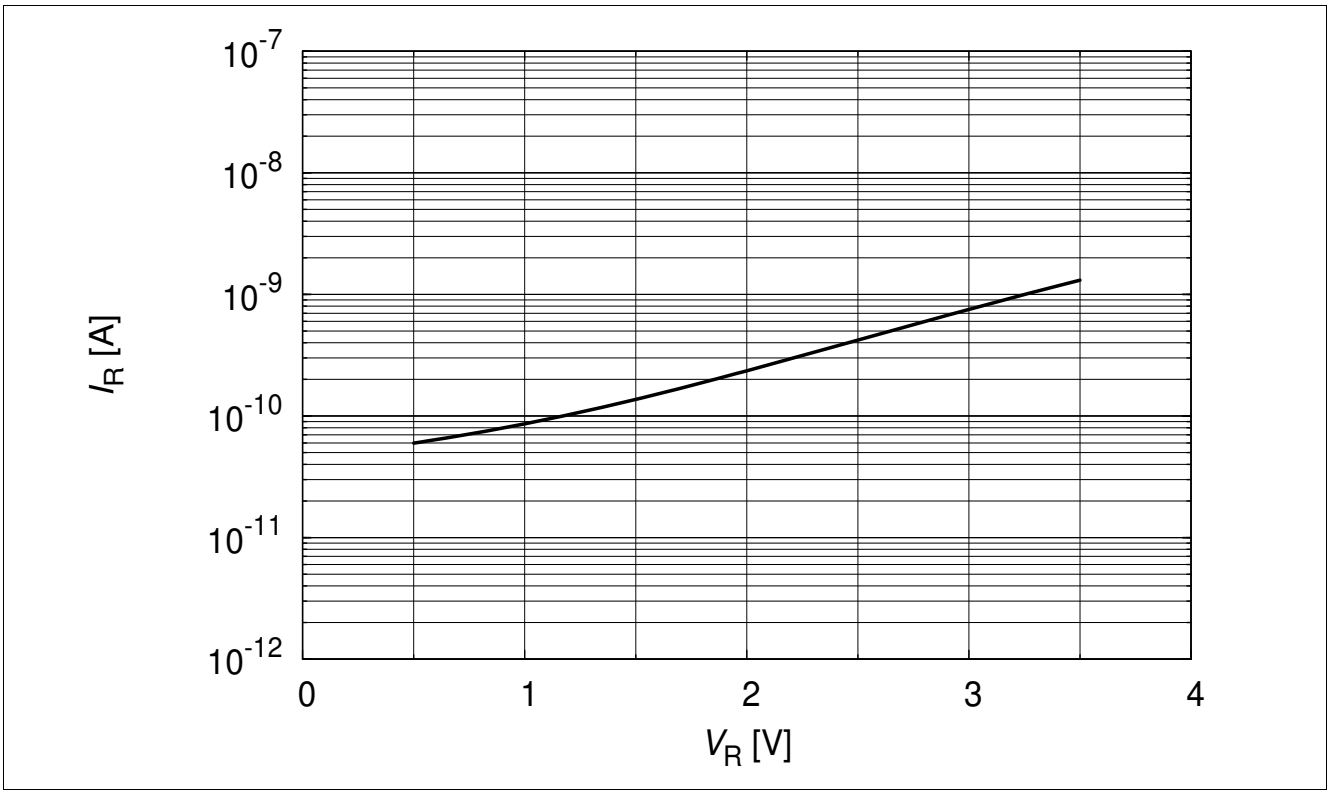

Figure 3 Reverse current, $I_R = (V_R)$

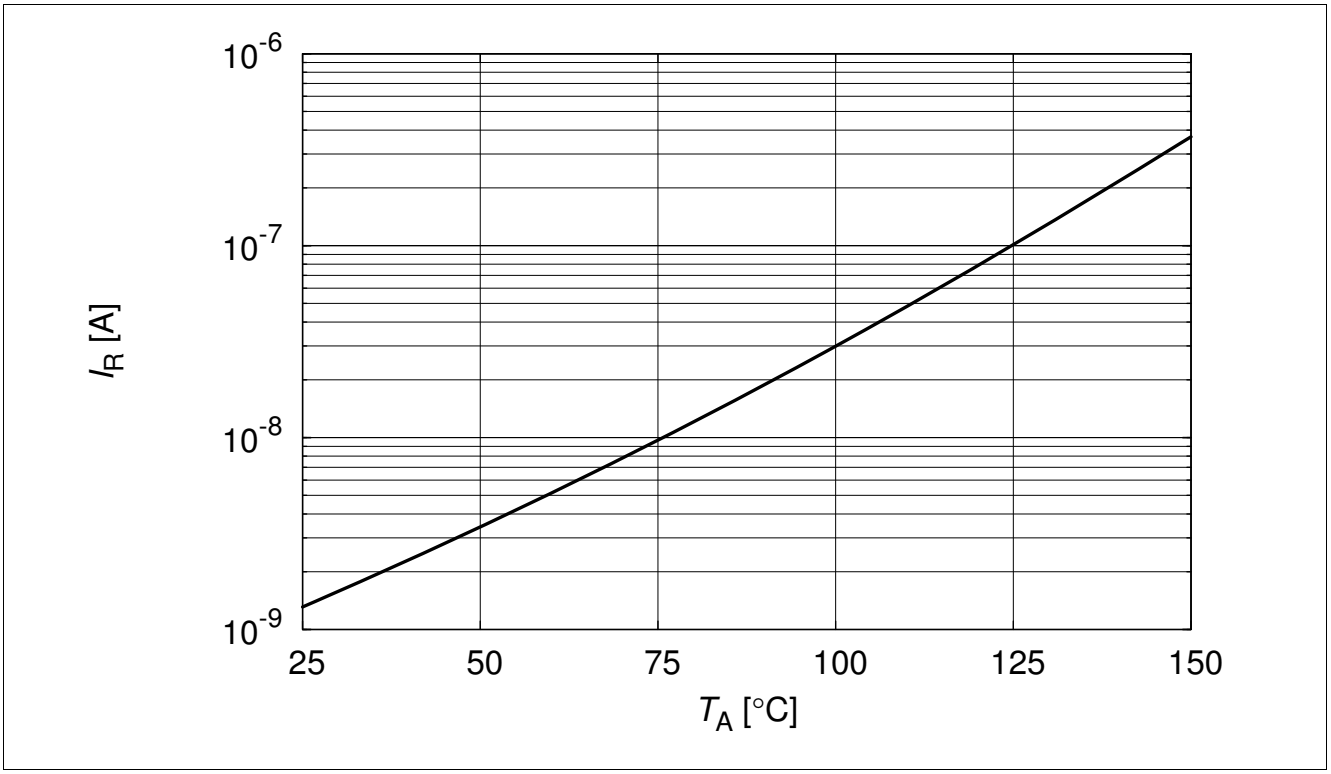

Figure 4 Reverse current: $I_R = f(T_A)$, V_R = 3.3 V

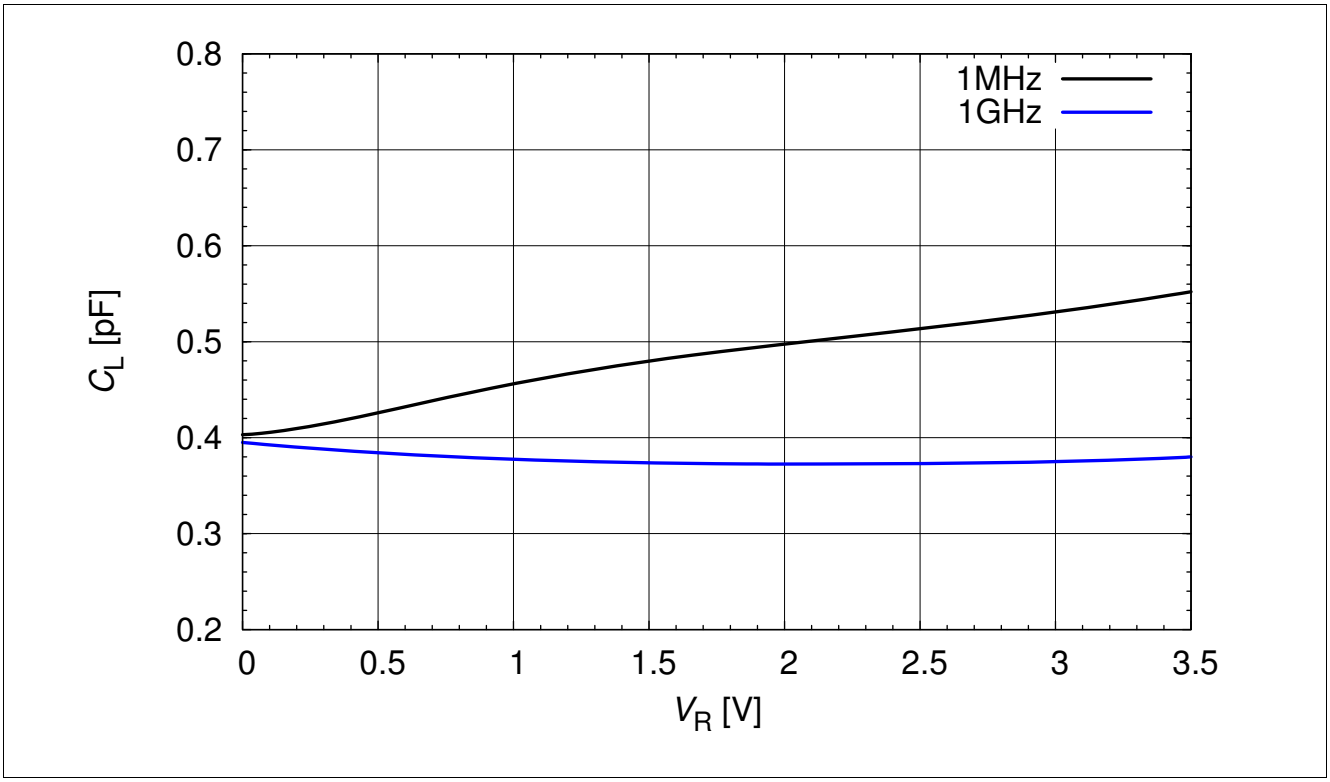

Figure 5 Line capacitance: $C_L = f(V_R)$, f = 1MHz, from I/O to GND

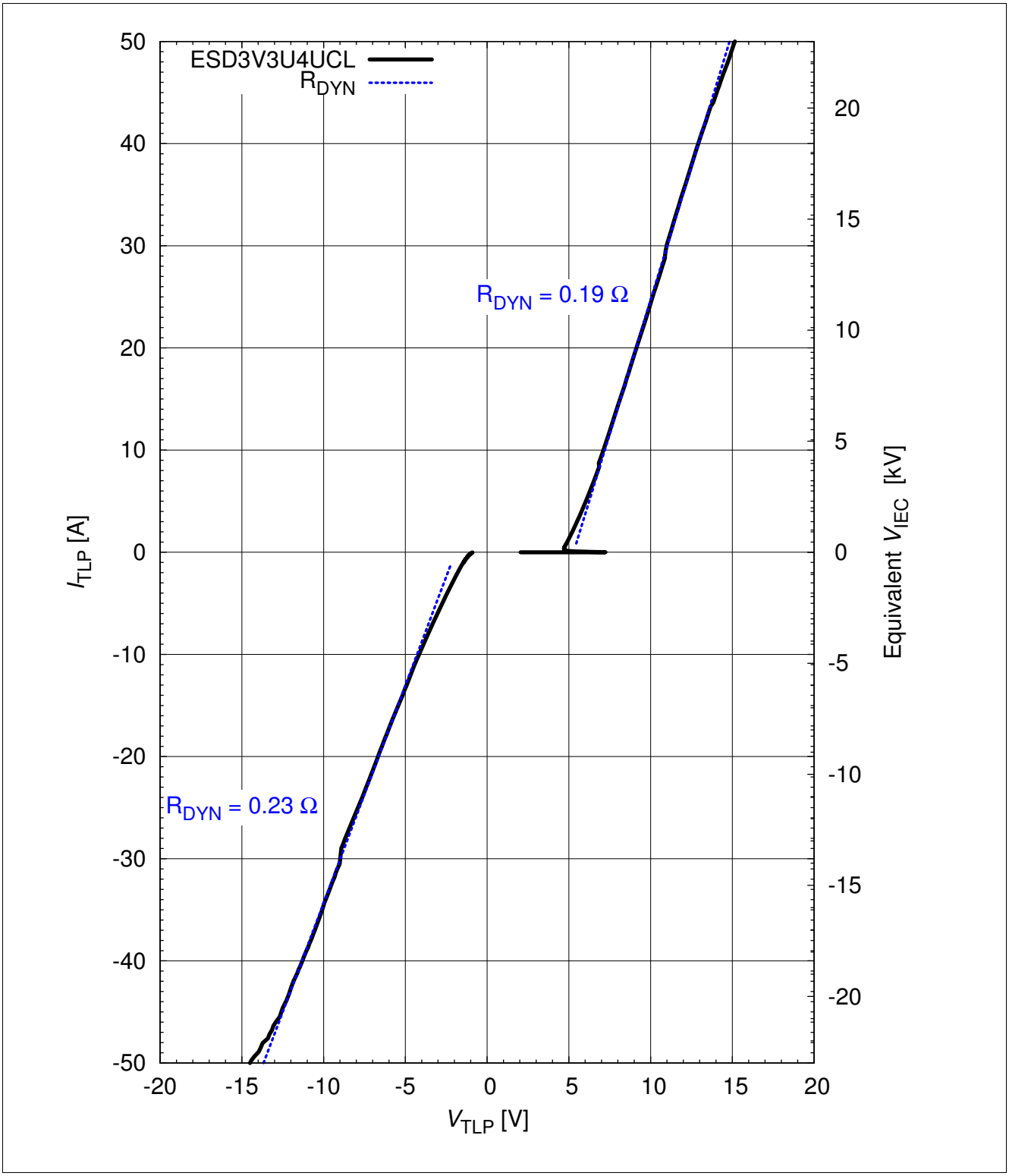

Figure 6 **Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between I_{TLP1} = 10 A and I_{TLP2} = 40 A. Please refer to Application Note AN210[2]**

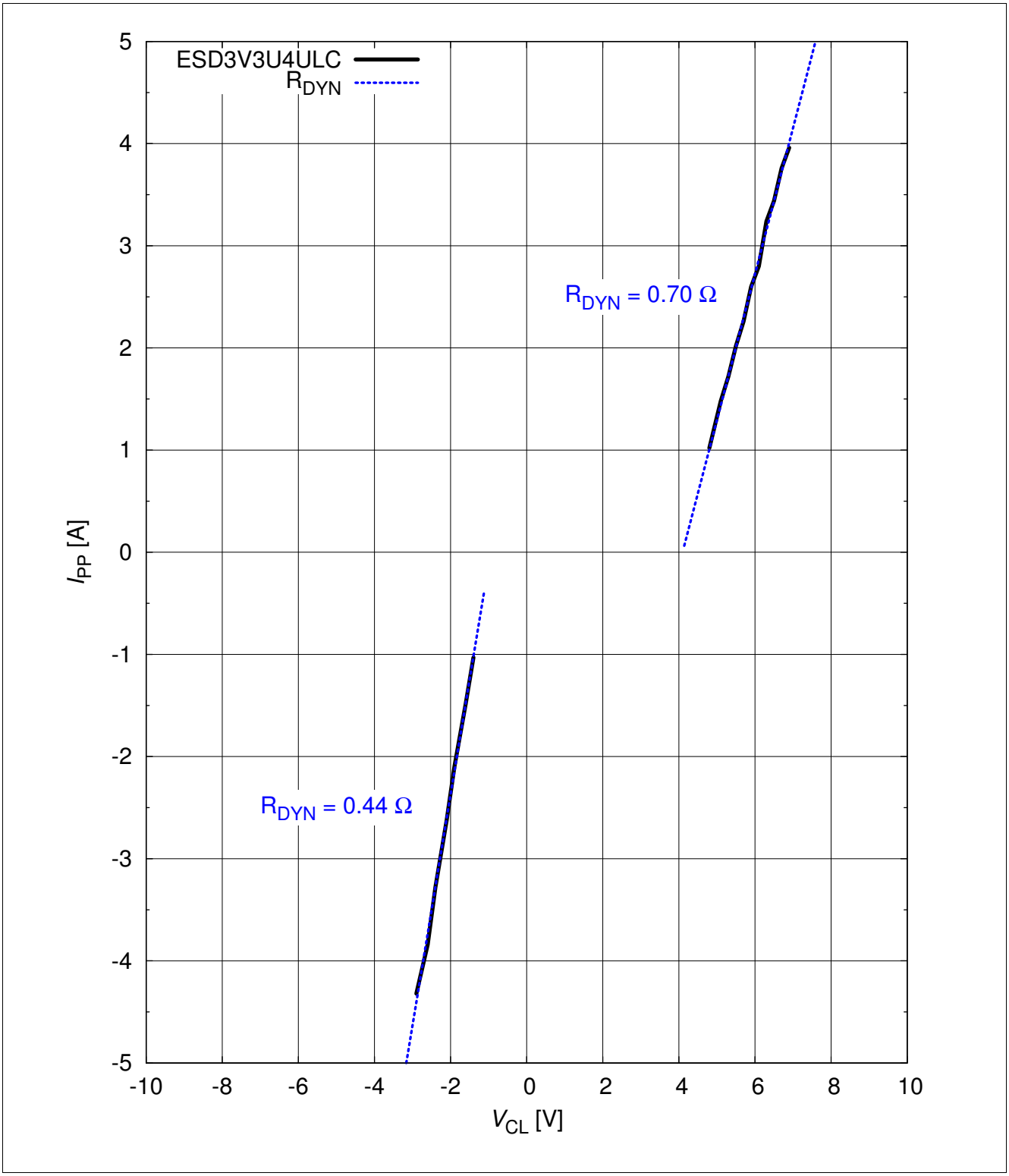

Figure 7 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

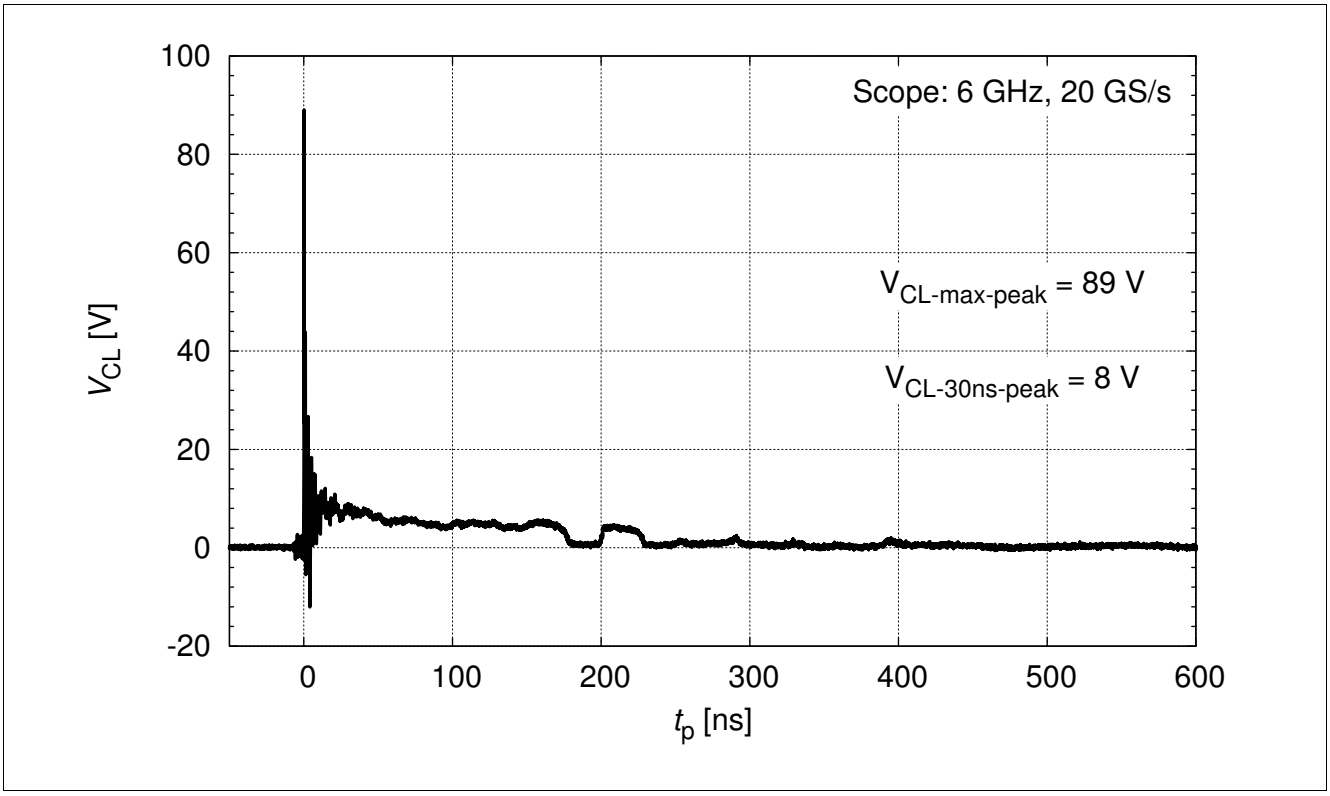

Figure 8 Clamping voltage at +8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

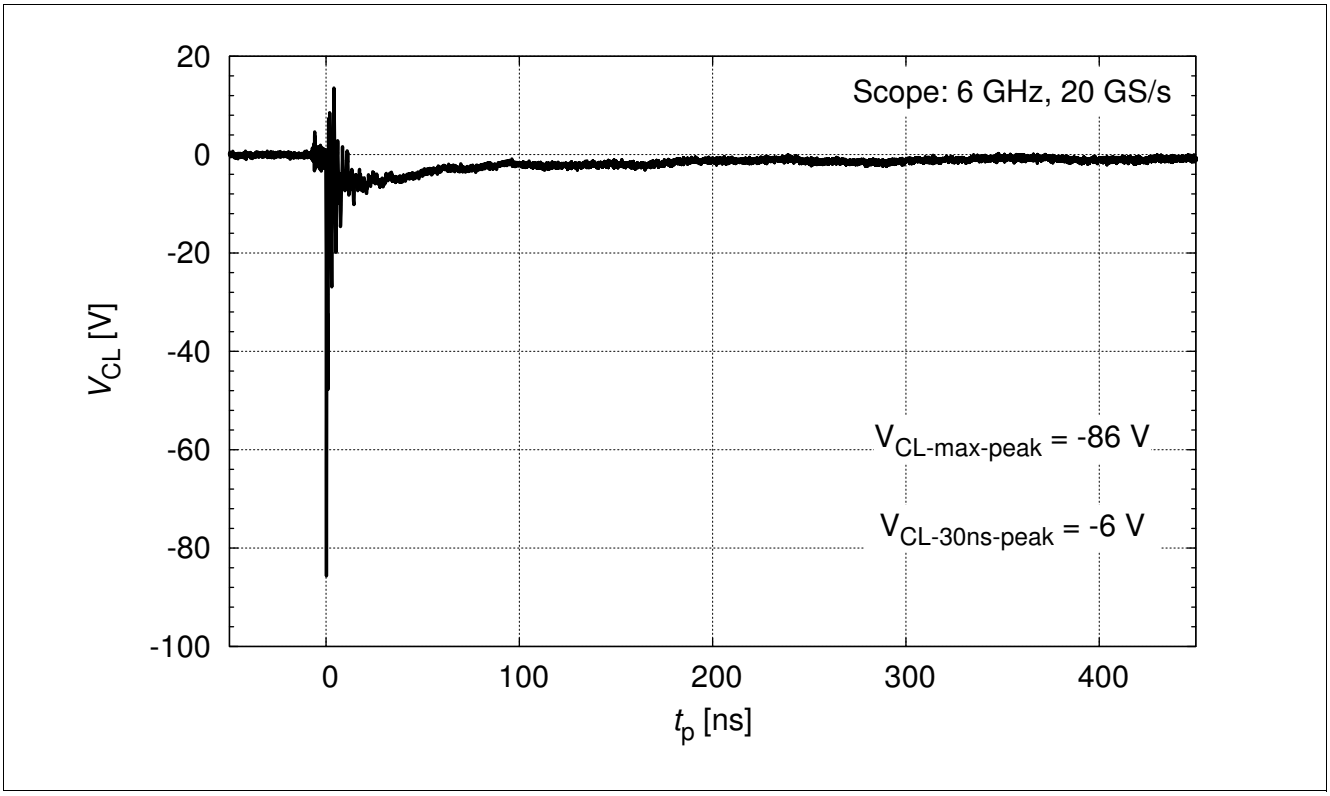

Figure 9 Clamping voltage at -8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

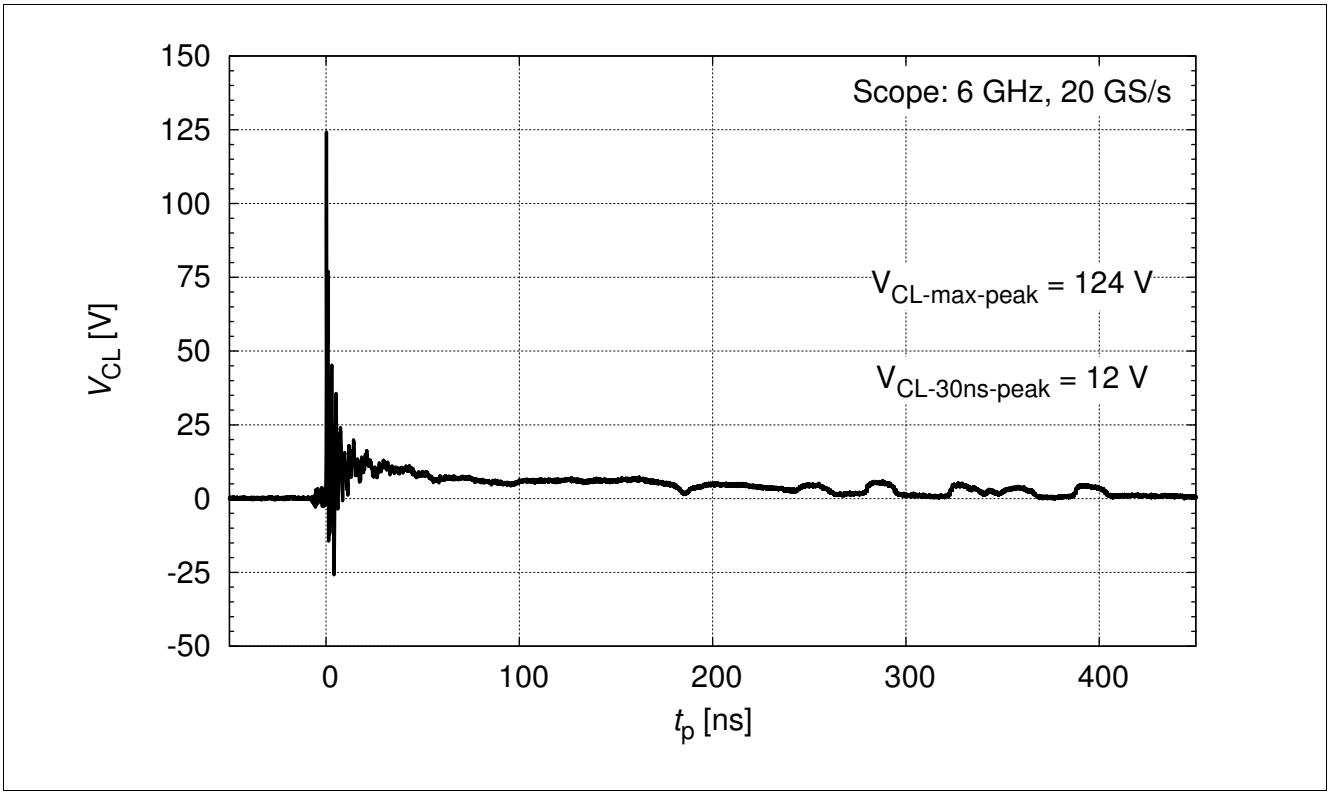

Figure 10 Clamping voltage at +15 kV discharge according IEC61000-4-2 (R = 330 Ohm, C = 150 pF)

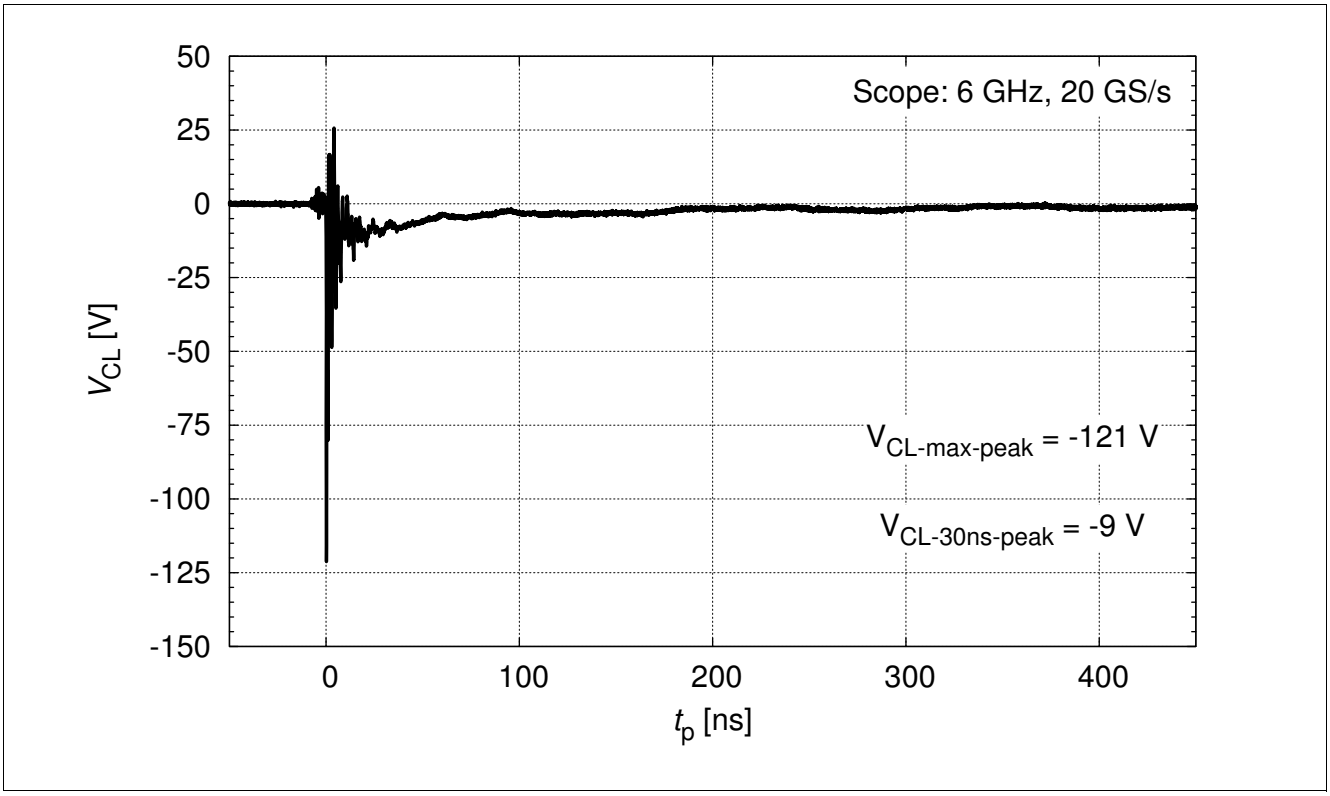

Figure 11 Clamping voltage at -15 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

4 Application Information

To design USB3.0 link for best system level ESD performance and error free Signal Integrity is mandatory.

To bring both requirements together, the ESD protection devices has to provide excellent ESD and a very low device capacitance. The Infineon ESD3V3U4ULC in “array” configuration, combined with a clear and straight forward “full through” layout fulfills these requirements in the best way.

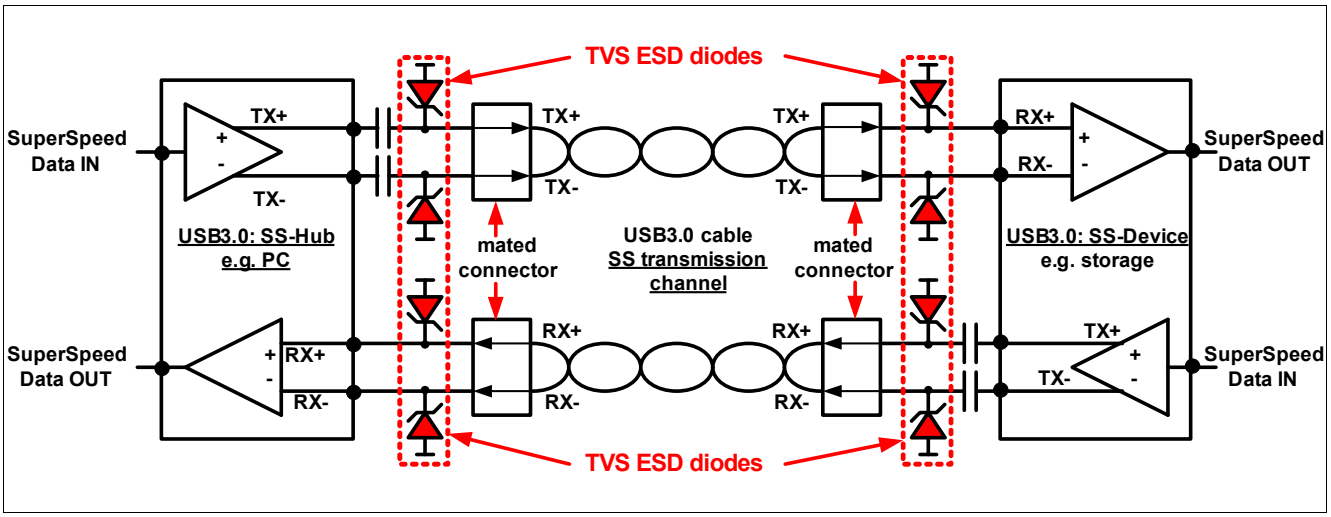

Figure 12 USB3.0 structure with ESD protection devices [3]

5 Ordering Information Scheme

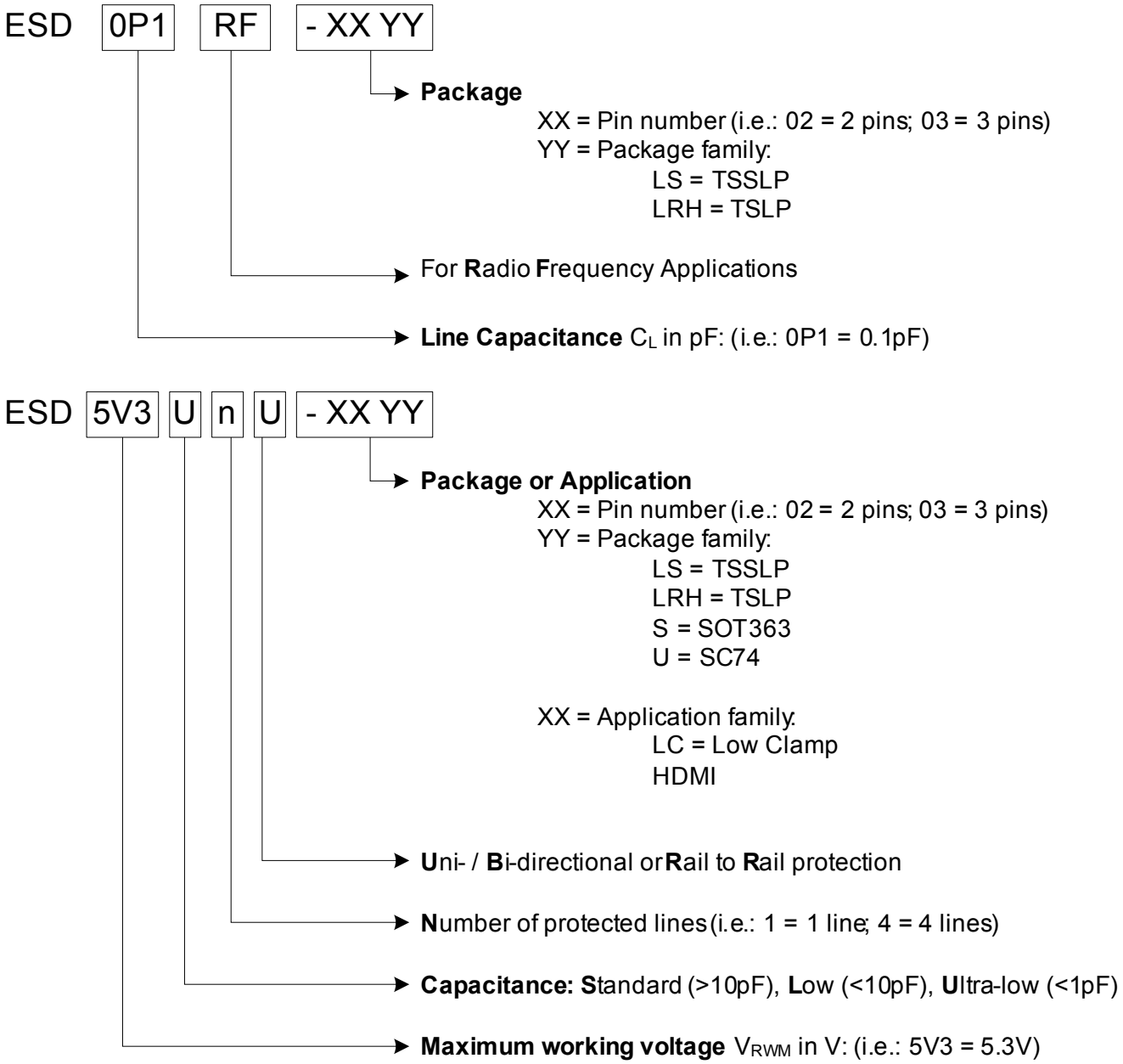

Figure 13 Ordering information scheme

6 Package Information

6.1 TSLP-9-1 (mm)

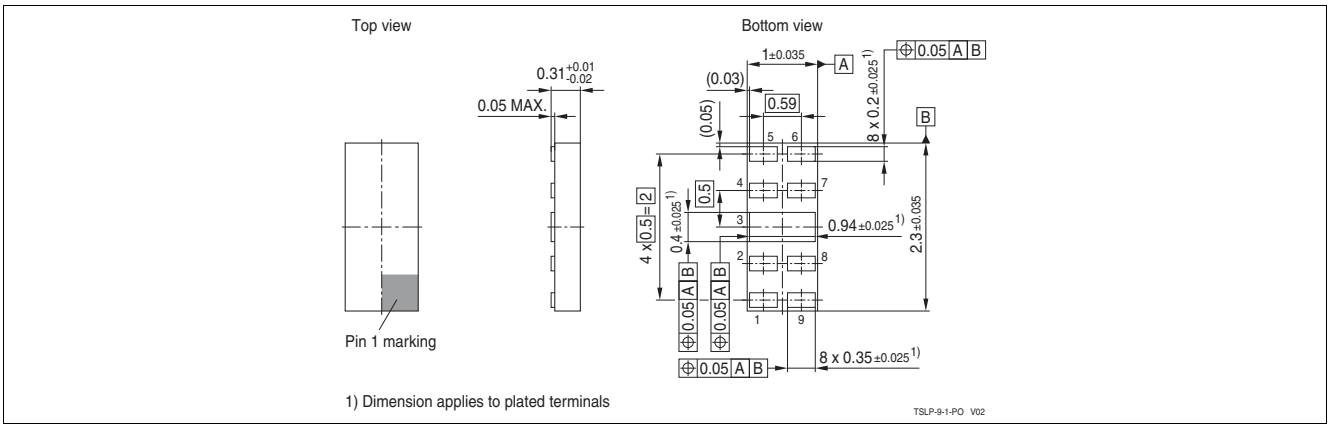

Figure 14 TSLP-9-1: Package overview

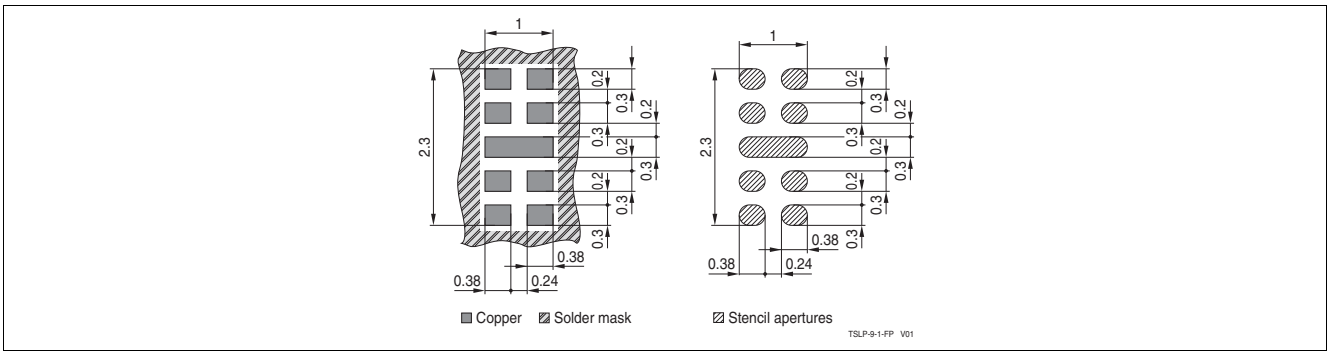

Figure 15 TSLP-9-1: Footprint

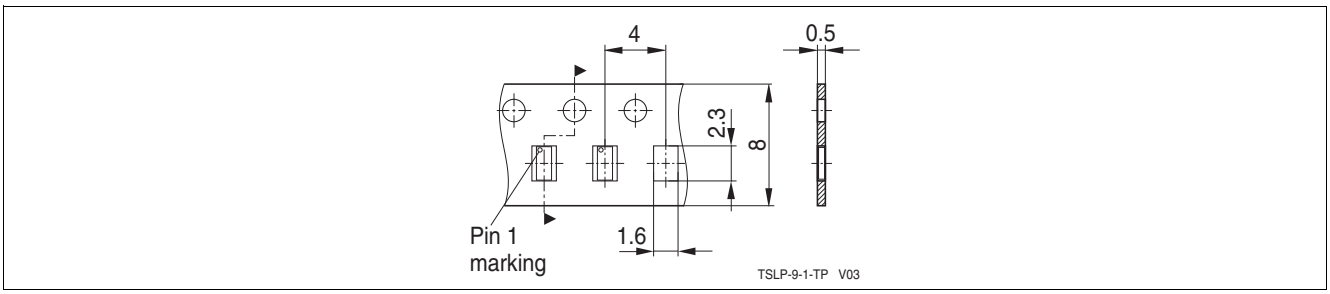

Figure 16 TSLP-9-1: Packing

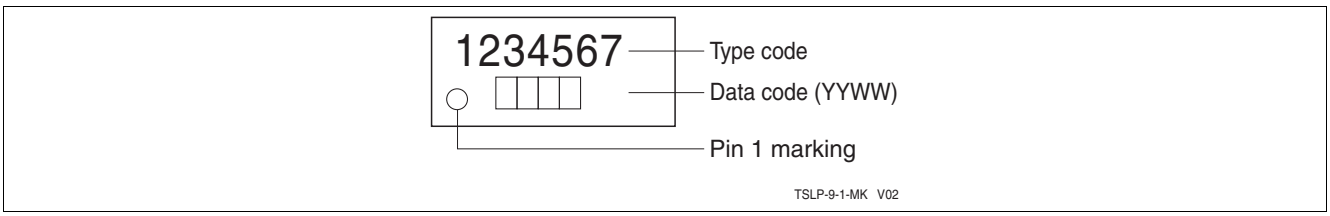

Figure 17 TSLP-9-1: Marking

References

[1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon Technologie AG - **Application Note AN240**: Effective ESD Protection for USB3.0, combined with perfect Signal Intergrity.

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