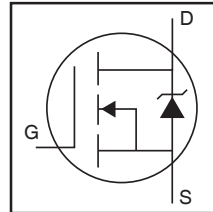


# IRFB4510GPbF

HEXFET® Power MOSFET

## Applications

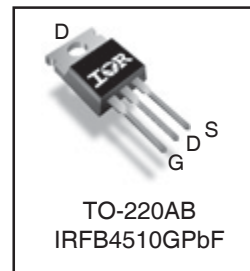
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



|                         |      |               |
|-------------------------|------|---------------|
| $V_{DSS}$               |      | <b>100V</b>   |
| $R_{DS(on)}$            | typ. | <b>10.7mΩ</b> |
|                         | max. | <b>13.5mΩ</b> |
| $I_D$ (Silicon Limited) |      | <b>62A</b>    |

## Benefits

- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free
- Halogen-Free



|          |          |          |
|----------|----------|----------|
| <b>G</b> | <b>D</b> | <b>S</b> |
| Gate     | Drain    | Source   |

## Absolute Maximum Ratings

| Symbol                          | Parameter   | Max.             | Units            |
|---------------------------------|---|------------------|------------------|
| $I_D @ T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) | 62               | A                |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) | 44               |                  |
| $I_{DM}$                        | Pulsed Drain Current ①  | 250              |                  |
| $P_D @ T_C = 25^\circ\text{C}$  | Maximum Power Dissipation   | 140              | W                |
|                                 | Linear Derating Factor  | 0.95             |                  |
| $V_{GS}$                        | Gate-to-Source Voltage  | $\pm 20$         | V                |
| $dv/dt$                         | Peak Diode Recovery ③   | 3.2              | V/ns             |
| $T_J$                           | Operating Junction and Storage Temperature Range                  | -55 to + 175     | $^\circ\text{C}$ |
| $T_{STG}$                       |   |                  |                  |
|                                 | Soldering Temperature, for 10 seconds (1.6mm from case)           | 300              |                  |
|                                 | Mounting torque, 6-32 or M3 screw                                 | 10lb·in (1.1N·m) |                  |

## Avalanche Characteristics

|                              |                                 |                            |    |
|------------------------------|---------------------------------|----------------------------|----|
| $E_{AS}$ (Thermally limited) | Single Pulse Avalanche Energy ② | 130                        | mJ |
| $I_{AR}$                     | Avalanche Current               | See Fig. 14, 15, 22a, 22b, | A  |
| $E_{AR}$                     | Repetitive Avalanche Energy ④   |                            | mJ |

## Thermal Resistance

| Symbol          | Parameter                          | Typ. | Max. | Units              |
|-----------------|------------------------------------|------|------|--------------------|
| $R_{\theta JC}$ | Junction-to-Case ⑦                 | —    | 1.05 | $^\circ\text{C/W}$ |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface | 0.50 | —    |                    |
| $R_{\theta JA}$ | Junction-to-Ambient, TO-220 ⑦      | —    | 62   |                    |

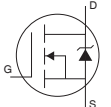
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

| Symbol                               | Parameter                            | Min. | Typ. | Max. | Units | Conditions  |
|--------------------------------------|--------------------------------------|------|------|------|-------|---|
| V <sub>(BR)DSS</sub>                 | Drain-to-Source Breakdown Voltage    | 100  | —    | —    | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA                        |
| ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub> | Breakdown Voltage Temp. Coefficient  | —    | 0.11 | —    | V/°C  | Reference to 25°C, I <sub>D</sub> = 5mA <sup>①</sup>                |
| R <sub>DS(on)</sub>                  | Static Drain-to-Source On-Resistance | —    | 10.7 | 13.5 | mΩ    | V <sub>GS</sub> = 10V, I <sub>D</sub> = 37A <sup>④</sup>            |
| V <sub>GS(th)</sub>                  | Gate Threshold Voltage               | 2.0  | —    | 4.0  | V     | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA          |
| I <sub>DSS</sub>                     | Drain-to-Source Leakage Current      | —    | —    | 20   | μA    | V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V                        |
|                                      |                                      | —    | —    | 250  |       | V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C |
| I <sub>GSS</sub>                     | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA    | V <sub>GS</sub> = 20V   |
|                                      | Gate-to-Source Reverse Leakage       | —    | —    | -100 |       | V <sub>GS</sub> = -20V  |
| R <sub>G</sub>                       | Internal Gate Resistance             | —    | 0.6  | —    | Ω     |   |

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

| Symbol                     | Parameter   | Min. | Typ. | Max. | Units | Conditions   |
|----------------------------|---|------|------|------|-------|--|
| g <sub>fs</sub>            | Forward Transconductance                                    | 100  | —    | —    | S     | V <sub>DS</sub> = 25V, I <sub>D</sub> = 37A                                    |
| Q <sub>g</sub>             | Total Gate Charge   | —    | 58   | 87   | nC    | I <sub>D</sub> = 37A   |
| Q <sub>gs</sub>            | Gate-to-Source Charge                                       | —    | 14   | —    |       | V <sub>DS</sub> = 50V  |
| Q <sub>gd</sub>            | Gate-to-Drain ("Miller") Charge                             | —    | 18   | —    |       | V <sub>GS</sub> = 10V <sup>④</sup>   |
| Q <sub>sync</sub>          | Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> ) | —    | 40   | —    |       | I <sub>D</sub> = 37A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V <sup>④</sup> |
| t <sub>d(on)</sub>         | Turn-On Delay Time  | —    | 13   | —    | ns    | V <sub>DD</sub> = 65V  |
| t <sub>r</sub>             | Rise Time   | —    | 32   | —    |       | I <sub>D</sub> = 37A   |
| t <sub>d(off)</sub>        | Turn-Off Delay Time   | —    | 28   | —    |       | R <sub>G</sub> = 2.7Ω  |
| t <sub>f</sub>             | Fall Time   | —    | 28   | —    |       | V <sub>GS</sub> = 10V <sup>④</sup>   |
| C <sub>iss</sub>           | Input Capacitance   | —    | 3180 | —    | pF    | V <sub>GS</sub> = 0V   |
| C <sub>oss</sub>           | Output Capacitance  | —    | 220  | —    |       | V <sub>DS</sub> = 50V  |
| C <sub>rss</sub>           | Reverse Transfer Capacitance                                | —    | 120  | —    |       | f = 1.0MHz, See Fig.5  |
| C <sub>oss eff. (ER)</sub> | Effective Output Capacitance (Energy Related) <sup>⑤</sup>  | —    | 260  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V <sup>⑥</sup> , See Fig.1     |
| C <sub>oss eff. (TR)</sub> | Effective Output Capacitance (Time Related) <sup>⑤</sup>    | —    | 325  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V <sup>⑤</sup>                 |

**Diode Characteristics**

| Symbol           | Parameter                                       | Min.   | Typ. | Max. | Units | Conditions  |
|------------------|---|--|------|------|-------|---|
| I <sub>S</sub>   | Continuous Source Current (Body Diode)          | —  | —    | 62   | A     | MOSFET symbol showing the integral reverse p-n junction diode.                        |
| I <sub>SM</sub>  | Pulsed Source Current (Body Diode) <sup>①</sup> | —  | —    | 250  | A     |  |
| V <sub>SD</sub>  | Diode Forward Voltage                           | —  | —    | 1.3  | V     | T <sub>J</sub> = 25°C, I <sub>S</sub> = 37A, V <sub>GS</sub> = 0V <sup>④</sup>        |
| t <sub>rr</sub>  | Reverse Recovery Time                           | —  | 54   | 81   | ns    | T <sub>J</sub> = 25°C V <sub>R</sub> = 85V,   |
|                  |   | —  | 60   | 90   |       | T <sub>J</sub> = 125°C I <sub>F</sub> = 37A   |
| Q <sub>rr</sub>  | Reverse Recovery Charge                         | —  | 95   | 140  | nC    | T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>④</sup>                                    |
|                  |   | —  | 130  | 195  |       | T <sub>J</sub> = 125°C  |
| I <sub>RRM</sub> | Reverse Recovery Current                        | —  | 3.3  | —    | A     | T <sub>J</sub> = 25°C   |
| t <sub>on</sub>  | Forward Turn-On Time                            | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) |      |      |       |   |

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.192mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 37A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 37A, di/dt ≤ 1550A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.

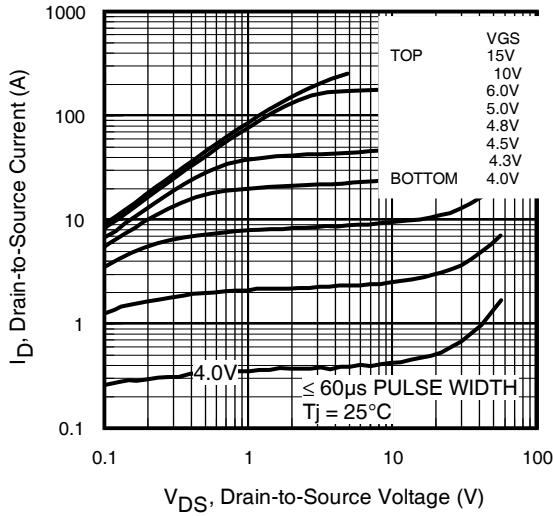


Fig 1. Typical Output Characteristics

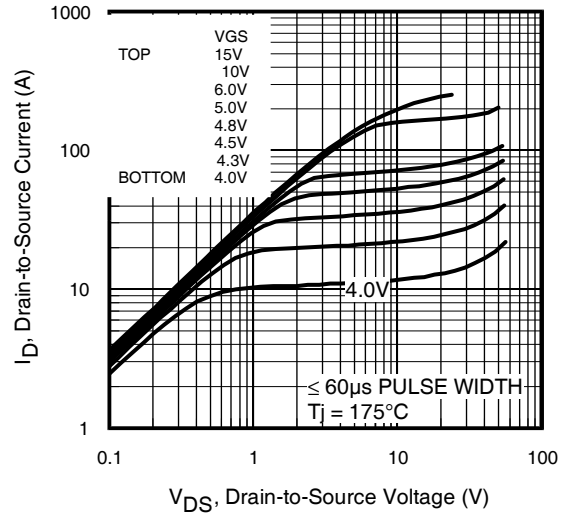


Fig 2. Typical Output Characteristics

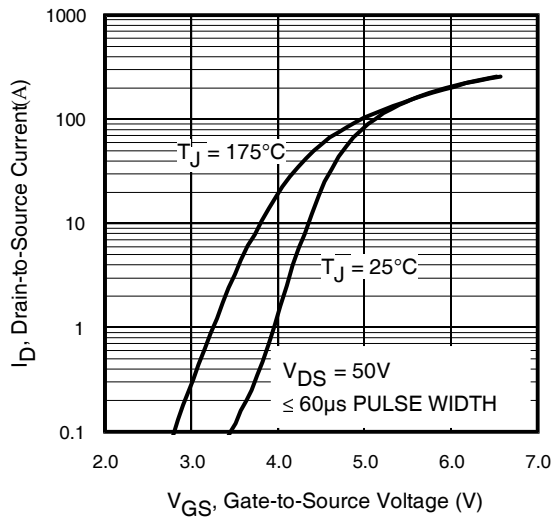


Fig 3. Typical Transfer Characteristics

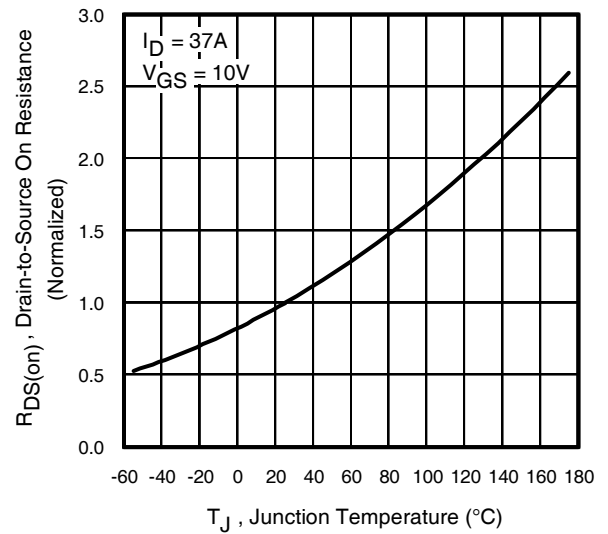


Fig 4. Normalized On-Resistance vs. Temperature

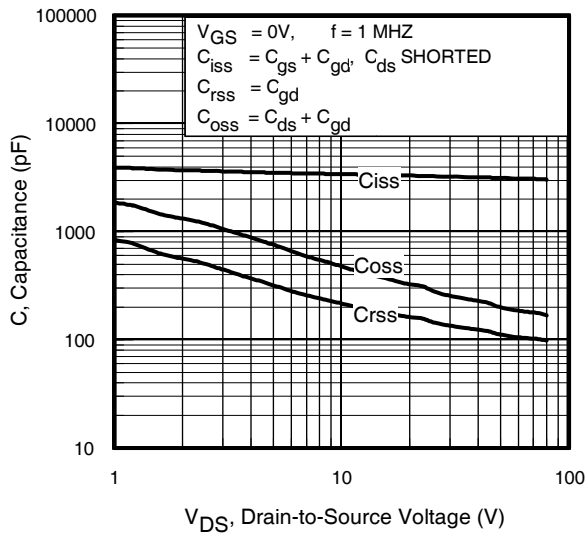


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

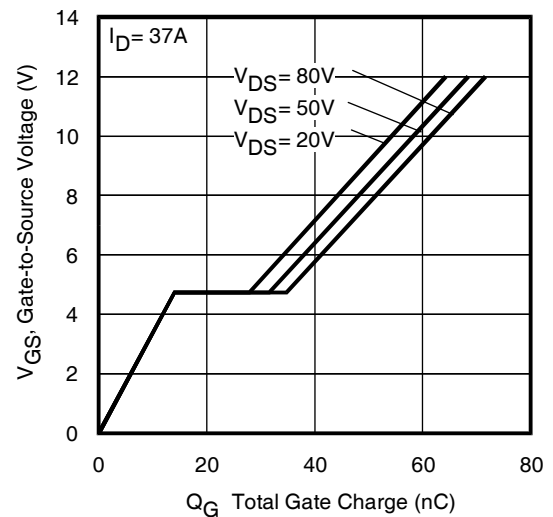


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

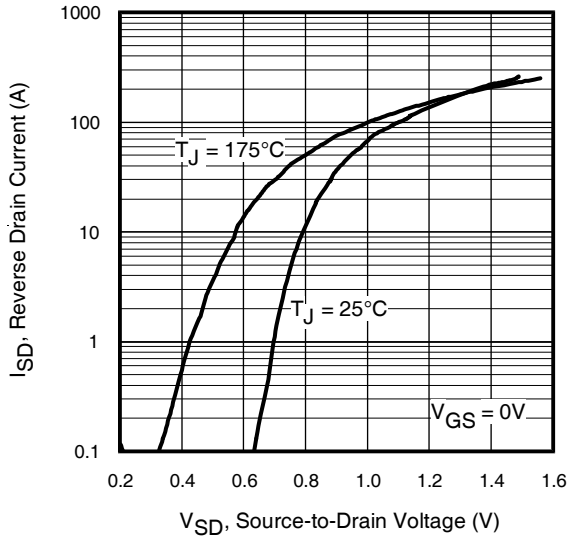


Fig 7. Typical Source-Drain Diode Forward Voltage

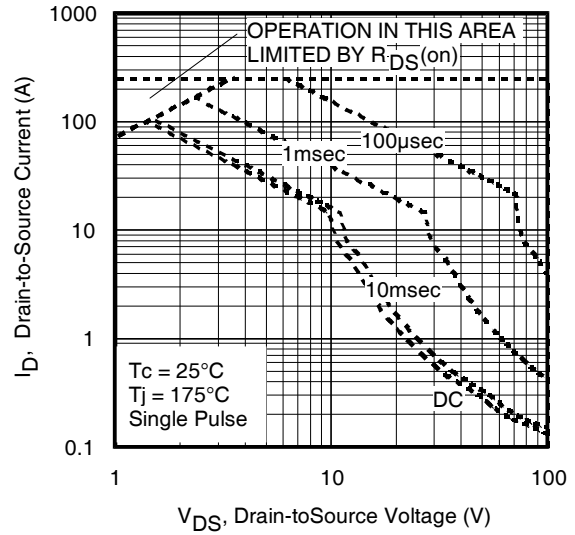


Fig 8. Maximum Safe Operating Area

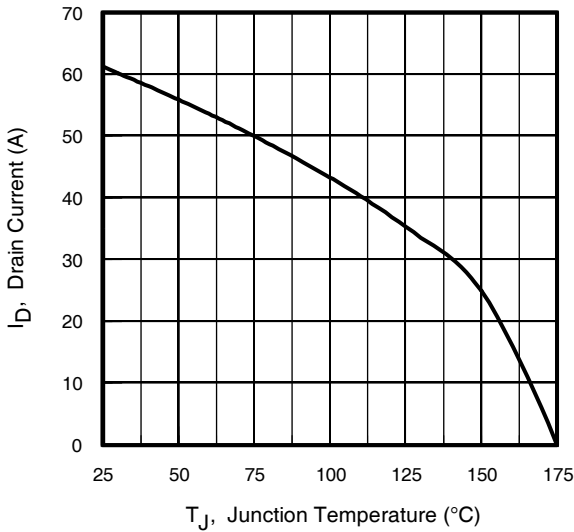


Fig 9. Maximum Drain Current vs. Case Temperature

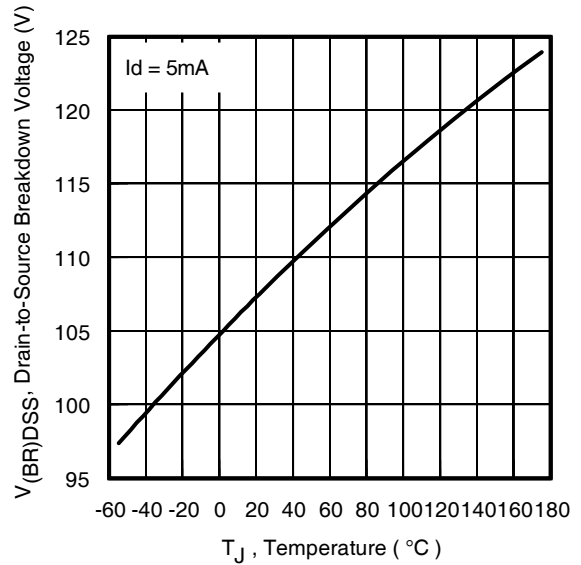


Fig 10. Drain-to-Source Breakdown Voltage

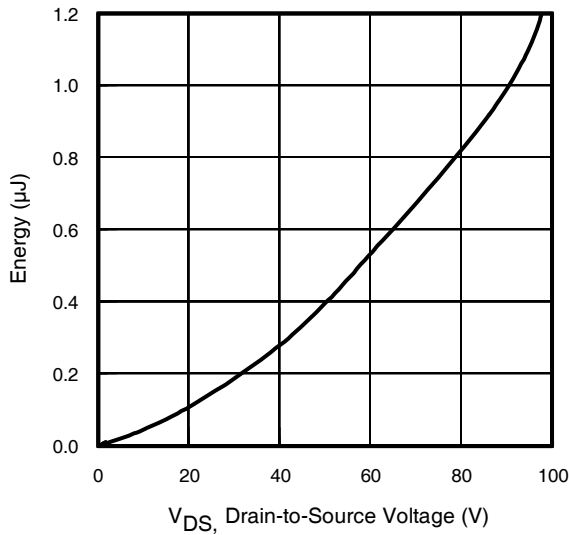


Fig 11. Typical  $C_{OSS}$  Stored Energy

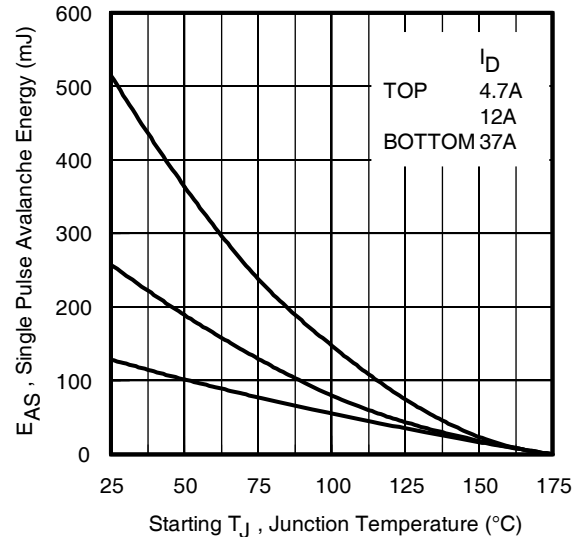


Fig 12. Maximum Avalanche Energy vs. Drain Current

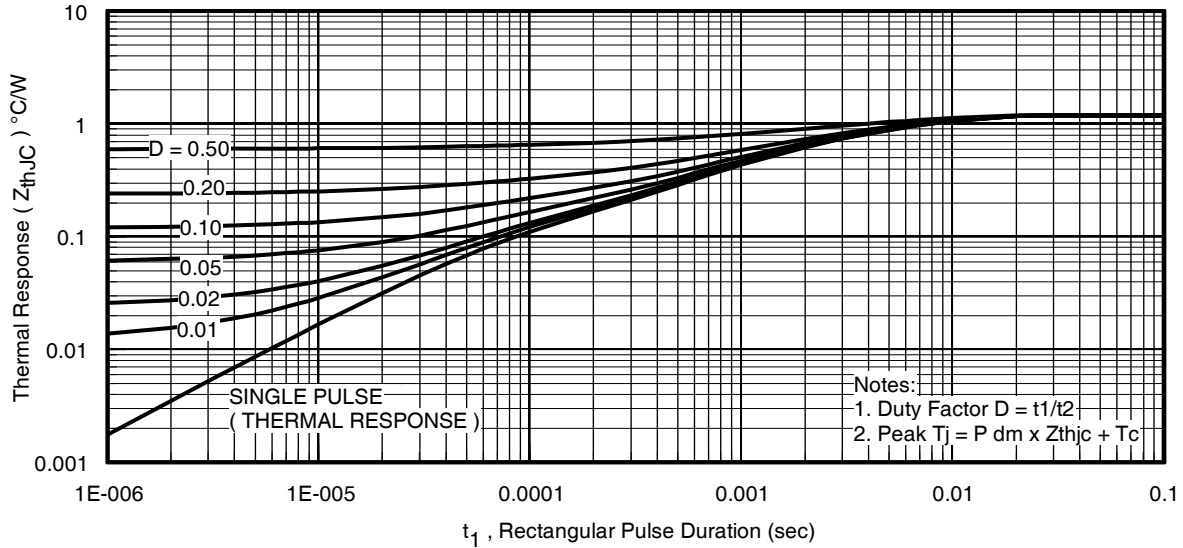


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

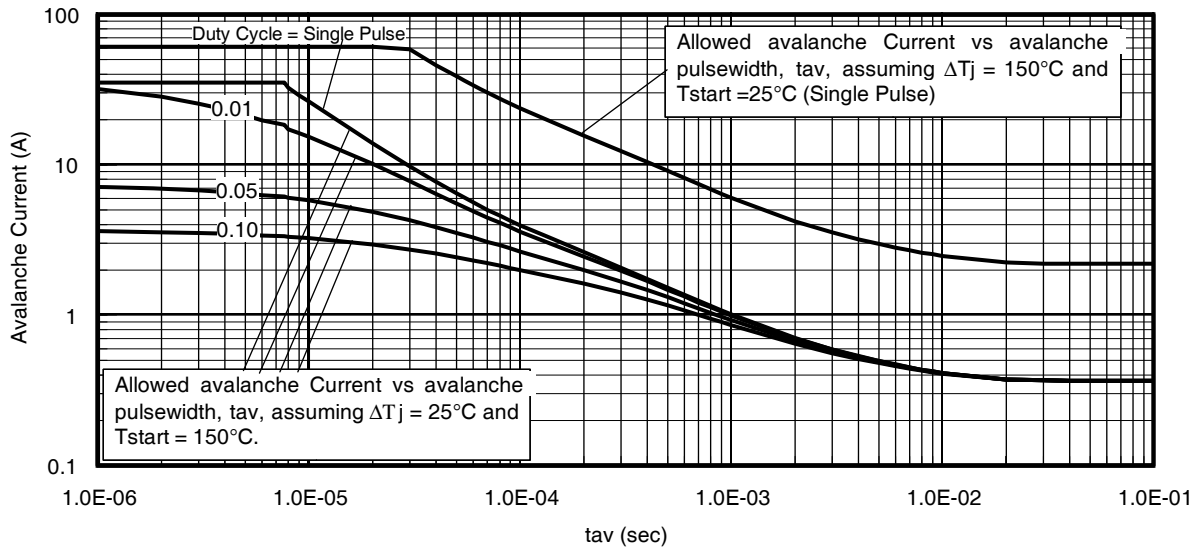


Fig 14. Typical Avalanche Current vs. Pulsewidth

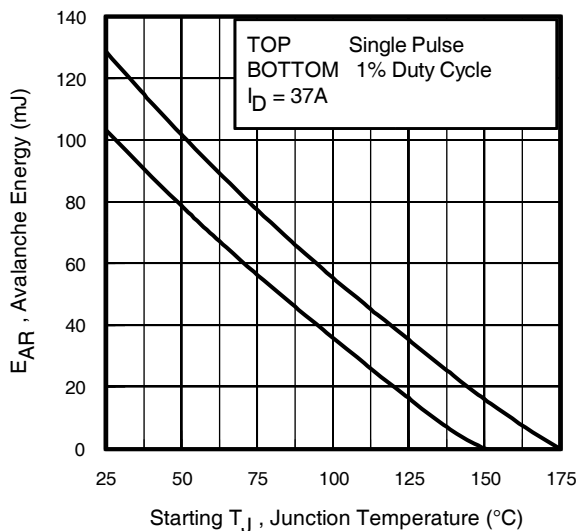


Fig 15. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

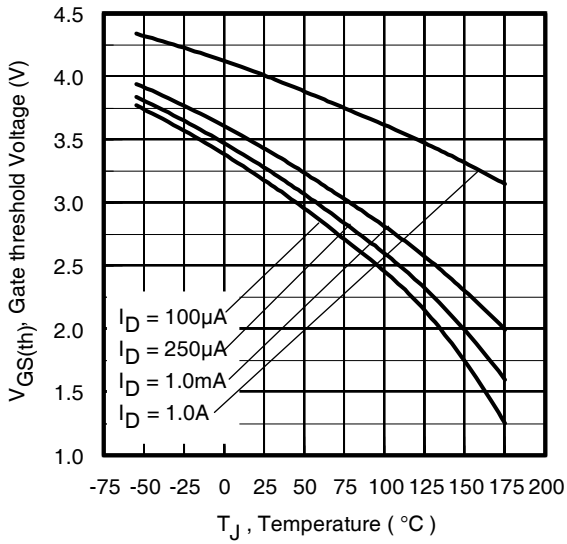


Fig 16. Threshold Voltage vs. Temperature

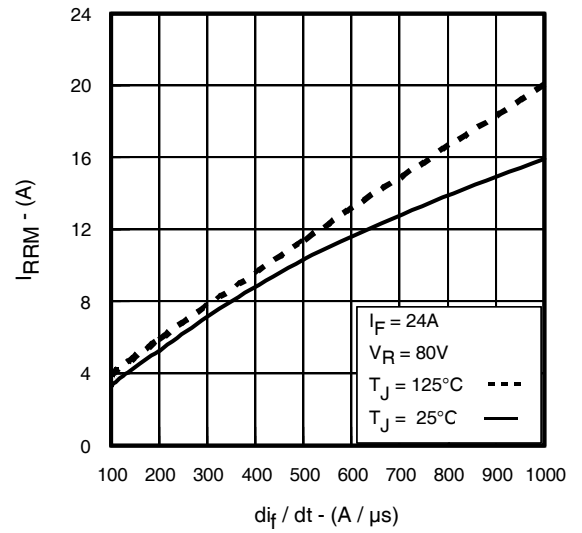


Fig. 17 - Typical Recovery Current vs.  $di_f/dt$

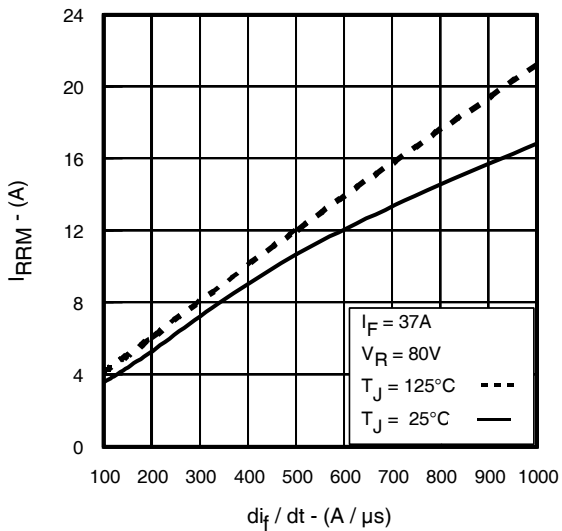


Fig. 18 - Typical Recovery Current vs.  $di_f/dt$

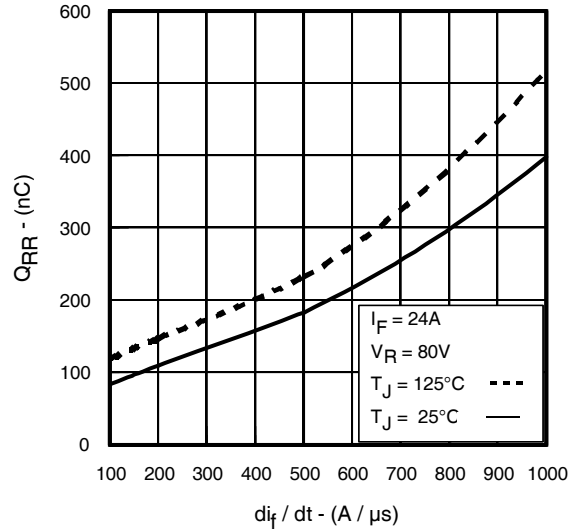


Fig. 19 - Typical Stored Charge vs.  $di_f/dt$

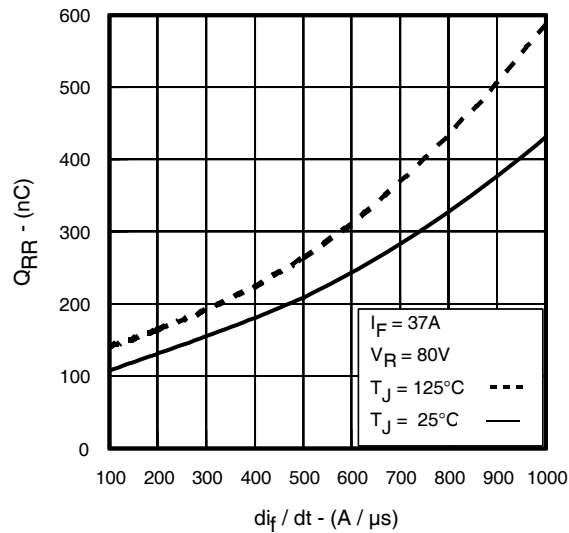
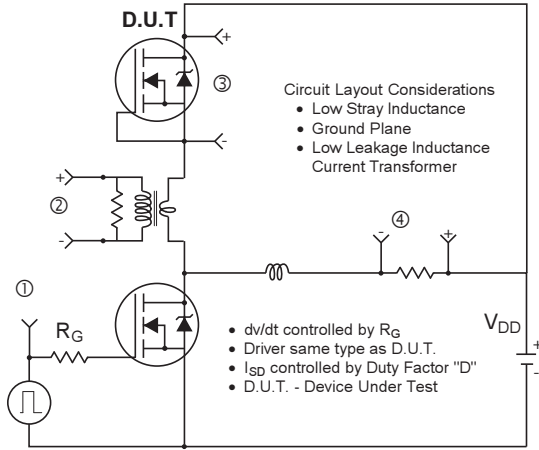
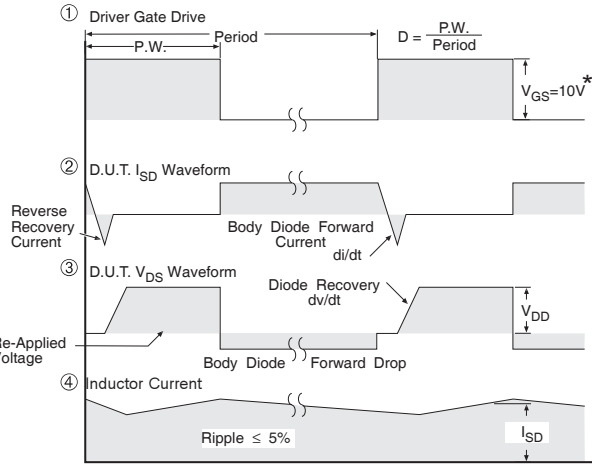


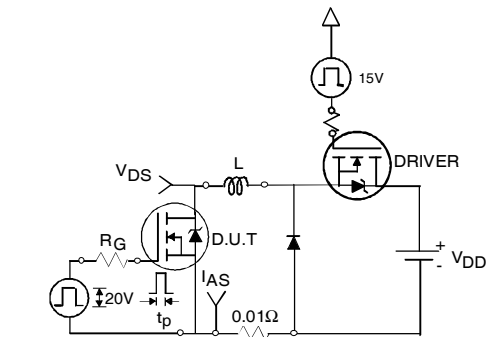
Fig. 20 - Typical Stored Charge vs.  $di_f/dt$



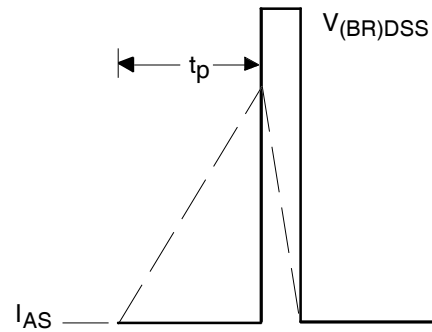
**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



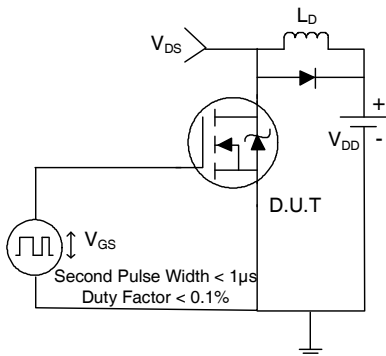
\*  $V_{GS} = 5V$  for Logic Level Devices



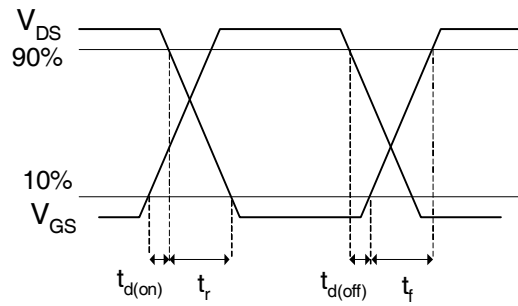
**Fig 22a. Unclamped Inductive Test Circuit**



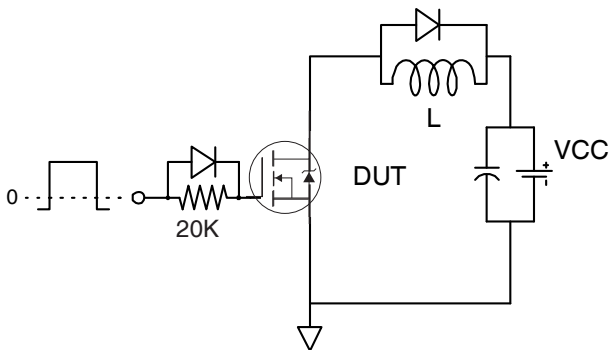
**Fig 22b. Unclamped Inductive Waveforms**



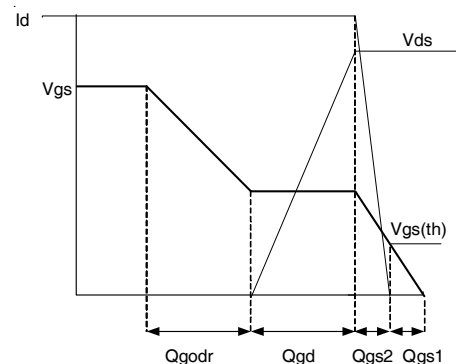
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

