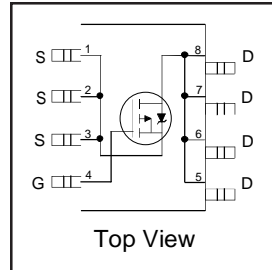


# IRF7406

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- P-Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

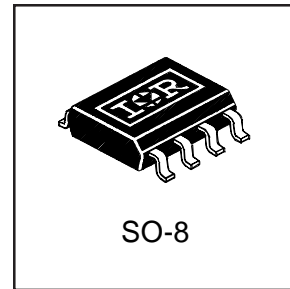


$V_{DSS} = -30V$
$R_{DS(on)} = 0.045\Omega$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



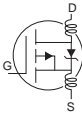
## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	10 Sec. Pulsed Drain Current, $V_{GS} @ -10V$	-6.7	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-5.8	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-3.7	
$I_{DM}$	Pulsed Drain Current $\text{\textcircled{D}}$	-23	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
dv/dt	Peak Diode Recovery dv/dt $\text{\textcircled{D}}$	-5.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to + 150	°C

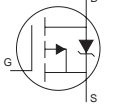
## Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient $\text{\textcircled{D}}$	---	50	°C/W

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.020	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.045	$\Omega$	$V_{GS} = -10V, I_D = -2.8A$ ③
		—	—	0.070		$V_{GS} = -4.5V, I_D = -2.4A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
$g_{fs}$	Forward Transconductance	3.1	—	—	S	$V_{DS} = -15V, I_D = -2.8A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-1.0	$\mu A$	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
$Q_g$	Total Gate Charge	—	—	59	nC	$I_D = -2.8A$
$Q_{gs}$	Gate-to-Source Charge	—	—	5.7		$V_{DS} = -2.4V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	21		$V_{GS} = -10V$ , See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = -15V$
$t_r$	Rise Time	—	33	—		$I_D = -2.8A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G = 6.0\Omega$
$t_f$	Fall Time	—	47	—		$R_D = 5.3\Omega$ , See Fig. 10 ③
$L_D$	Internal Drain Inductance	—	2.5	—	nH	Between lead tip and center of die contact 
$L_S$	Internal Source Inductance	—	4.0	—		
$C_{ISS}$	Input Capacitance	—	1100	—	pF	$V_{GS} = 0V$
$C_{OSS}$	Output Capacitance	—	490	—		$V_{DS} = -25V$
$C_{RSS}$	Reverse Transfer Capacitance	—	220	—		$f = 1.0\text{MHz}$ , See Fig. 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-23		
$V_{SD}$	Diode Forward Voltage	—	—	-1.0	V	$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	42	63	ns	$T_J = 25^\circ\text{C}, I_F = -2.8A$
$Q_{rr}$	Reverse Recovery Charge	—	64	96	nC	$di/dt = 100A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $I_{SD} \leq -2.8A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ④ Surface mounted on FR-4 board,  $t \leq 10\text{sec}$ .

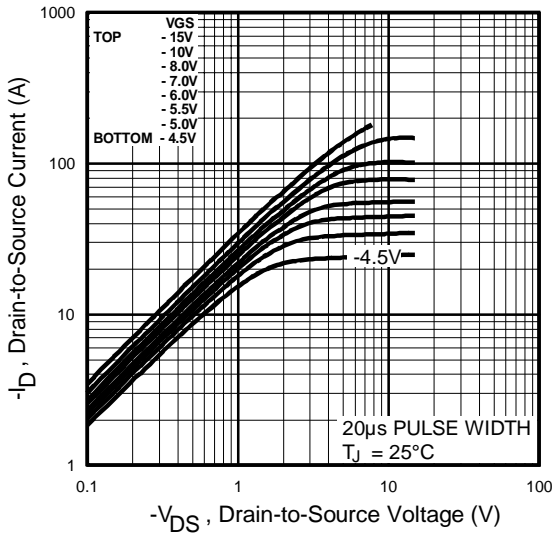


Fig 1. Typical Output Characteristics

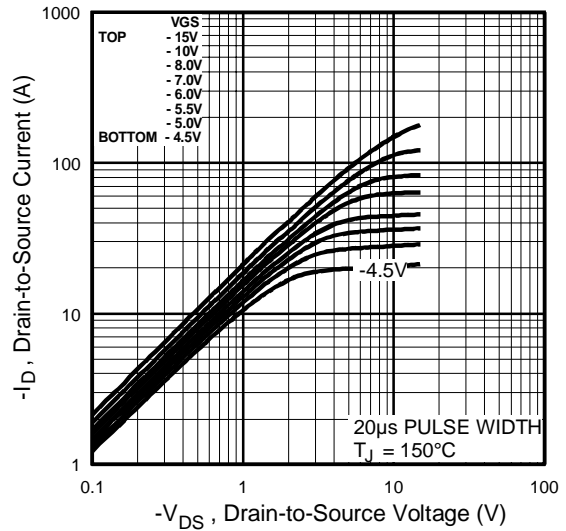


Fig 2. Typical Output Characteristics

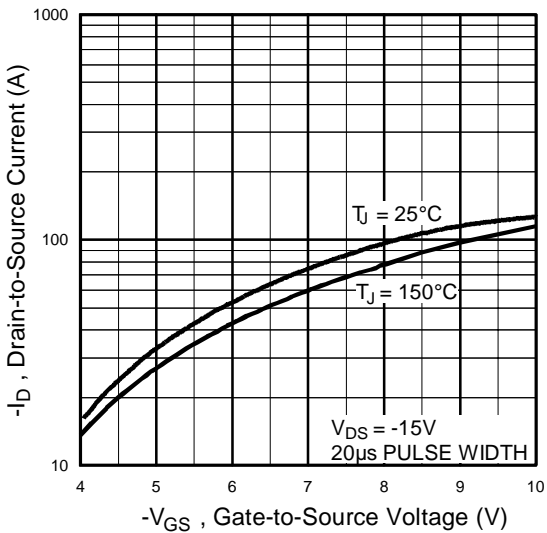


Fig 3. Typical Transfer Characteristics

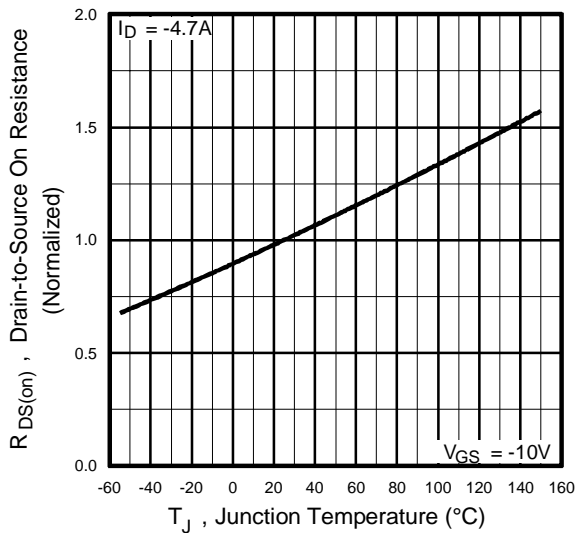
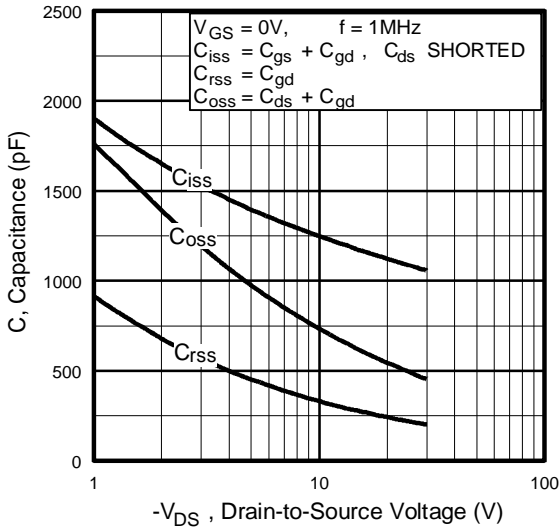
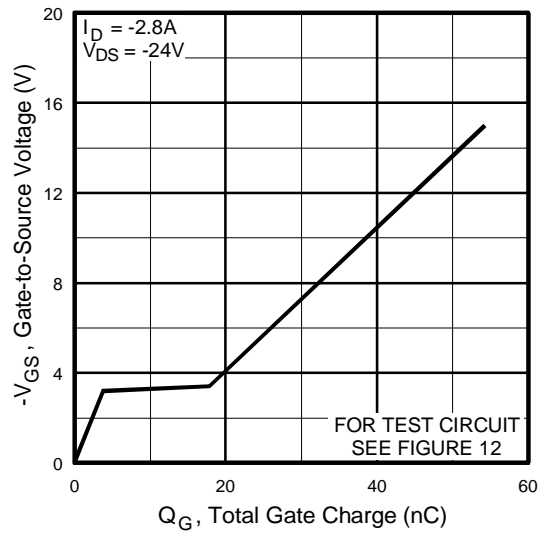


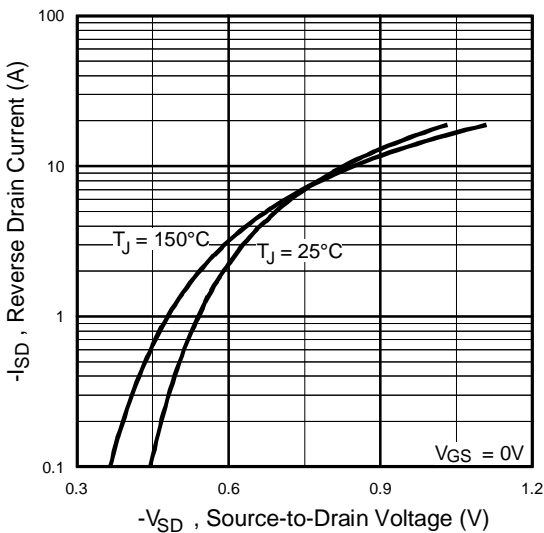
Fig 4. Normalized On-Resistance Vs. Temperature



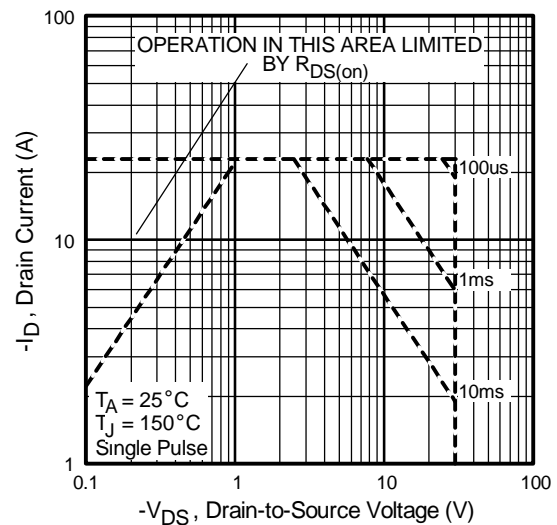
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



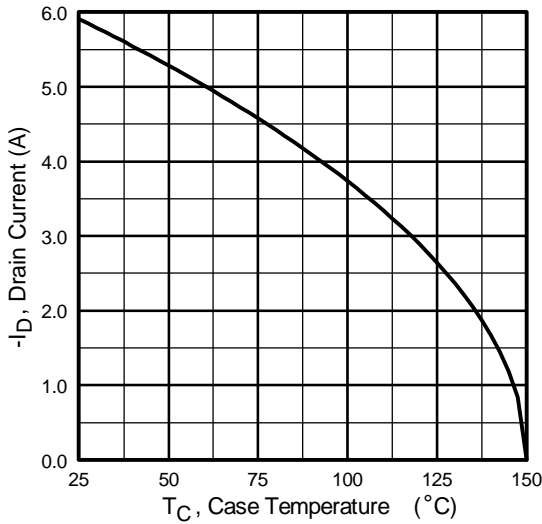
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



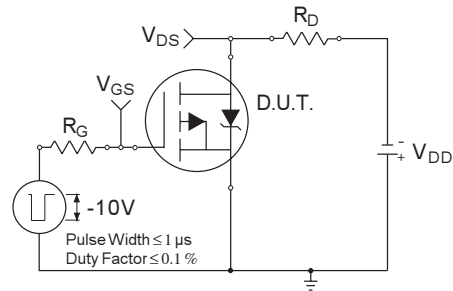
**Fig 7.** Typical Source-Drain Diode Forward Voltage



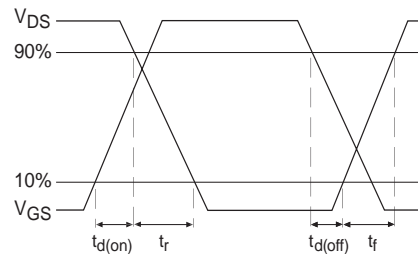
**Fig 8.** Maximum Safe Operating Area



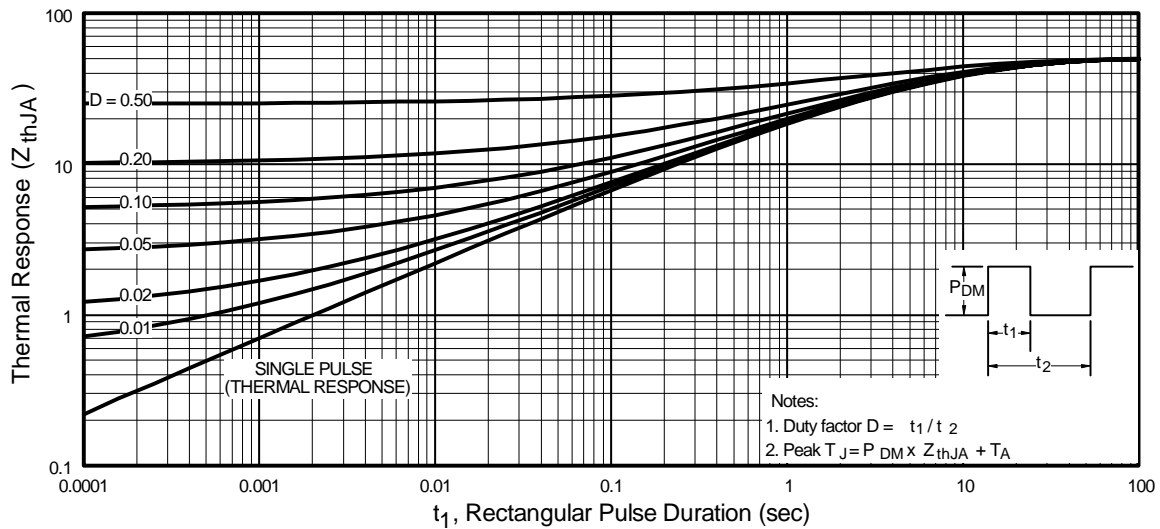
**Fig 9.** Maximum Drain Current Vs. Ambient Temperature



**Fig 10a.** Switching Time Test Circuit

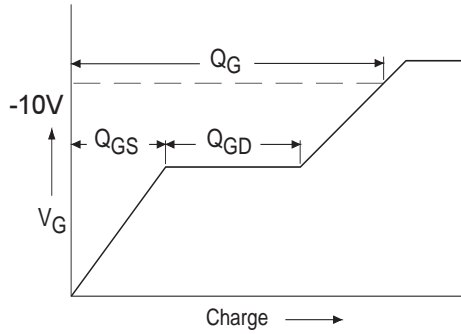


**Fig 10b.** Switching Time Waveforms

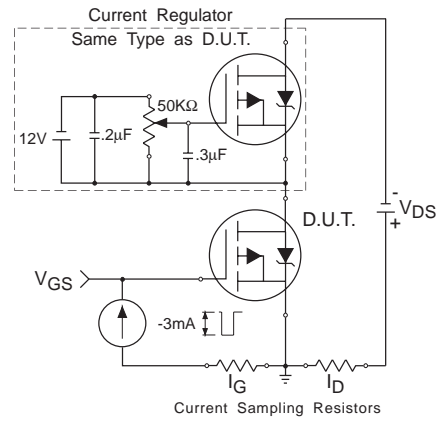


# IRF7406

International  
**IR** Rectifier

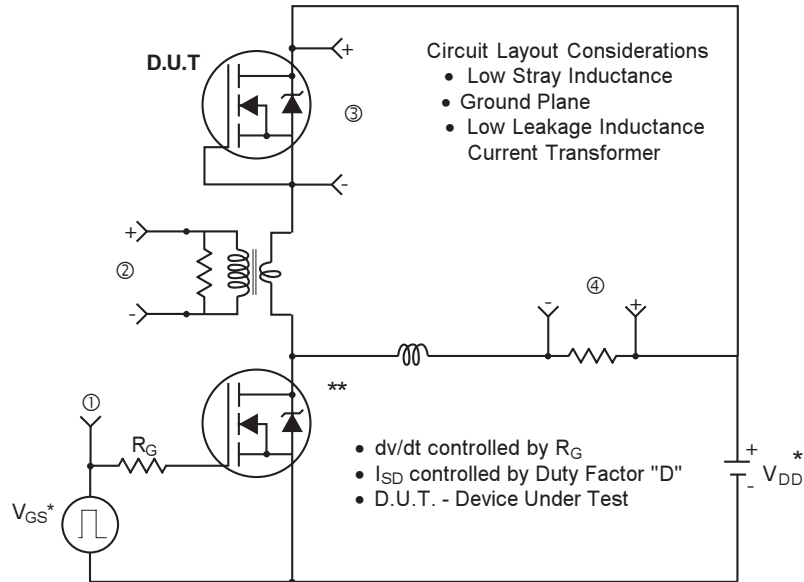


**Fig 12a.** Basic Gate Charge Waveform



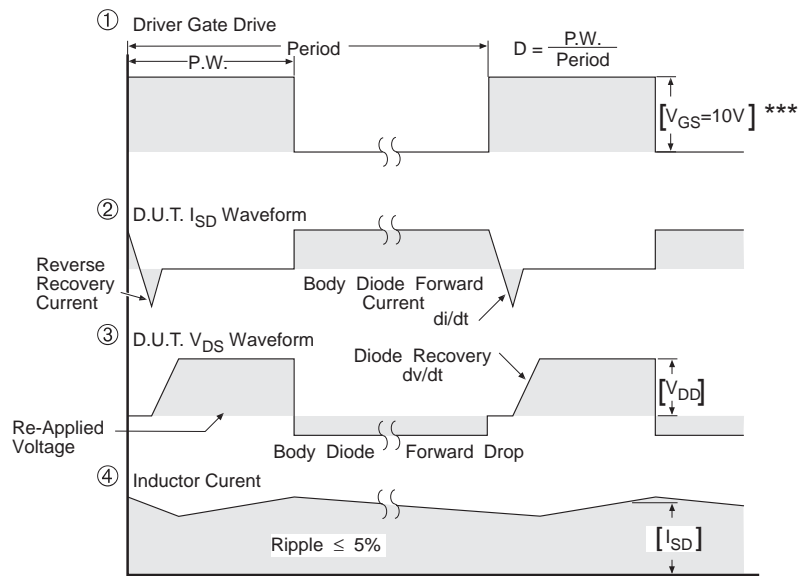
**Fig 12b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and  $3V$  Drive Devices

**Fig 13. For P-Channel HEXFETS**

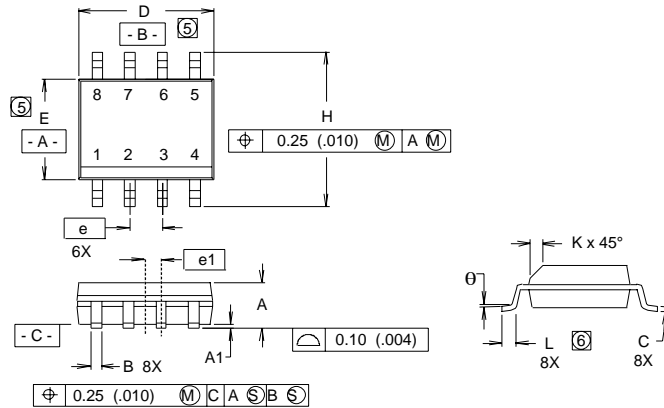
# IRF7406

International  
**IR** Rectifier

## Package Outline

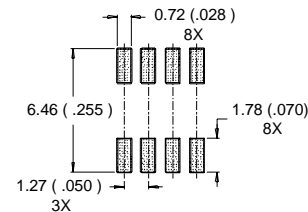
### SO-8 Outline

Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
$\theta$	0°	8°	0°	8°

#### RECOMMENDED FOOTPRINT



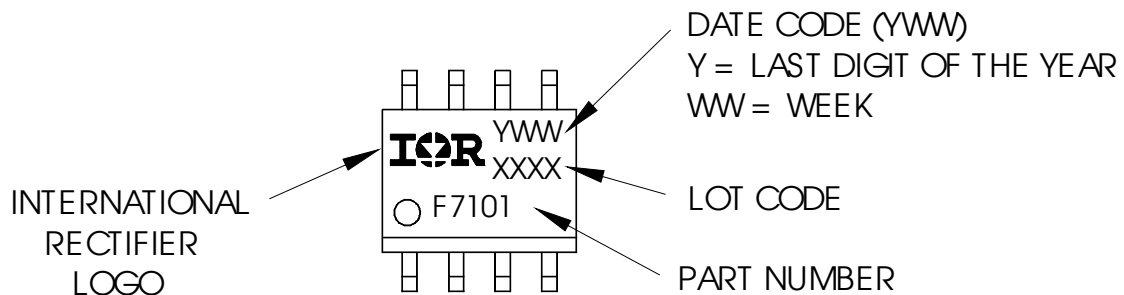
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS  
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- ⑥ DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

## Part Marking Information

### SO-8

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

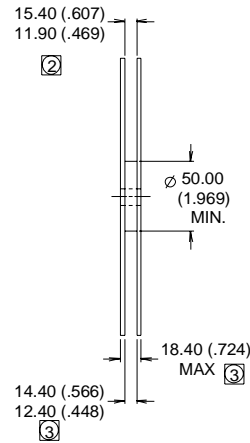
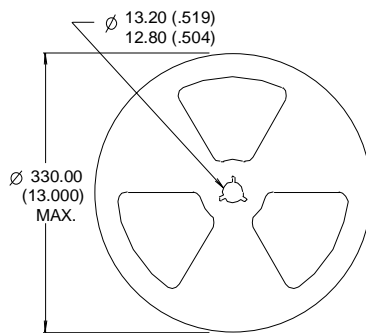
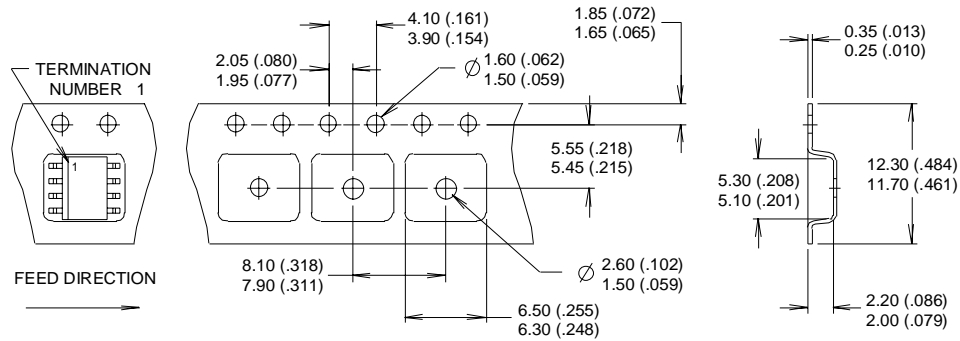




Tape & Reel Information

SO-8

Dimensions are shown in millimeters (inches)



- NOTES:
- 1 CONFORMS TO EIA-481-1
  - 2 INCLUDES FLANGE DISTORTION @ OUTER EDGE
  - 3 DIMENSIONS MEASURED @ HUB
  - 4 CONTROLLING DIMENSION : METRIC

Data and specifications subject to change without notice.