The documentation and process conversion measures necessary to comply with this revision shall be completed by 10 June 2019.

INCH-POUND

MIL-PRF-19500/746C
w/AMENDMENT 3
8 March 2019
SUPERSEDING
MIL-PRF-19500/746C
w/AMENDMENT 2
19 April 2018

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED, N-CHANNEL, SILICON, SURFACE MOUNT, TYPES 2N7587, 2N7589, 2N7591, AND 2N7593, QUALITY LEVELS JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device. Two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device.

1.2 Package outlines. The device package outline is a TO-276AA in accordance with figure 1 for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are in accordance with figure 2.

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type (1)	P_T (2) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (3)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (4) (5) T_C =+25°C	I_{D2} T_C = +100°C	I_S	I_{DM} (6)	T_J and T_{STG}	V_{ISO} 70,000 ft. altitude
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C	V dc
2N7587	75	1.56	1.67	100	100	±20	22	19	22	88	-55 to +150	250
2N7589	75	1.56	1.67	150	150	±20	19	12	19	76		
2N7591	75	1.56	1.67	200	200	±20	16	10	16	64		
2N7593	75	1.56	1.67	250	250	±20	12.4	7.8	12.4	49.6		

(1) Also applies to U3 and U3C suffix versions.
(2) Derate linearly by 0.6 W/°C for T_C > +25°C.
(3) See figure 3, thermal impedance curves.
(4) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(5) See figure 4, maximum drain current graph.
* (6) I_{DM} = 4 X I_{D1}; I_{D1} as calculated by footnote (4).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A

FSC 5961

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80% of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = 12V, I_D = I_{D2}		E_{AS}
					T_J = +25°C	T_J = +150°C	
	V dc	V dc		µA dc	Ω	Ω	mJ
		Min	Max				
2N7587, 2N7587U3, 2N7587U3C	100	2.0	4.0	10	0.042	0.084	73
2N7589, 2N7589U3, 2N7589U3C	150	2.0	4.0	10	0.088	0.207	60
2N7591, 2N7591U3, 2N7591U3C	200	2.0	4.0	10	0.130	0.300	60
2N7593, 2N7593U3, 2N7593U3C	250	2.0	4.0	10	0.210	0.494	56

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.6 for PIN construction example and 6.7 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The only quality level designators for encapsulated devices that are applicable for this specification sheet are the quality levels "JANTXV" and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: “R” and “F”.

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

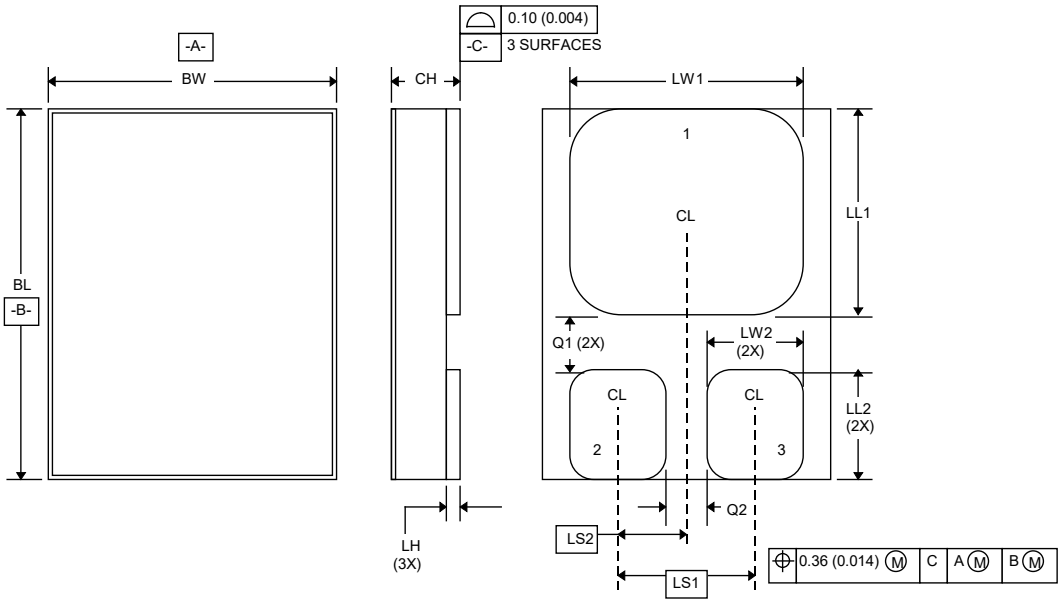
1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7587", "7589", "7591", and "7593".

1.5.4 Suffix letters. The following suffix letters are incorporated in the PIN for this specification sheet:

U3	Indicates a metal lidded 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 1).
U3C	Indicates a ceramic lidded 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 1).
	Indicates a JANHC or JANKC die, see figure 2.

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

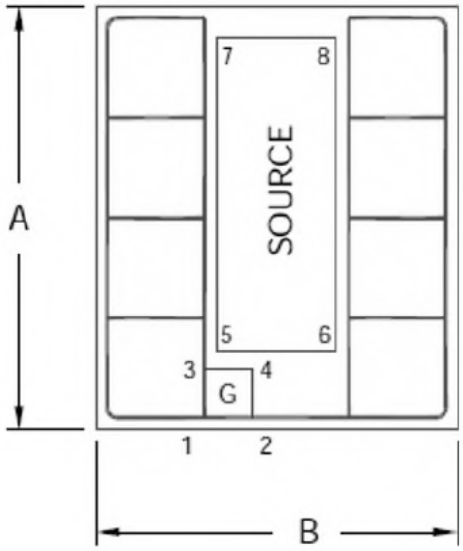
1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifier that is applicable for this specification sheet is "A" (see figure 2 and 6.5).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH (for U3)		.124		3.15
CH (for U3C)		.1335		3.39
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimension are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate, and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
5. Metal lid: U3 suffix; Ceramic lid: U3C suffix.

FIGURE 1. Dimensions and configuration (TO-276AA, SMD-0.5), with metal lid or ceramic lid.



Key	Dimensions				
	Micrometers		Mils		Tolerance
	Min	Max	Min	Max	
1	0	0	0	0	±5 µm
2	541	0	21.299	0	±5 µm
3	0	538.3	0	21.193	±5 µm
4	541	538.3	21.299	21.193	±5 µm
5	77	906.8	3.031	35.70	±5 µm
6	1170	906.8	46.06	35.70	±5 µm
7	77	3994.5	3.031	157.26	±5 µm
8	1170	3994.5	46.06	157.26	±5 µm
A	4611		181.5		±200 µm
B	2946		116		±200 µm

NOTES:
1. Dimensions are in mils. Micrometers are given for general information only.
2. Key 2 through 8 are relative to Key 1.
3. Top metal: Aluminum, 5.6 µm (0.22 mils) thick.
4. Back metal: Aluminum, Titanium, nickel, silver, 0.1, 0.1, 0.4, 0.6 µm thick, respectively.
5. All dimensions are valid for all radiation hardness levels specified.
6. Backside metal is the drain connection.
7. Die thickness: 187.9 µm (7.4 mils).
8. For sawn die, outline dimensions (A and B) will be reduced by 25 µm (0.98 mils), due to saw kerf.
9. Die bond pad coordinates are provided for use in automated bonding equipment. Key locations 1 through 8 refer to adjacent gate (G) /source (S) pad corners.
10. See 6.6.2 and 6.5 for ordering information.

FIGURE 2. JANHC and JANKC (A-version) die dimensions.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
* MIL-STD-883 - Test Method Standard for Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and herein. The device package style is either a metal lidded or ceramic lidded TO-276AA in accordance with figure 1 for all encapsulated devices. See figure 2 for unencapsulated JANHC/JANKC die.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Multiple chip construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.4.3 Pin-out. The pin-out of the device shall be as shown on figure 1.

* 3.4.4 Silicone Die coating. The use of a silicone die coat requires a successful completion of MIL-STD-883, method 5011 on each epoxy lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, R $\leq$ or 100 kΩ, whenever bias voltage is applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figures herein. Electrical measurements (end-points) shall be in accordance with table IV herein.

4.3 Screening of encapsulated devices. Screening of packaged devices shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.
17	For TO-276AA packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.	For TO-276AA packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 24 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Inductance: ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200\ \Omega$.

d. Supply voltage (V_{DD})..... V_{DD} = 25 V dc, except V_{DD} = 50 V dc (2N7593), up to rated V_{DS}.

e. Peak gate voltage (V_{GS}) ..... 12 V, up to maximum rated V_{GS}.

f. Initial case temperature ..... T_C = +25°C +10°C, -5°C.

g. Number of pulses to be applied..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 30 - 60 μs max. See table III, group E, subgroup 4 herein.

4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.3.5 Dielectric withstanding voltage.

a. Magnitude of test voltage……600V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……All leads to case (bunch connection).

d. Method of connection……Mechanical

e. Kilovolt-ampere rating of high voltage source……..1,200 V.1,0 mA (min).

f. Maximum leakage current……...1.0 mA.

g. Voltage ramp up time……500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows.

4.4.2.1 Quality level JANS (table E-VIA of MIL-PRF-19500).

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM).
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	Intermittent operation life, condition D, t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Test condition D.

4.4.2.2 Quality level JANTXV (table E-VIB of MIL-PRF-19500).

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, t_{on} = 30 seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	2036	Terminal strength is not applicable.
C3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	See 4.3.3, $R_{\theta JC}$ = 1.67 °C/W.
C6	1042	Intermittent operation life, condition D, t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.4.5.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the safe operation area graph herein. Electrical measurements (end-points) shall be in accordance with table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/, 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 3/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	Bias condition C, V_{GS} = 0 V, I_D = 1 mA dc	$V_{(BR)DSS}$			
2N7587				100		V dc
2N7589				150		V dc
2N7591				200		V dc
2N7593				250		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0 V	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0 V	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS},	I_{DSS1}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)1}$			
2N7587					0.042	Ω
2N7589					0.088	Ω
2N7591					0.130	Ω
2N7593					0.210	Ω
Forward voltage	4011	V_{GS} = 0 V dc, condition A, I_D = I_{D1}	V_{SD}		1.2	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/, 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7587					0.080	Ω
2N7589					0.176	Ω
2N7591					0.273	Ω
2N7593					0.441	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	$I_D = I_{D2}$, V_{DD} = 15 V dc (see 4.5.1)	g_{FS}			
2N7587				14		S
2N7589				13		S
2N7591				10		S
2N7593				8.8		S
Switching time test	3472	I_D = rated I_{D1}, V_{GS}= 12 V dc, $R_G = 7.5\ \Omega$, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$		25	ns
Rise-time			t_r		30	ns
Turn-off delay time			$t_{d(off)}$		60	ns
Fall time			t_f		30	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/, 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 5						
Safe operating area test	3474	See figure 5 ~~4~~; tp = 10 ms min. VDS = 80 percent of max. rated VDS				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B, $I_D = I_{D1}$, V_{GS} = 12 V dc V_{DD} = 50 percent of rated V_{DS}				
On-state gate charge and turn-off gate charge			$Q_{G(ON)}$ $Q_{G(OFF)}$		50 50	nC
Gate to source charge (turn-on and turn-off)			Q_{GS1} Q_{GS2}		15 15	nC
Gate to drain charge (turn-on and turn-off)			Q_{GD1} Q_{GD2}		20 20	nC
Reverse recovery time	3473	Condition A, di/dt = -100 A/µs, $V_{DD} \leq 50$ V, $I_D = I_{D1}$	t_{rr}		350	ns

1/ Also applies to U3 and U3C suffix versions.
2/ For sampling plan, see MIL-PRF-19500.
3/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
				R and F		R and F		
	Method	Conditions		Min	Max	Min	Max	
Subgroup 1								
Not applicable								
Subgroup 2		T_C = + 25°C						
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{GS} = 12 V; V_{DS} = 0						
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS}(pre-irradiation)						
End-point electricals:								
Breakdown voltage, drain to source	3407	Bias condition C, V_{GS} = 0; I_D = 1 mA	$V_{(BR)DSS}$					
2N7587				100		100		V dc
2N7589				150		150		V dc
2N7591				200		200		V dc
2N7593				250		250		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = 1 mA	$V_{GS(th)1}$	2.0	4.0	2.0	4.0	V dc
Gate current	3411	Bias condition C, V_{GS} = +20 V; V_{DS} = 0	I_{GSSF1}		100		100	nA dc
Gate current	3411	Bias condition C, V_{GS} = -20 V; V_{DS} = 0	I_{GSSR1}		-100		-100	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS}		10		10	µA dc
Static drain to source on-state voltage	3405	V_{GS} = 12 V; I_D = I_{D2} condition A, pulsed (see 4.5.1)	$V_{DS(on)}$					
2N7587					0.855		0.855	V dc
2N7589					1.104		1.104	V dc
2N7591					1.340		1.340	V dc
2N7593					1.638		1.638	V dc
Forward voltage source drain diode	4011	Bias condition A, V_{GS} = 0; I_D = I_{D1}	V_{SD}		1.2		1.2	V dc

1/ For sampling plan, see MIL-PRF-19500. Characteristics also apply to U3 and U3C suffix versions.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	-55°C to +150°C, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I, subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			3 devices c = 0
Barometric pressure 2N7593, 2N7593U3, and 2N7593U3C only	1001	To 70,000 feet	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level linear energy transfer (LET) is sufficient to qualify all lower level LETs.

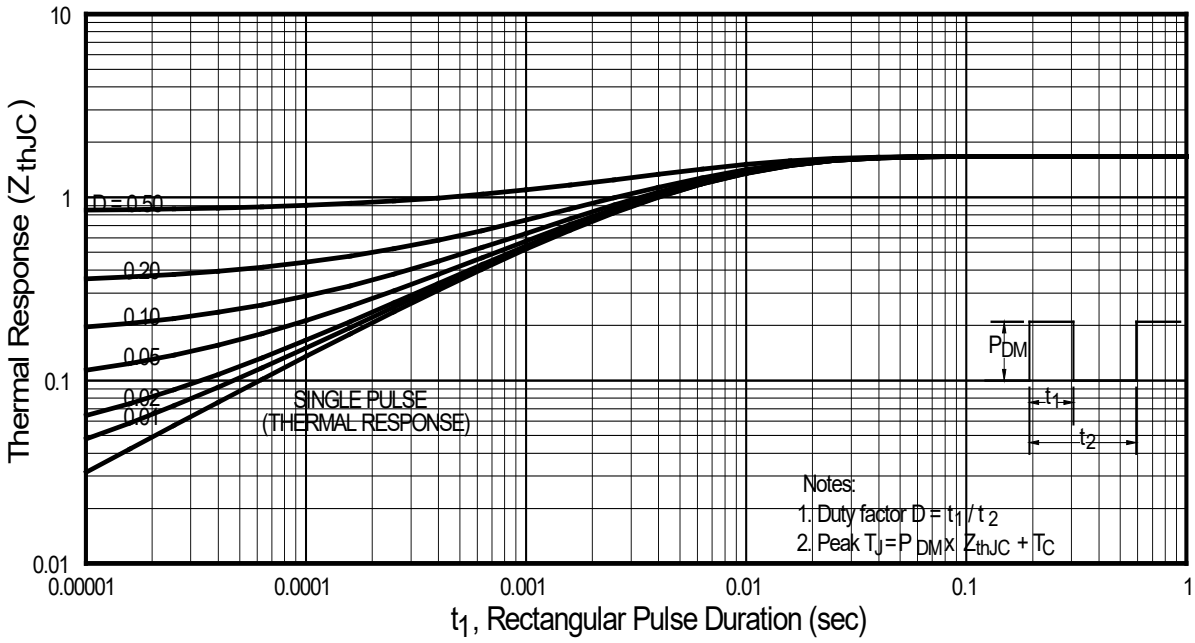
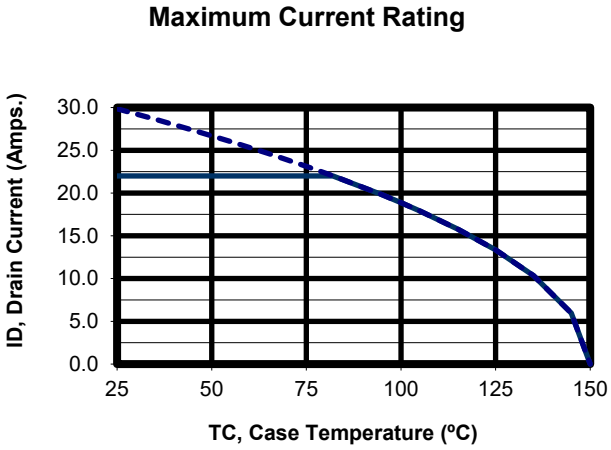
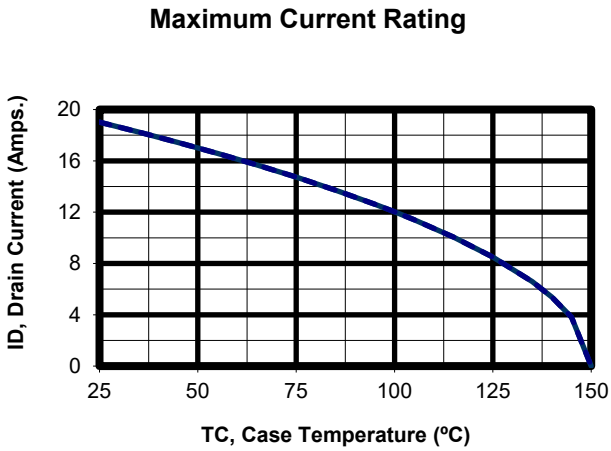


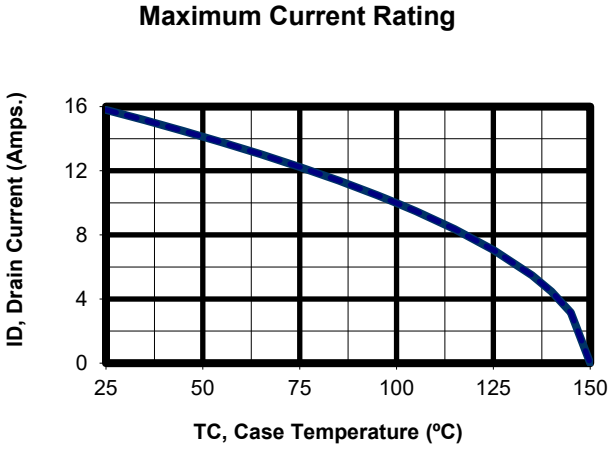
FIGURE 3. Thermal response curve.



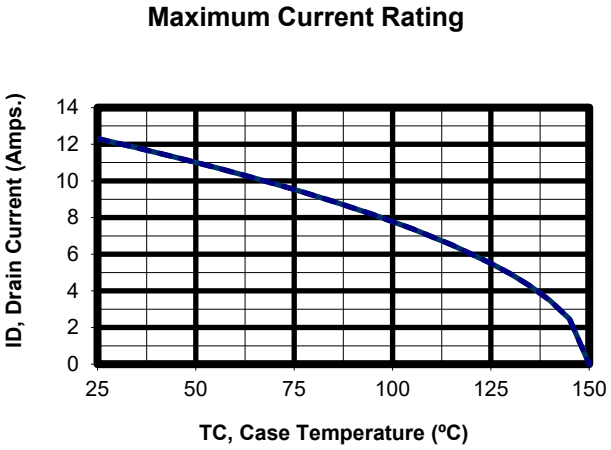
2N7587, 2N7587U3, 2N7587U3C



2N7589, 2N7589U3, 2N7589U3C



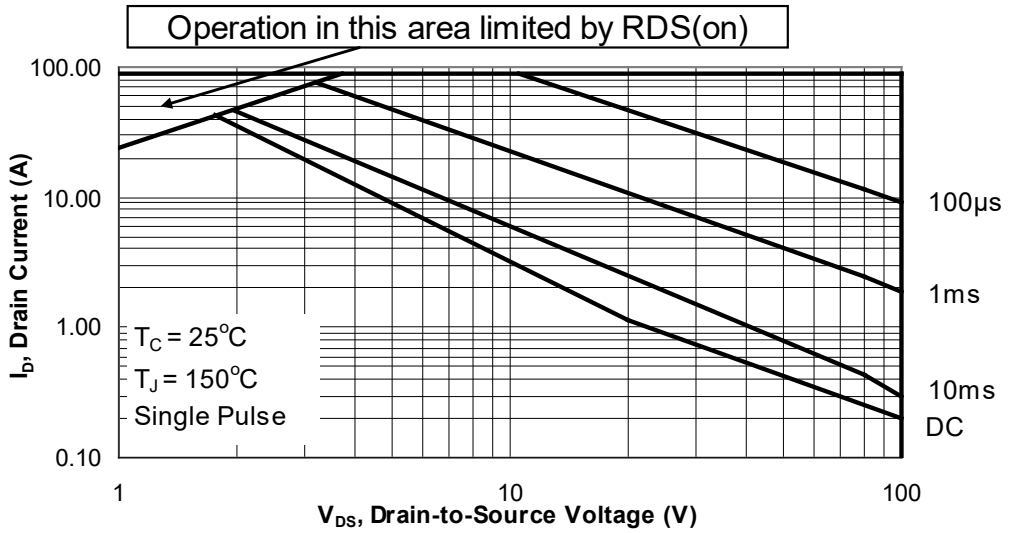
2N7591, 2N7591U3, 2N7591U3C



2N7593, 2N7593U3, 2N7593U3C

FIGURE 4. Maximum drain current versus case temperature graphs.

2N7587, 2N7587U3, 2N7587U3C



2N7589, 2N7589U3, 2N7589U3C

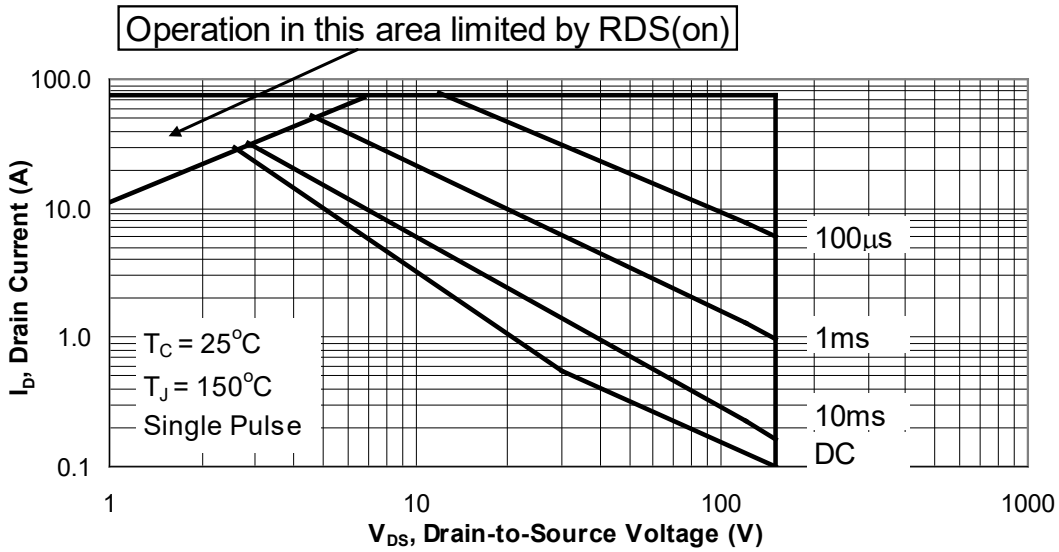
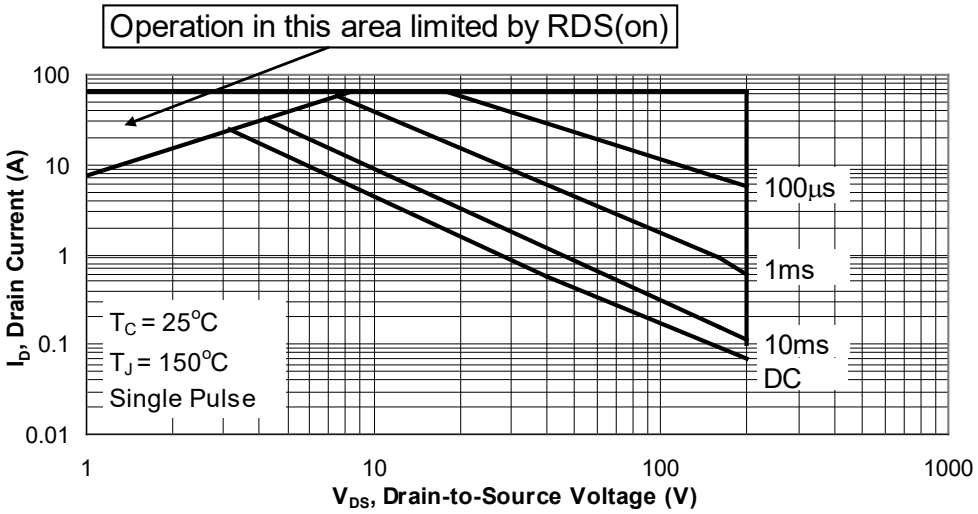


FIGURE 5. Safe operating area graph.

2N7591, 2N7591U3, 2N7591U3C



2N7593 2N7593U3, 2N7593U3C

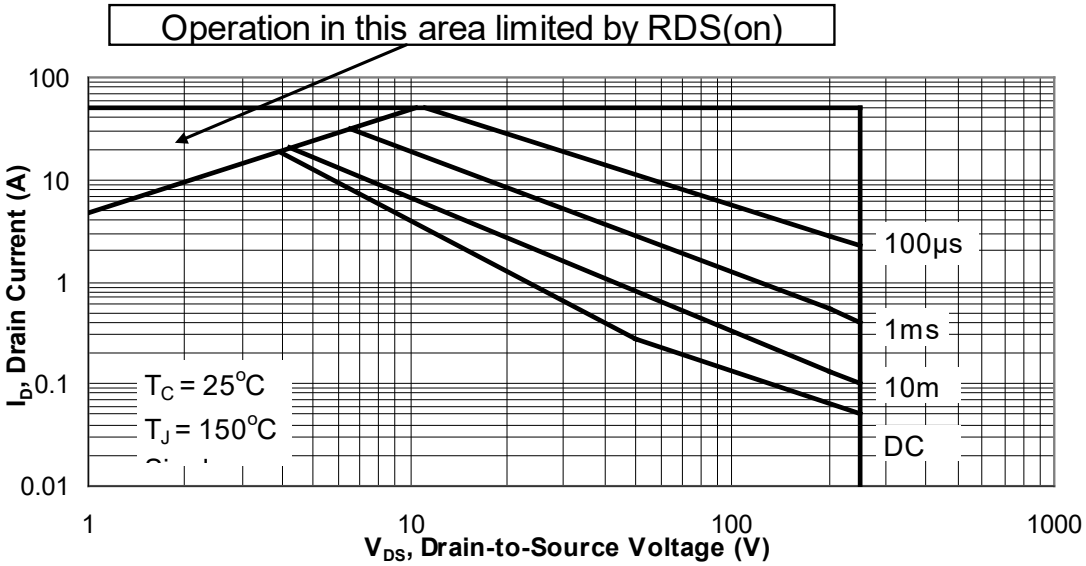


FIGURE 5. Safe operating area graph - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.6.

e. For die acquisition, the JANHC or JANKC letter version shall be specified (see figure 2).

f. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.

g. If specific SEE characterization conditions are desired (see section 6.6 and table IV), manufacturer's cage code should be specified in the contract or order.

h. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN) (without JAN and RHA prefix). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Preferred types military PIN	Commercial PIN
2N7587U3 2N7589U3 2N7591U3 2N7593U3	IRHNJ67130 IRHNJ67134 IRHNJ67230 IRHNJ67234
2N7587U3C 2N7589U3C 2N7591U3C 2N7593U3C	IRHNJC67130 IRHNJC67134 IRHNJC67230 IRHNJC67234

6.5 Application data.

6.5.1 Manufacturer specific irradiation data. Each manufacturer qualified to this specification sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25 ±5°C	
	2N7587, 2N7587U3, 2N7587U3C		Surface LET = 39 MeV-cm2/mg ±5%, range = 40 µm ±7.5%, energy = 315 MeV ±5% In-situ bias conditions: V_{DS} = 100 V and V_{GS} = -19 V; V_{DS} = 40 V and V_{GS} = -20 V (Typical 3.80 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7589, 2N7589U3, 2N7589U3C			
	2N7591, 2N7591U3, 2N7591U3C		Surface LET = 39 MeV-cm2/mg ±5%, range = 50 µm ±5%, energy = 410 MeV ±5% In-situ bias conditions: V_{DS} = 150 V and V_{GS} = -20 V (Typical 4.90 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7593, 2N7593U3, 2N7593U3C		Surface LET = 42 MeV-cm2/mg ±5%, range = 205 µm ±5%, energy = 2450 MeV ±5% In-situ bias conditions: V_{DS} = 200 V and V_{GS} = -10 V; V_{DS} = 190 V and V_{GS} = -15 V (Typical 8.49 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7587, 2N7587U3, 2N7587U3C		Surface LET = 44 MeV-cm2/mg ±5%, range = 125 µm ±10%, energy = 1350 MeV ±5% In-situ bias conditions: V_{DS} = 250 V and V_{GS} = -15 V, V_{DS} = 40 V and V_{GS} = -20 V (Typical 10.05 MeV/Nucleon at Texas A & M Cyclotron)	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	

TABLE IV. Manufacturers characterization conditions - continued.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25 ±5°C	
	2N7587, 2N7587U3, 2N7587U3C		Surface LET = 61 MeV-cm2/mg ±5%, range = 32 µm ±7.5%, energy = 345 MeV ±5% In-situ bias conditions: V_{DS} = 100 V and V_{GS} = -10 V; V_{DS} = 30 V and V_{GS} = -15 V (Typical 2.70 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7589, 2N7589U3, 2N7589U3C		Surface LET = 61 MeV-cm2/mg ±5%, range = 66 µm ±7.5%, energy = 825 MeV ±5% In-situ bias conditions: V_{DS} = 150 V and V_{GS} = -10 V V_{DS} = 40- V and V_{GS} = -15 V (Typical 6.40 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7591, 2N7591U3, 2N7591U3C		Surface LET = 61 MeV-cm2/mg ±5%, range = 66 µm ±7.5%, energy = 825 MeV ±5% In-situ bias conditions: V_{DS} = 200 V and V_{GS} = -15 V, V_{DS} = 190 V and V_{GS} = -20 V (Typical 6.41 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7593, 2N7593U3, 2N7593U3C		Surface LET = 61 MeV-cm2/mg ±5%, range = 66 µm ±7.5%, energy = 825 MeV ±5% In-situ bias conditions: V_{DS} = 250 V and V_{GS} = -10 V, V_{DS} = 50 V and V_{GS} = -15 V (Typical 6.41 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7587, 2N7587U3, 2N7587U3C		Surface LET = 90 MeV-cm2/mg ±5%, range = 29 µm ±7.5%, energy = 375 MeV ±7.5% In-situ bias conditions: V_{DS} = 100 V and V_{GS} = -5 V, (Typical 1.88 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7589, 2N7589U3, 2N7589U3C		Surface LET = 90 MeV-cm2/mg ±5%, range = 80 µm ±5%, energy = 1470 MeV ±5% In-situ bias conditions: V_{DS} = 50 V and V_{GS} = -5 V, V_{DS} = 30 V and V_{GS} = -10 V (Typical 7.47 MeV/Nucleon at Texas A & M Cyclotron)	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	

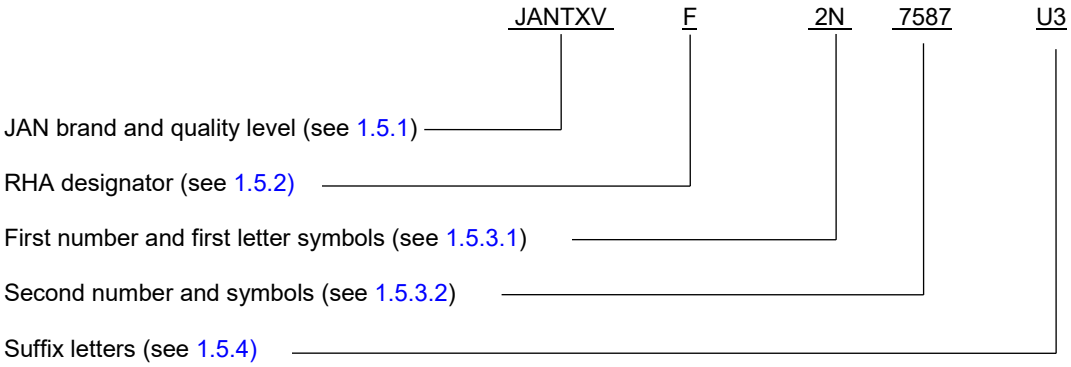
TABLE IV. Manufacturers characterization conditions - continued.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
	2N7591, 2N7591U3, 2N7591U3C		Surface LET = 90 MeV-cm2/mg ±5%, range = 80 µm ±5%, energy = 1470MeV ±5% In-situ bias conditions: V_{DS} = 170 V and V_{GS} = -5 V; (Typical 7.47 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7593, 2N7593U3, 2N7593U3C		Surface LET = 90 MeV-cm2/mg ±5%, range = 80 µm ±5%, energy = 1470 MeV ±5% In-situ bias conditions: V_{DS} = 75 V and V_{GS} = -5 V (Typical 6.40 MeV/Nucleon at Texas A & M Cyclotron)	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.				

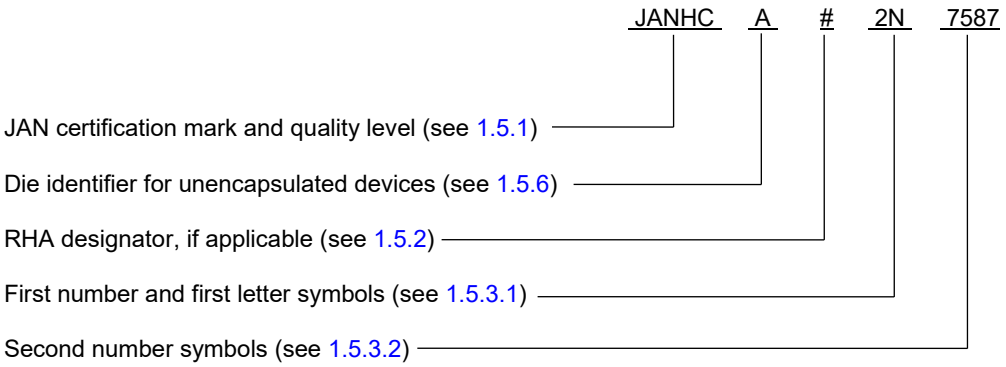
1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias conditions. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

6.6 PIN construction example.

6.6.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.6.2 Unencapsulated devices. The PINs for unencapsulated devices are constructed using the following form.



6.7 List of PINs.

* 6.7.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

JANTXVF2N7587U3	JANTXVF2N7589U3	JANTXVF2N7591U3	JANTXVF2N7593U3
JANTXVR2N7587U3	JANTXVR2N7589U3	JANTXVR2N7591U3	JANTXVR2N7593U3
JANTXVF2N7587U3C	JANTXVF2N7589U3C	JANTXVF2N7591U3C	JANTXVF2N7593U3C
JANTXVR2N7587U3C	JANTXVR2N7589U3C	JANTXVR2N7591U3C	JANTXVR2N7593U3C
JANSF2N7587U3	JANSF2N7589U3	JANSF2N7591U3	JANSF2N7593U3
JANSR2N7587U3	JANSR2N7589U3	JANSR2N7591U3	JANSR2N7593U3
JANSF2N7587U3C	JANSF2N7589U3C	JANSF2N7591U3C	JANSF2N7593U3C
JANSR2N7587U3C	JANSR2N7589U3C	JANSR2N7591U3C	JANSR2N7593U3C

6.7.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified die suppliers with the applicable letter version (e.g., JANHCAR2N7587) will be identified on the QML.

Die ordering information	
PIN	Manufacturer 1/
	69210
2N7587	JANHCA#2N7587 JANKCA#2N7587
2N7589	JANHCA#2N7589 JANKCA#2N7589
2N7591	JANHCA#2N7591 JANKCA#2N7591
2N7593	JANHCA#2N7593 JANKCA#2N7593

1/ The number sign (#) represent one of eight RHA designators available (R or F). The PIN is also available without a RHA designator.

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

6.9 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activity:
Army - MI
* Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2019-024)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.