The documentation and process conversion measures necessary to comply with this revision shall be completed by 25 September 2010.

INCH-POUND

MIL-PRF-19500/683D
25 June 2010
SUPERSEDING
MIL-PRF-19500/683C
5 November 2009

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, FIELD EFFECT, N-CHANNEL,
RADIATION HARDENED (TOTAL DOSE AND SINGLE EVENT EFFECTS)
TYPE 2N7467U2, JANTXVR, F, G, AND H AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode power MOSFET transistor with radiation hardened total dose and single event (SEE) effects ratings, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500. See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See figure 1, surface mount, TO-276AC, (SMD-2).

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C (free air)	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} T_C = +25°C (3) (4)	I_{D2} T_C = +100°C (3) (4)	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7467U2	250	2.5	0.50	30	30	±20	75	75	75	300	-55 to +150

(1) Derate linearly 2.0 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and device construction to 75 Amps:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.daps.dla.mil/.

AMSC N/A FSC 5961

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc		E_{AS} at I_{D1}	I_{AS}
					T_J = 25°C at I_{D2}	T_J = 150°C at I_{D2}		
	V dc	V dc		µA dc	ohm	ohm	mJ	A
		Min	Max					
2N7467U2	30	2.0	4.0	10	.0035	.006	500	75

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

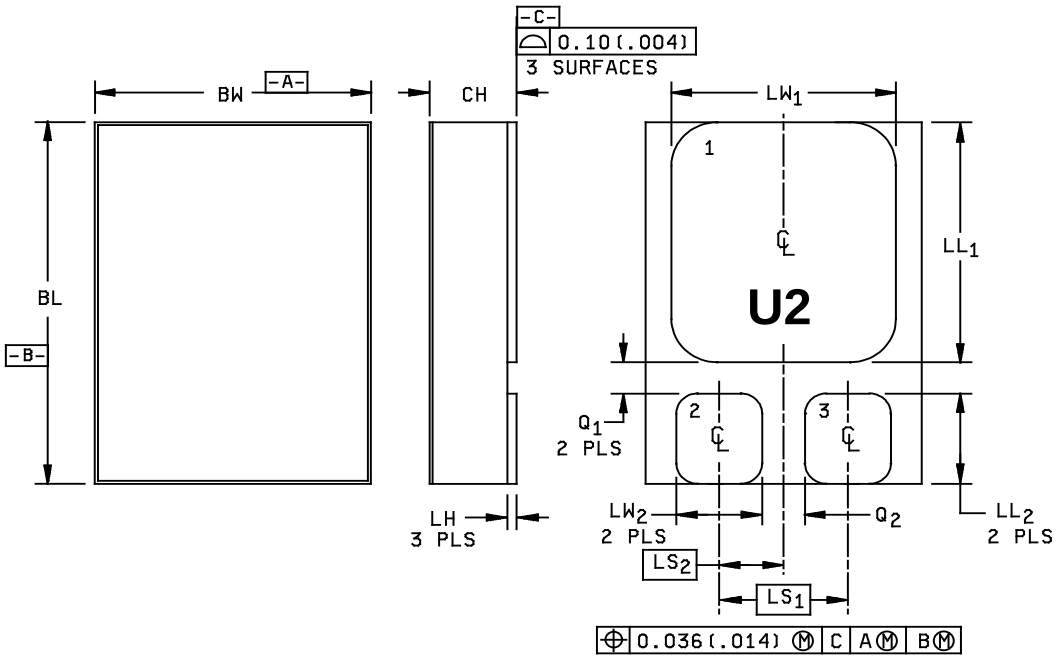
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or https://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



LTR	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
* CH		.142		3.61
LL1	.470	.480	11.94	12.19
LL2	.152	.162	3.86	4.11
LH	.010	.020	.254	.508
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
LW1	.435	.445	11.05	11.30
LW2	.135	.145	3.43	3.68
Q1	.035		.89	
Q2	.050		1.27	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimensions and tolerancing shall be in accordance with ASME Y14.5M.
4. Terminal 1 – Drain, Terminal 2 – Gate, Terminal 3 – Source

* FIGURE 1. Physical dimensions for surface mount - 2N7467U2 (TO-276AC).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS}.....Rated avalanche current, nonrepetitive
nC .....nano Coulomb.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and figure 1 (U2, TO-276AC) herein. Methods used for the electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Lead material and finish. Terminal material shall be copper tungsten. Terminal finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of terminal finish is desired, it shall be specified in the acquisition document (see 6.5).

3.4.2 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.6).

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area graph shown herein. End-point measurements shall be in accordance with table III.

4.3 Screening (JANS, JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
9	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$ ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{DSS1} = ±5 μA dc or ±100 percent of initial value, whichever is greater	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{DSS1} = ±5 μA dc or ±100 percent of initial value, whichever is greater $\Delta r_{DS(on)1}$ =±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value	Subgroup 2 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{DSS1} = ±5 μA dc or ±100 percent of initial value, whichever is greater $\Delta r_{DS(on)1}$ = ±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 24 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_{AS}) ..... $I_{AS(max)}$.

b. Peak gate voltage (V_{GS}) ..... 12 V minimum up to rated V_{GS} maximum.

c. Gate to source resistor (R_{GS}) ..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance (L)..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 25 V minimum up to rated V_{GS} maximum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, appendix E, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2075	See 3.4.2.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B4	1042	Test condition D, 2,000 cycles. Neither heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
B5	1042	Test condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours.
B5	1042	Test condition A, V_{DS} = rated; T_A = +175°C; t = 120 hours.
B5	2037	Bond strength; test condition D.

4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening).
B3	1042	Test condition D, 2,000 cycles. Neither heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
B4	2075	See 3.4.2.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein.

	Subgroup	Method	Condition
	C2	1021	Omit initial conditioning.
*	C2	2036	Not applicable.
	C5	3161	See 4.3.3.
	C6	1042	Test condition D, 6,000 cycles. Neither heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with appendix E, table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See MIL-PRF-19500, table E-IX, group E, subgroup 4.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0 V dc, I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$	30		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 24 V dc	I_{DSS1}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$		.0035	Ω
Forward voltage	4011	Pulsed (see 4.5.1), $I_D = I_{D1}$, V_{GS} = 0 V dc	V_{SD}		1.3	V
Subgroup 3						
High-temperature operation:		$T_C = T_J$ = +125°C				
Gate current	3411	V_{GS} = +20 V dc and -20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 24 V dc	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$		.0055	Ω
Gate to source voltage (thresholds)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low-temperature operation:		$T_C = T_J$ = -55°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Forward transconductance	3475	I_D = 45 A, V_{DD} = 15 V (see 4.5.1)	g_{FS}	45		
Switching time test	3472	I_D = 45 A, V_{GS}= 12 V dc, R_G = 2.35Ω, V_{DD} = 15 V dc				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r		125	ns
Turn-off delay time			$t_{d(off)}$		80	ns
Fall time			t_f		50	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 4; t_p = 10 ms V_{DS} = 24 V				
Electrical measurements		See table I, subgroup 2 herein.				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B, I_D = 45 A				
On-state gate charge			$Q_{G(on)}$		200	nC
Gate to source charge			Q_{GS}		55	nC
Gate to drain charge			Q_{GD}		40	nC
Reverse recovery time	3473	$d_i/ d_t \leq$ 100 A/µs, $V_{DD} \leq$ 25 V, I_D = 45 A	t_{rr}		165	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
	Method	Conditions		R, F, G and H		R, F and G		H 4/		
				Min	Max	Min	Max	Min	Max	
Subgroup 1										
Not applicable										
Subgroup 2		T_C = +25°C								
Steady-state total dose irradiation (V_{GS} bias) 5/	1019	V_{GS} = 12V V_{DS} = 0								
Steady-state total dose irradiation (V_{DS} bias) 5/	1019	V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	Bias condition C V_{GS} = 0 I_D = 1 mA	$V_{(BR)DSS}$	30		30		30		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	V_{GSth1}	2.0	4.0	2.0	4.0	1.5	4.0	V dc
Gate current	3411	Bias condition C V_{GS} = 20 V V_{DS} = 0	I_{GSSF1}		100		100		100	nA dc
Gate current	3411	Bias condition C V_{GS} = -20 V V_{DS} = 0	I_{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	Bias condition C V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		10		10		25	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
	Method	Conditions		R, F, G and H		R, F and G		H 4/		
				Min	Max	Min	Max	Min	Max	
Subgroup 2 -Continued										
Static drain to source on-state voltage 6/	3405	Condition A V_{GS} = 12 V pulsed (see 4.5.1) I_D= 45 A	V_{Dson1}		.180		.180		.2025	V dc
Static drain to source on-state voltage	3405	Condition A V_{GS} = 12 V pulsed (see 4.5.1) I_D= 45 A	V_{Dson1}		.1575		.1575		.180	V dc
Forward voltage source to drain diode	4011	V_{GS} = 0 I_D= 45 A	V_{SD}		1.3		1.3		1.3	V dc

1/ For sampling plan, see MIL-PRF-19500.
2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its' qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ The "H" designation represents devices which pass end-points at the G, R, and F designated Total-Ionizing-Dose (TID).
5/ Separate samples shall be pulled for each bias.
6/ Limit using TO-204AE package. The higher package resistance necessitates the higher V_{DSon1} limit when the manufacturer uses the alternate package as allowed in 4/ above.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			
Not applicable			
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 11			3 devices
SEE 2/ 3/ 4/	1080	See figure 5.	
Electrical measurements 5/		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
SEE irradiation		Fluence = 3E5 ±20 percent ions/cm^2, flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25 ± 5 °C. Surface LET = 38 MeV-cm2/mg ±5%, range = 38 µm ±7.5%, energy = 300 MeV ±7.5%. In situ bias conditions: V_{DS} = 30 V and V_{GS} = -10 V, V_{DS} = 22.5 V and V_{GS} = -15 V, V_{DS} = 15 V and V_{GS} = -20 V, (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator). Surface LET = 61 MeV-cm2/mg ±5%, range = 31 µm ±10%, energy = 330 MeV ±7.5%. In situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V, V_{DS} = 20 V and V_{GS} = -10 V, V_{DS} = 15 V and V_{GS} = -15 V, V_{DS} = 7.5 V and V_{GS} = -20 V, (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator). Surface LET = 84 MeV-cm2/mg ±5%, range = 28 µm ±7.5%, energy = 350 MeV ±7.5%. In situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V, V_{DS} = 20 V and V_{GS} = -10 V, (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator).	
Electrical measurements 5/		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.
4/ The sampling plan applies to each bias condition.
5/ Examine I_{GSSF1}, I_{GSSR1}, and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2 herein, may be performed at the manufacturer's option."

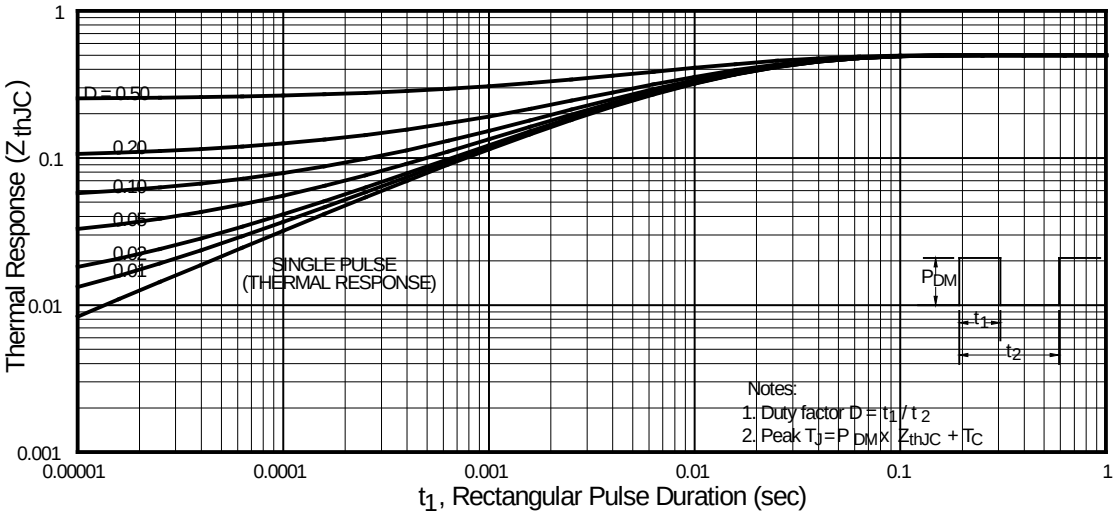


FIGURE 2. Thermal impedance curves.

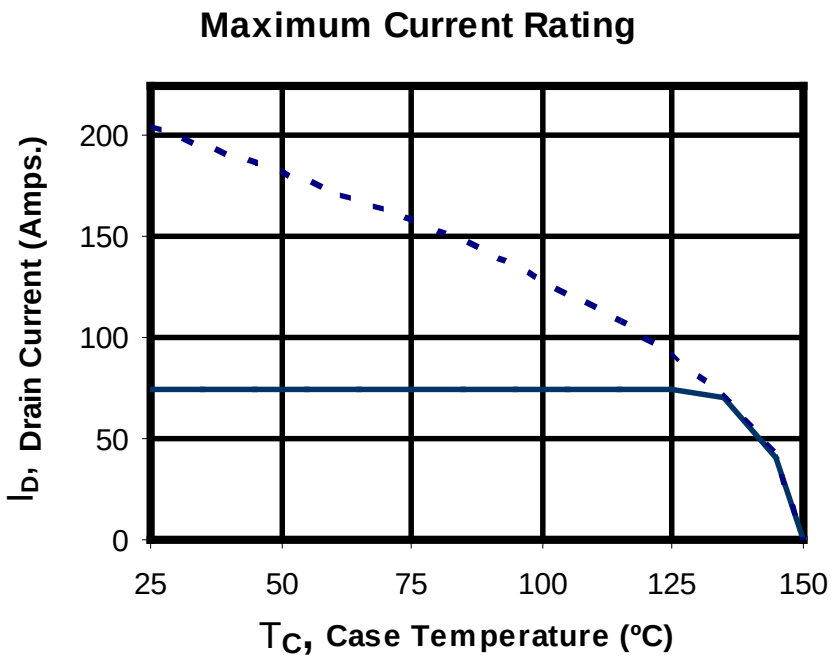


FIGURE 3. Maximum drain current versus case temperature graph.

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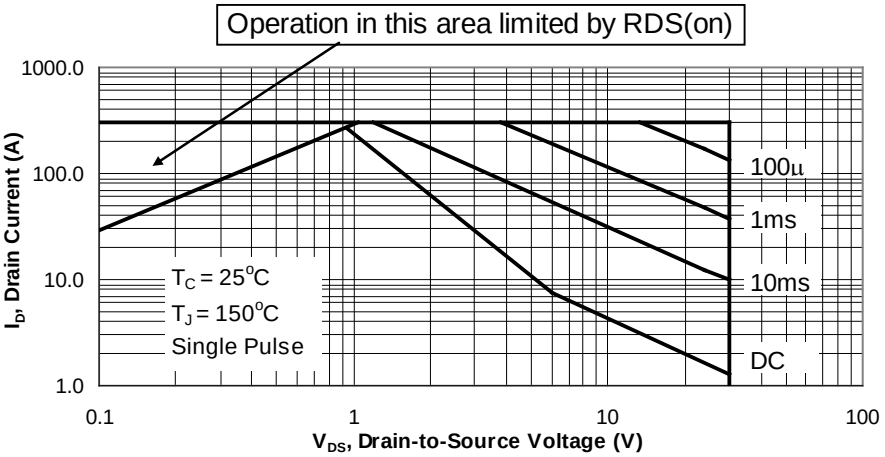
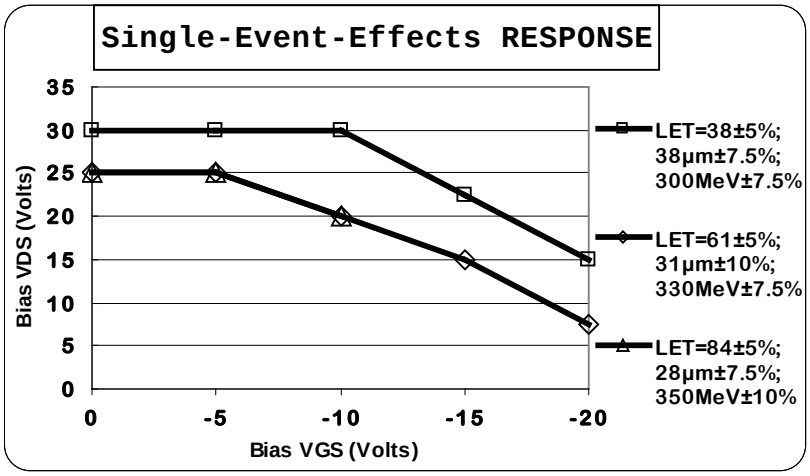


FIGURE 4. Safe operating area graph.



* FIGURE 5. Typical SEE safe operation area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.daps.dla.mil .

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types	Commercial types
2N7467U2	IRHNA57Z60

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2010-013)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.daps.dla.mil/ .