

DirectFET® P-Channel Power MOSFET ②

Typical values (unless otherwise specified)

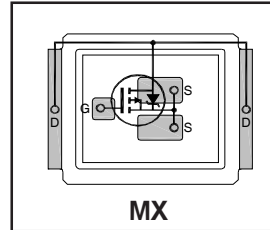
$V_{DS}$	$V_{GS}$	$R_{DS(on)}$	$R_{DS(on)}$		
-30V max	±20V max	2.3mΩ@-10V	3.8mΩ@-4.5V		
$Q_{g\ tot}$	$Q_{gd}$	$Q_{gs2}$	$Q_{rr}$	$Q_{oss}$	$V_{gs(th)}$
67nC	29nC	9.4nC	315nC	59nC	-1.8V

**Applications**

- Isolation Switch for Input Power or Battery Application
- High Side Switch for Inverter Applications

**Features and Benefits**

- Environmentally Friendly Product
- RoHS Compliant Containing no Lead, no Bromide and no Halogen
- Common-Drain P-Channel MOSFETs Provides High Level of Integration and Very Low RDS(on)



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST	MQ	<b>MX</b>	MT	MP	MC
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**Description**

The IRF9383MTRPbF combines the latest HEXFET® P-Channel Power MOSFET Silicon technology with the advanced DirectFET® packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.6 mm profile. The DirectFET® package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET® package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF9383MTRPbF	DirectFET® Medium Can	Tape and Reel	4800	
IRF9383MTR1PbF	DirectFET® Medium Can	Tape and Reel	4000	"TR1" suffix EOL notice #264

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	-30	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	-22	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	-17	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ④	-160	
$I_{DM}$	Pulsed Drain Current ⑤	-180	

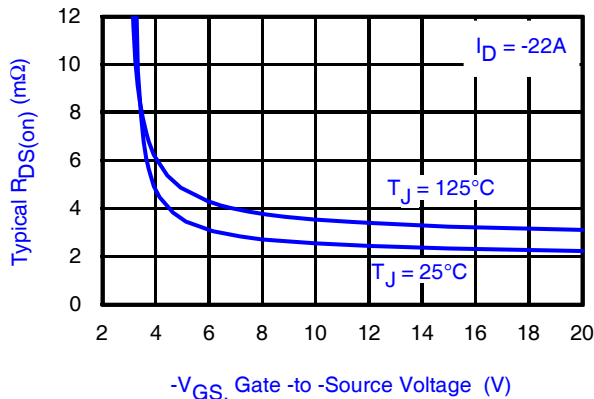


Fig 1. Typical On-Resistance vs. Gate Voltage

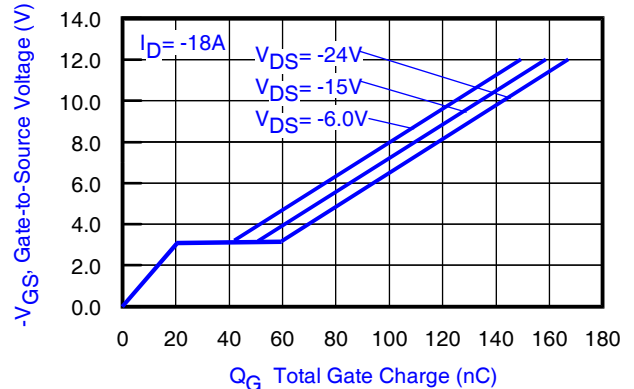


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

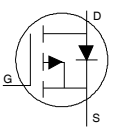
Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET® Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_C$  measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.0159	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.3	2.9	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -22A ⑥
		—	3.8	4.8		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -18A ⑥
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.3	-1.8	-2.4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -150μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-5.9	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-1.0	μA	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V
		—	—	-150		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V
g <sub>fs</sub>	Forward Transconductance	56	—	—	S	V <sub>DS</sub> = -10V, I <sub>D</sub> = -18A
Q <sub>g</sub>	Total Gate Charge	—	130	—	nC	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -18A  V <sub>DS</sub> = -15V V <sub>GS</sub> = -4.5V I <sub>D</sub> = -18A See Fig.15
Q <sub>g</sub>	Total Gate Charge	—	67	—		
Q <sub>gs1</sub>	Pre- V <sub>th</sub> Gate-to-Source Charge	—	12	—		
Q <sub>gs2</sub>	Post -V <sub>th</sub> Gate-to-Source Charge	—	9.4	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	29	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	16.6	—		
Q <sub>sw</sub>	Switch charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	38.4	—		
Q <sub>oss</sub>	Output Charge	—	59	—		
R <sub>G</sub>	Gate Resistance	—	6.5	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	29	—	ns	V <sub>DD</sub> = -15V, V <sub>GS</sub> = -4.5V ⑥ I <sub>D</sub> = -18A R <sub>G</sub> = 1.8Ω See Fig.17
t <sub>r</sub>	Rise Time	—	160	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	115	—		
t <sub>f</sub>	Fall Time	—	110	—		
C <sub>iss</sub>	Input Capacitance	—	7305	—	pF	V <sub>DS</sub> = -15V f = 1.0KHz
C <sub>oss</sub>	Output Capacitance	—	1780	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	1030	—		

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-114	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ⑤	—	—	-180		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -18A, V <sub>GS</sub> = 0V ⑥
t <sub>rr</sub>	Reverse Recovery Time	—	52	78	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -18A, V <sub>DD</sub> = -15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	315	470	nC	di/dt = 500A/μs ⑥

**Notes:**

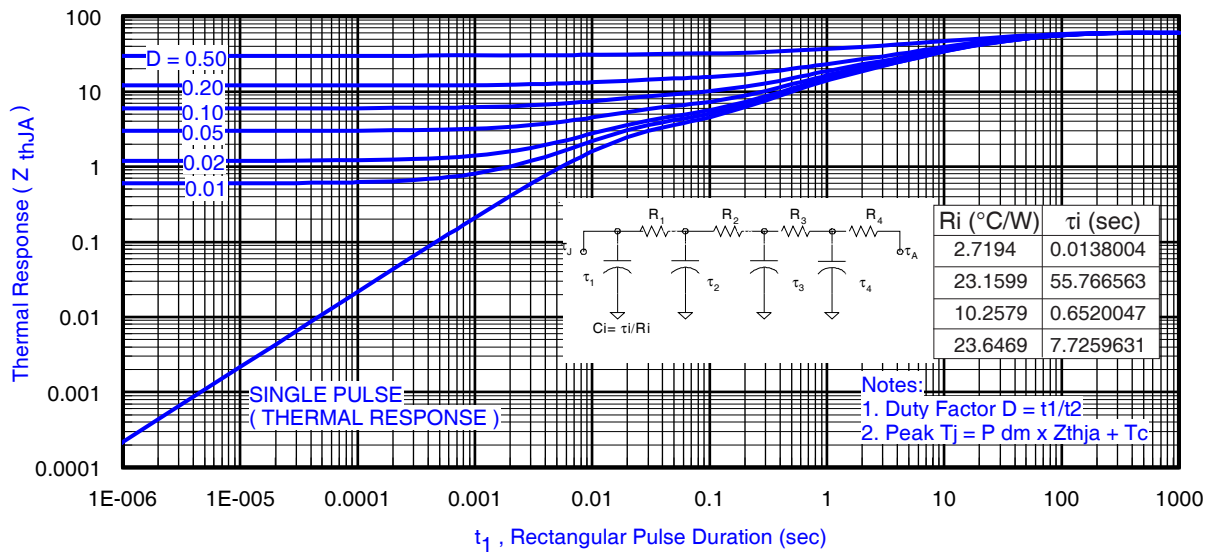
⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

**Absolute Maximum Ratings**

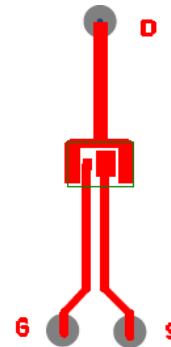
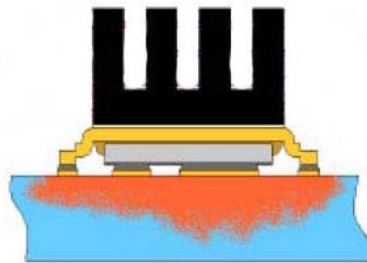
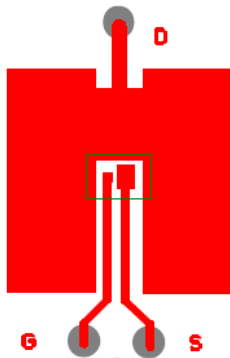
	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.1	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.3	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	113	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$	Operating Junction and	-40 to +150	
$T_{STG}$	Storage Temperature Range		

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	60	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑦	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	20	—	
$R_{\theta JC}$	Junction-to-Case ④,⑤	—	1.1	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.02		W/°C


**Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①**
**Notes:**

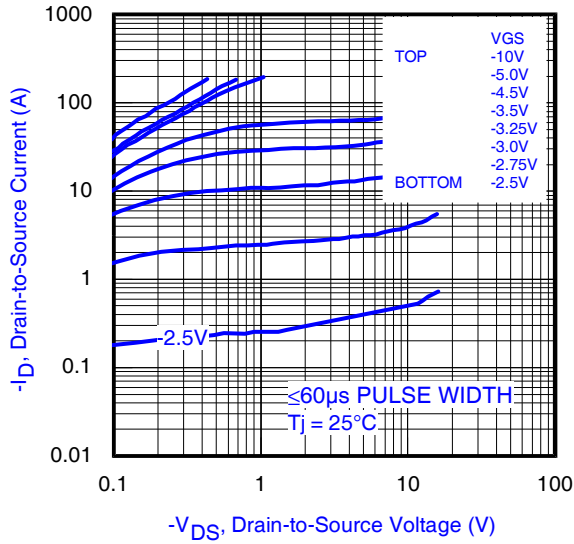
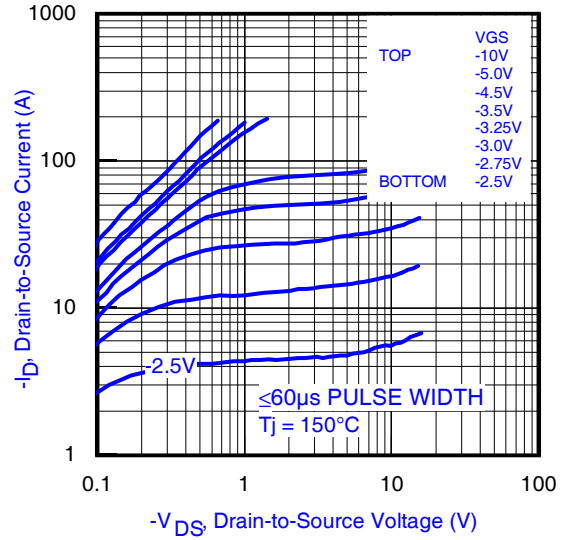
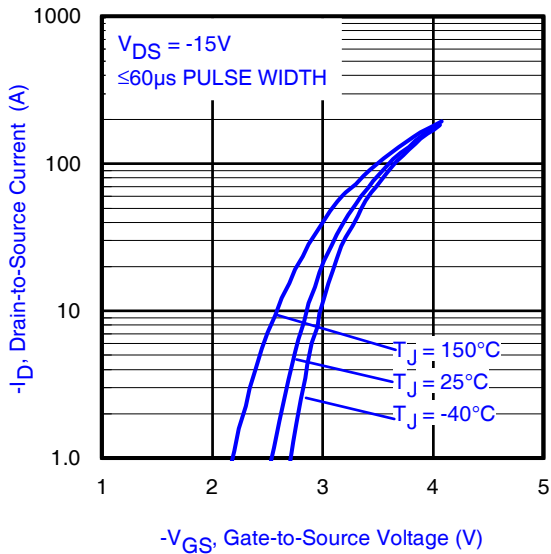
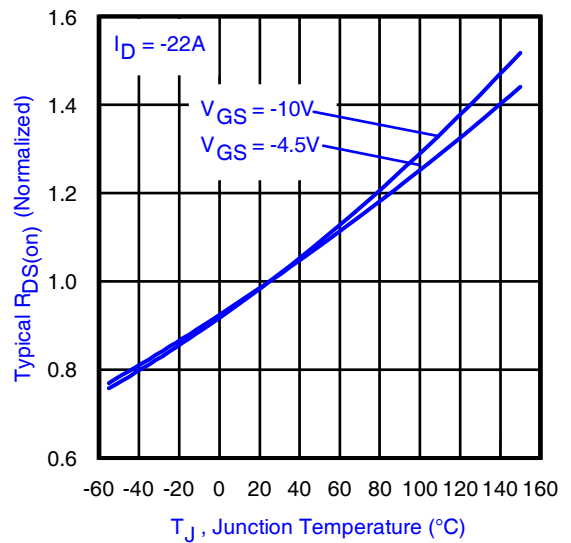
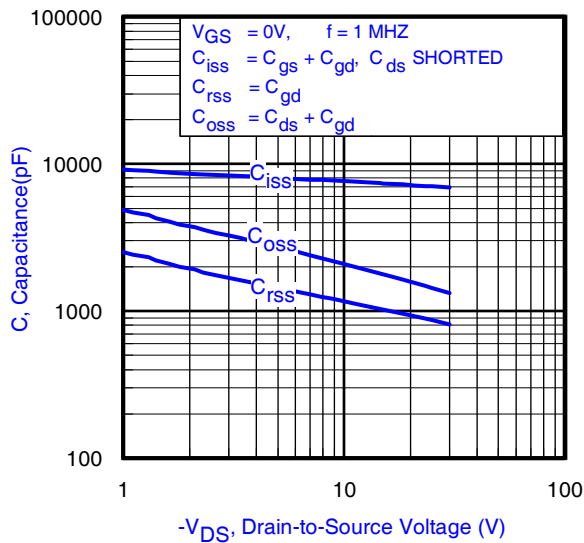
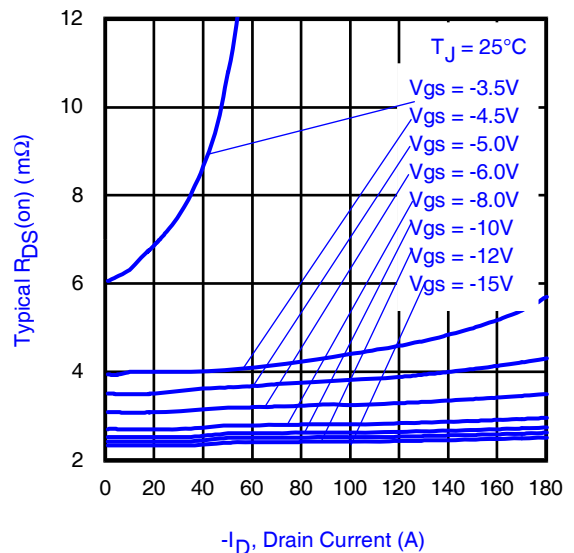
- ⑦ Used double sided cooling, mounting pad with large heatsink.
- ⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑨  $R_{\theta}$  is measured at  $T_J$  of approximately 90°C.

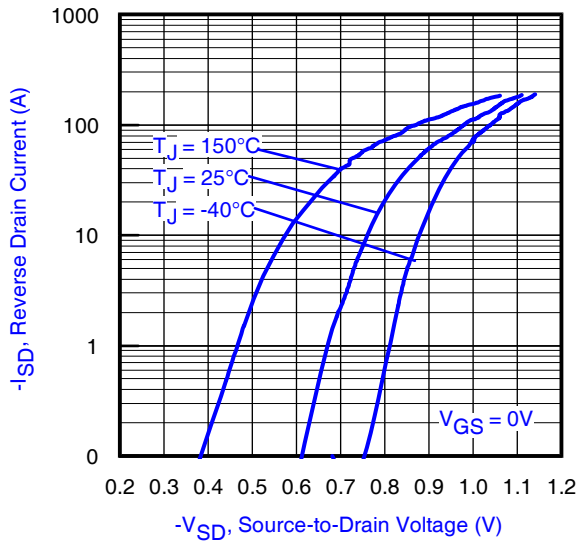
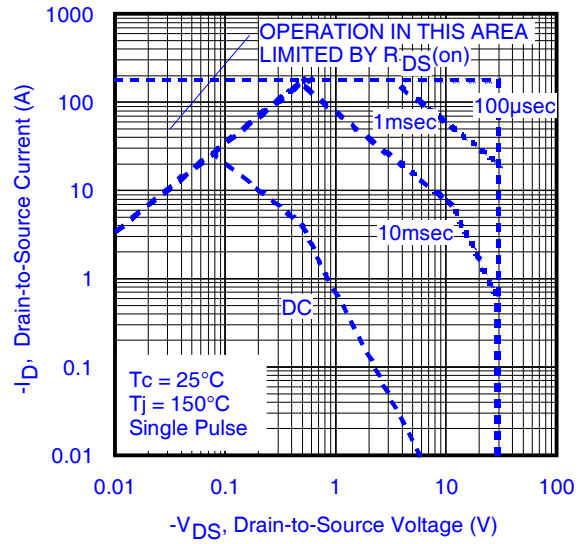
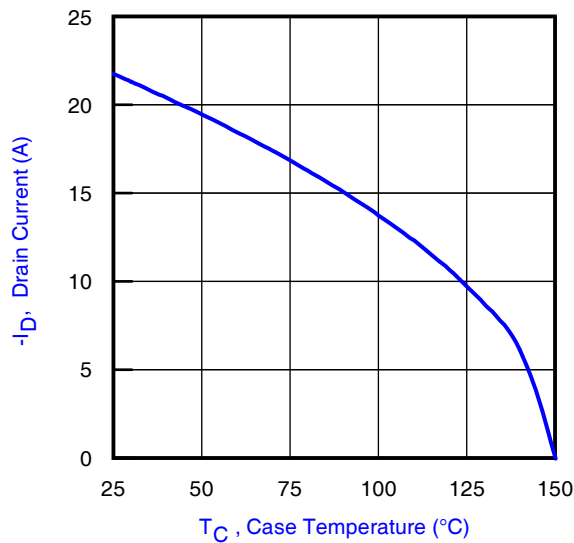
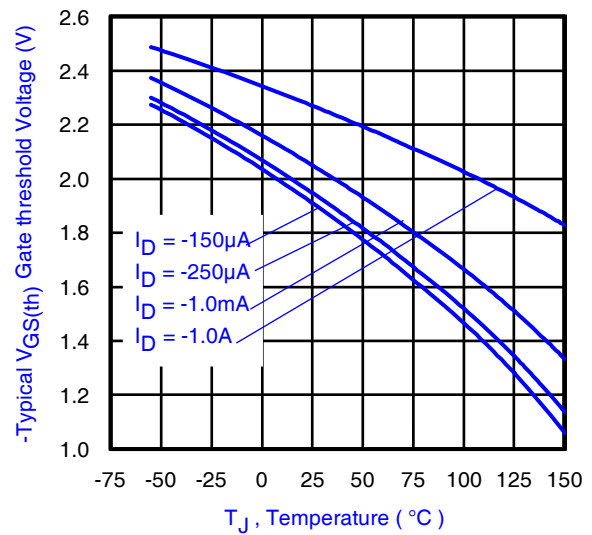
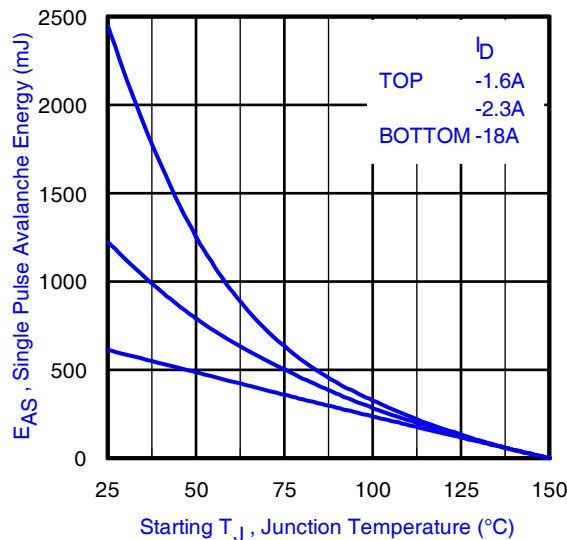


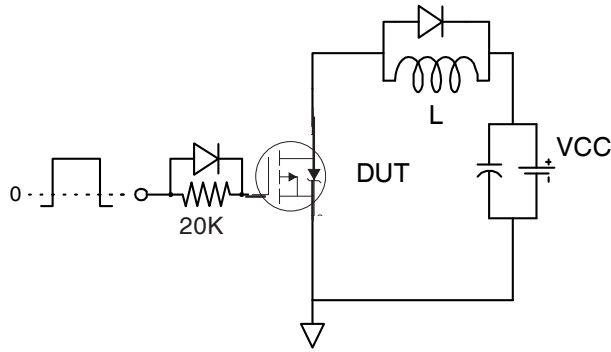
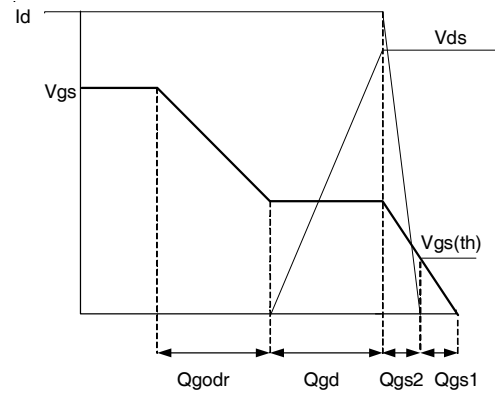
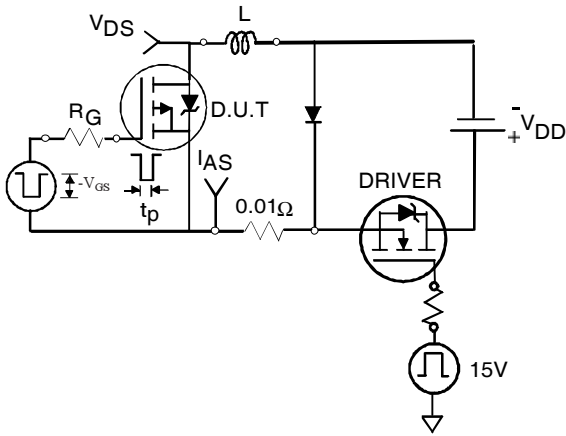
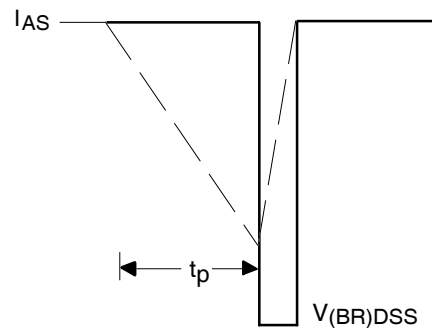
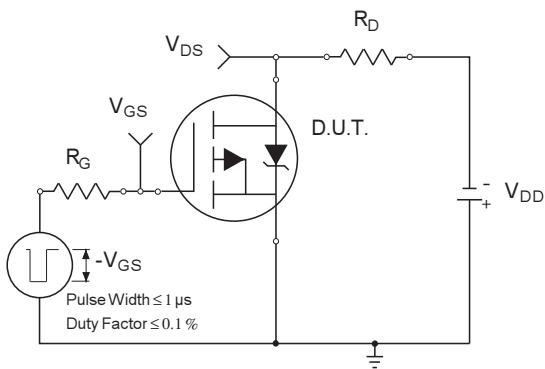
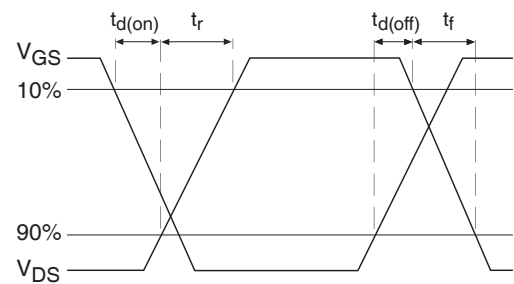
③ Surface mounted on 1 in. square Cu board (still air).

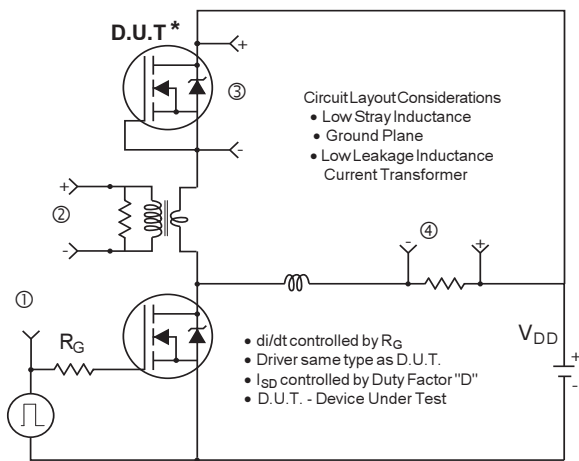
⑧ Mounted to a PCB with small clip heatsink (still air)

⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

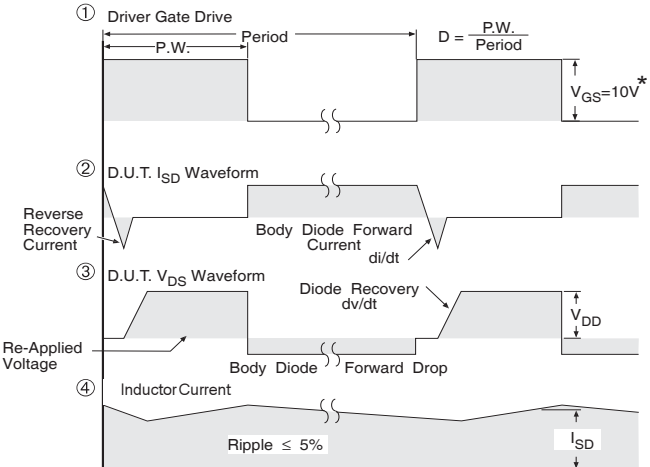

**Fig 4.** Typical Output Characteristics

**Fig 5.** Typical Output Characteristics

**Fig 6.** Typical Transfer Characteristics

**Fig 7.** Normalized On-Resistance vs. Temperature

**Fig 8.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 9.** Typical On-Resistance vs. Drain Current and Gate Voltage


**Fig 10.** Typical Source-Drain Diode Forward Voltage

**Fig 11.** Maximum Safe Operating Area

**Fig 12.** Maximum Drain Current vs. Case Temperature

**Fig 13.** Typical Threshold Voltage vs. Junction Temperature

**Fig 14.** Maximum Avalanche Energy vs. Drain Current


**Fig 17a.** Gate Charge Test Circuit

**Fig 17b.** Gate Charge Waveform

**Fig 18a.** Unclamped Inductive Test Circuit

**Fig 18b.** Unclamped Inductive Waveforms

**Fig 19a.** Switching Time Test Circuit

**Fig 19b.** Switching Time Waveforms



\* Reverse Polarity of D.U.T for P-Channel



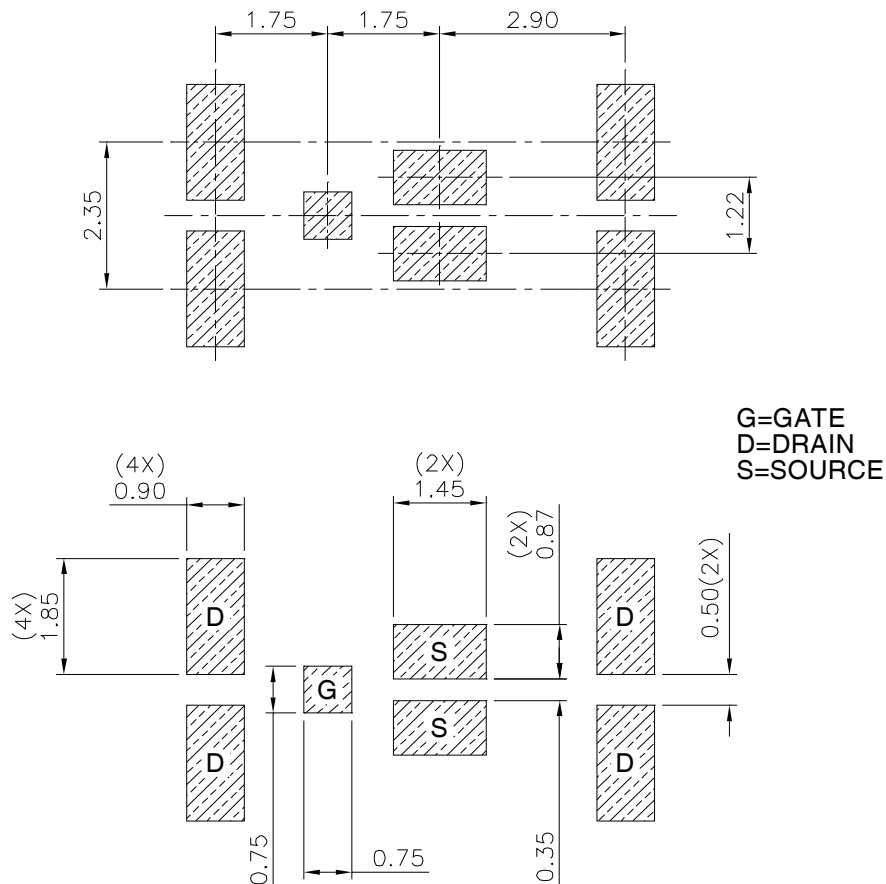
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 20. Diode Reverse Recovery Test Circuit for P-Channel HEXFET® Power MOSFETs**

### DirectFET® Board Footprint, MX Outline (Medium Size Can, X-Designation).

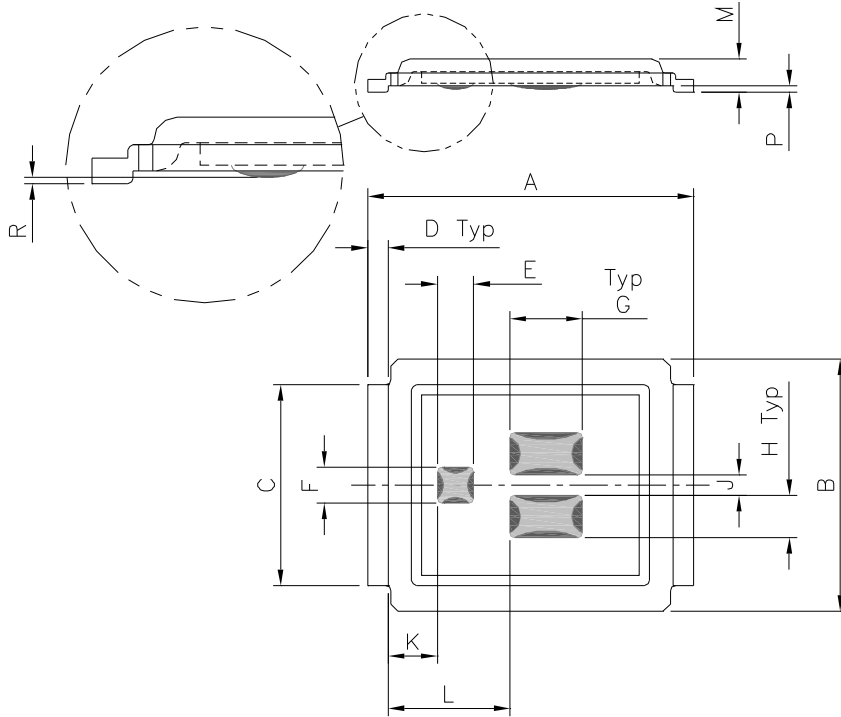
Please see DirectFET® application note AN-1035 for all details regarding the assembly of DirectFET®.

This includes all recommendations for stencil and substrate designs.



## DirectFET® Outline Dimension, MX Outline (Medium Size Can, X-Designation).

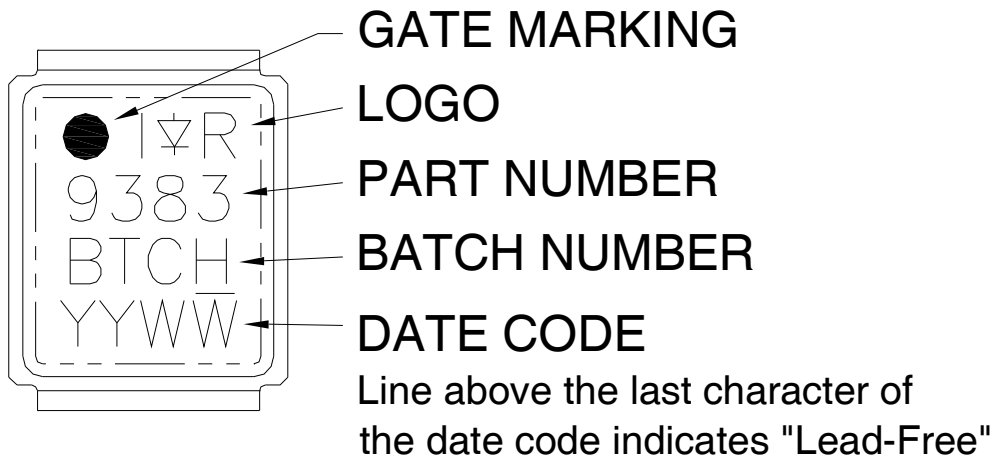
Please see DirectFET® application note AN-1035 for all details regarding the assembly of DirectFET®. This includes all recommendations for stencil and substrate designs.



CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.68	0.72	0.027	0.028
F	0.68	0.72	0.027	0.028
G	1.38	1.42	0.054	0.056
H	0.80	0.84	0.031	0.033
J	0.38	0.42	0.015	0.017
K	0.88	1.02	0.035	0.040
L	2.28	2.42	0.090	0.095
M	0.59	0.70	0.023	0.028
R	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

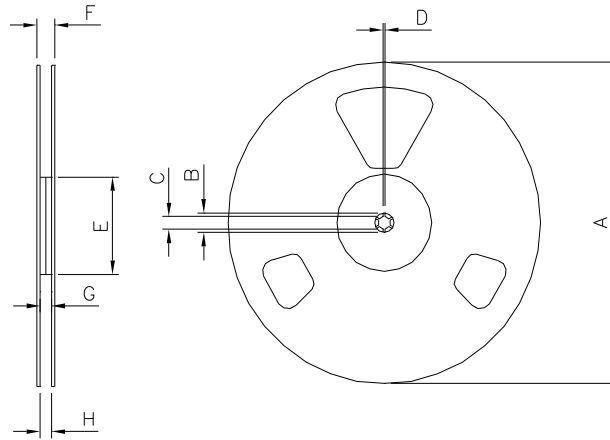
Dimensions are shown in millimeters (inches)

## DirectFET® Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

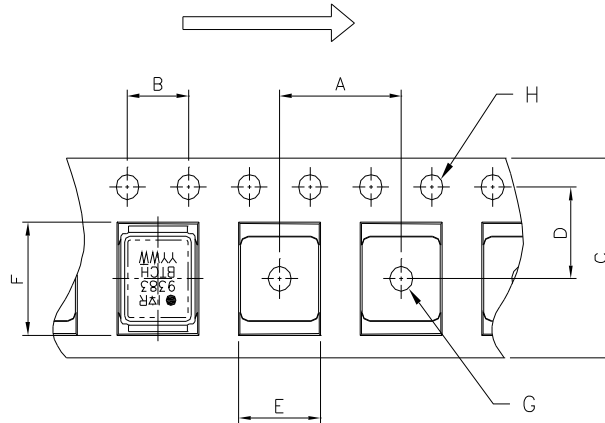


**DirectFET® Tape & Reel Dimension (Showing component orientation).**


NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. (ordered as IRF9383MTRPBF). For 1000 parts on 7" reel, order IRF9383MTR1PBF

REEL DIMENSIONS				
STANDARD OPTION (QTY 4800)				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information†**

Qualification level	Consumer ††	
	(per JEDEC JESD47F††† guidelines)	
Moisture Sensitivity Level	DirectFET®	MSL1 (per JEDEC J-STD-020D†††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site  
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
2/17/2014	<ul style="list-style-type: none"> <li>Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #264).</li> <li>Updated data sheet with new IR corporate template.</li> </ul>
2/25/2014	<ul style="list-style-type: none"> <li>Change MSL3 to MSL1, on page 9.</li> </ul>
6/2/2015	<ul style="list-style-type: none"> <li>Updated schematics from "N-Channel" to "P-Channel" on page 1.</li> <li>Updated "IFX logo" on page 1 and page 10..</li> </ul>

## **IMPORTANT NOTICE**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffheitsgarantie").

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