

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-0.2)

Product Summary

Part Number	Radiation Level	RDS(on)	Ι _D	QPL Part Number
IRHNM57110	100 kRads(Si)	0.22Ω	6.9A	JANSR2N7503U8
IRHNM53110	300 kRads(Si)	0.22Ω	6.9A	JANSF2N7503U8
IRHNM55110	500 kRads(Si)	0.22 Ω	6.9A	JANSG2N7503U8
IRHNM58110	1000 kRads(Si)	0.22Ω	6.9A	JANSH2N7503U8

Refer to page 9 for additional part number-IRHNMC57110 (Ceramic Lid)

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- Complimentary P-Channel Available -IRHNM597110, IRHNMC597110

Absolute Maximum Rat	F	re-irradiation		
Symbol	Parameter	Value	Units	
$I_{D1} \oslash V_{GS} = 12V, T_C = 25^{\circ}C$ Continuous Drain Current		6.9		
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	4.4	А	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	27.6		
P _D @ T _C = 25°C	Maximum Power Dissipation	23	W	
	Linear Derating Factor	0.18	W/°C	
V _{GS}	Gate-to-Source Voltage	± 20	V	
E _{AS}	E _{AS} Single Pulse Avalanche Energy ②		mJ	
I _{AR}	Avalanche Current ①	6.9	A	
E _{AR}	Repetitive Avalanche Energy ①	2.3	mJ	
dv/dt	Peak Diode Recovery dv/dt 3	11.5	V/ns	
T _J Operating Junction and		55 to 1 150		
T _{STG}	Storage Temperature Range	-55 to + 150	°C	
	Lead Temperature	300 (for 5s)		
	Weight	0.25 (Typical)	g	

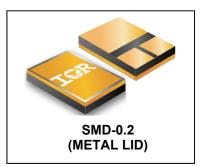
For footnotes refer to the page 2.

Absolute Maximum Patings

Dro-Irradiation

IRHNM57110 JANSR2N7503U8

100V, N-CHANNEL REF: MIL-PRF-19500/743 REF: TECHNOLOGY





Pre-Irradiation

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

		1	1	· ·		
Symbol	Parameter	Min.	Тур.	Max.		Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_{D} = 1.0mA$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.13		V/°C	Reference to 25°C, I_D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.22	Ω	V_{GS} = 12V, I_{D2} = 4.4A ④
V _{GS(th)}	Gate Threshold Voltage	2.0		4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Coefficient		-7.5		mV/°C	$v_{\text{DS}} = v_{\text{GS}}, i_{\text{D}} = 1.011\text{A}$
Gfs	Forward Transconductance	3.6			S	V _{DS} = 15V, I _{D2} = 4.4A ④
I _{DSS}	Zero Gate Voltage Drain Current			10	μA	V _{DS} = 80V, V _{GS} = 0V
				25	μΛ	$V_{DS} = 80V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Leakage Forward			100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse			-100		V _{GS} = -20V
Q _G	Total Gate Charge			15		I _{D1} = 6.9A
Q_{GS}	Gate-to-Source Charge			4.0	nC	V _{DS} = 50V
Q _{GD}	Gate-to-Drain ('Miller') Charge			5.0		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time			6.6		V _{DD} = 50V
Tr	Rise Time			8.0	20	I _{D1} = 6.9A
t _{d(off)}	Turn-Off Delay Time			34	ns	R _G = 7.5Ω
Tf	Fall Time			15		V _{GS} = 12V
Ls +L _D	Total Inductance		6.8		nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance		378			V _{GS} = 0V
C _{oss}	Output Capacitance		108		pF	V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance		2.3			<i>f</i> = 100KHz
R _G	Gate Resistance		8.0		Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current (Body Diode)			6.9	^	
I _{SM}	Pulsed Source Current (Body Diode) ①			27.6	A	
V _{SD}	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 6.9A, V_{GS} = 0V ④$
t _{rr}	Reverse Recovery Time			144	ns	$T_{\text{J}} = 25^{\circ}C \ , I_{\text{F}} = 6.9 \text{A}, \ V_{\text{DD}} \ \leq 50 \text{V}$
Q _{rr}	Reverse Recovery Charge			633	nC	di/dt = 100A/µs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Units
$R_{ ext{ heta}JC}$	Junction-to-Case			5.4	°C/W

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- $@~V_{\text{DD}}$ = 50V, starting T_{J} = 25°C, L =1.0mH, Peak I_L = 6.9A, V_{GS} = 12V
- $\label{eq:ISD} \textcircled{3} \quad I_{SD} \leq 6.9 A, \ di/dt \leq 560 A/\mu s, \ V_{DD} \leq 100 V, \ T_J \leq 150^\circ C$
- $\ \, { \mbox{ Pulse width } \leq 300 \ \mu s; \ \, Duty \ \, Cycle \leq 2\% }$
- \odot Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- \odot Total Dose Irradiation with V_{DS} Bias. 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.



Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Symbol	Parameter	Up to 500 kRads (Si) ¹		1000 kRads (Si) ²		Units	Test Conditions	
		Min.	Max.	Min.	Max.			
BV _{DSS}	Drain-to-Source Breakdown Voltage	100		100		V	V_{GS} = 0V, I_{D} = 1.0mA	
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0$ mA	
I _{GSS}	Gate-to-Source Leakage Forward		100		100	nA	V _{GS} = 20V	
I _{GSS}	Gate-to-Source Leakage Reverse		-100		-100	nA	V _{GS} = -20V	
I _{DSS}	Zero Gate Voltage Drain Current		10		10	μA	V_{DS} = 48V, V_{GS} = 0V	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO - 3)		0.226		0.246	Ω	V _{GS} = 12V, I _{D2} = 4.4A	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SMD – 0.2)		0.226		0.246	Ω	V _{GS} = 12V, I _{D2} = 4.4A	
V _{SD}	Diode Forward Voltage ④		1.2		1.2	V	V_{GS} = 0V, I _S = 6.9A	

1. Part numbers IRHNM57110 (JANSR2N7503U8), IRHNM53110 (JANSF2N7503U8), and IRHNM55110 (JANSG2N7503U8),

2. Part numbers IRHNM58110 (JANSH2N7503U8)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

	F				VDS (V)		
LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	100	100	100	100	100
61 ± 5%	330 ± 7.5%	31 ± 10%	100	100	100	35	25
84 ± 5%	350 ± 10%	28 ± 7.5%	100	100	80	25	

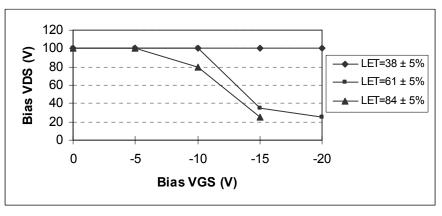


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the page 2.



Pre-Irradiation

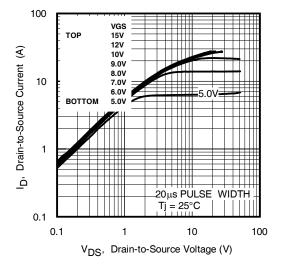


Fig 1. Typical Output Characteristics

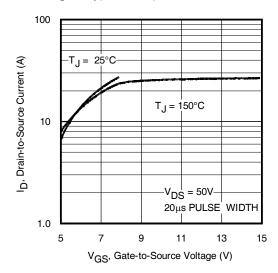


Fig 3. Typical Transfer Characteristics

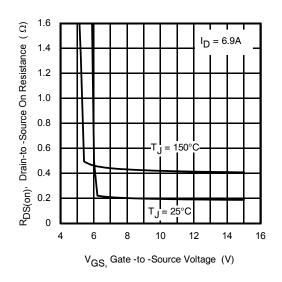


Fig 5. Typical On-Resistance Vs Gate Voltage

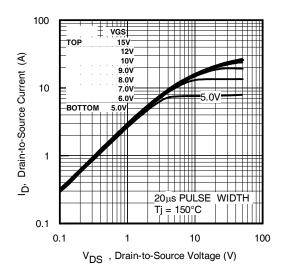


Fig 2. Typical Output Characteristics

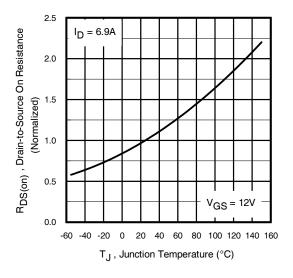


Fig 4. Normalized On-Resistance Vs. Temperature

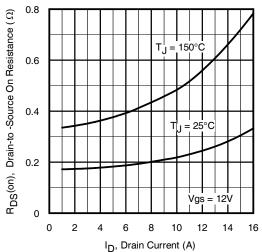


Fig 6. Typical On-Resistance Vs Drain Current



Pre-Irradiation

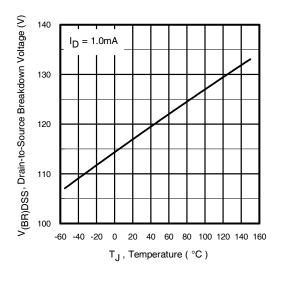


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

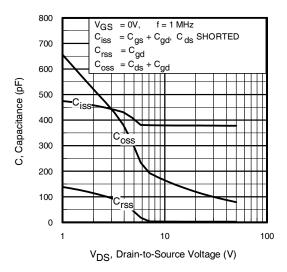


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

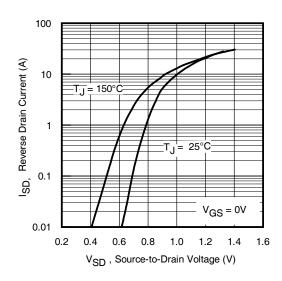


Fig 11. Typical Source-Drain Diode Forward Voltage

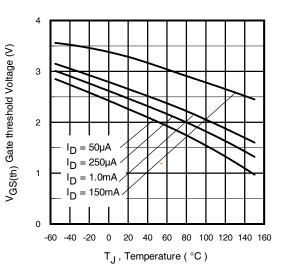


Fig 8. Typical Threshold Voltage Vs Temperature

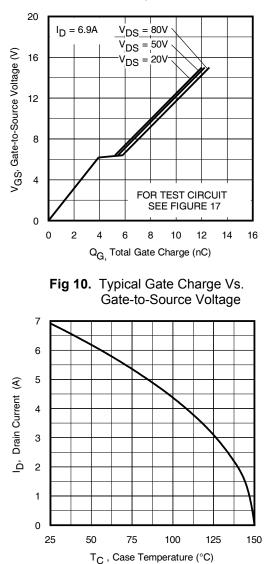


Fig 12. Maximum Drain Current Vs.Case Temperature



Pre-Irradiation

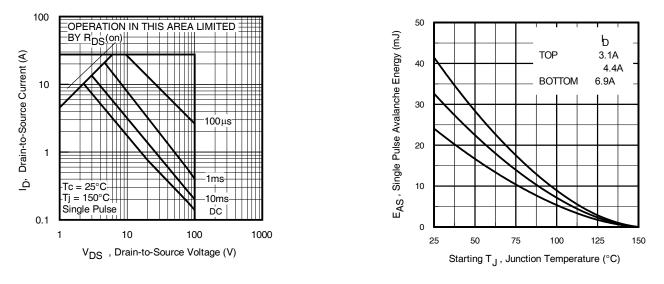


Fig 13. Maximum Safe Operating Area

Fig 14. Maximum Avalanche Energy Vs. Drain Current

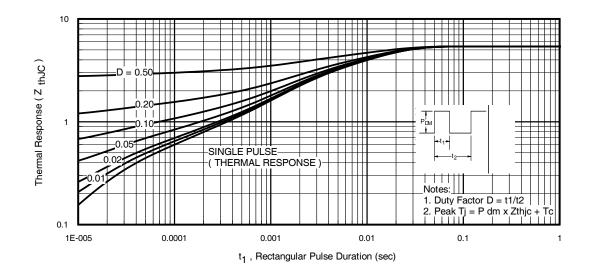


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Pre-Irradiation

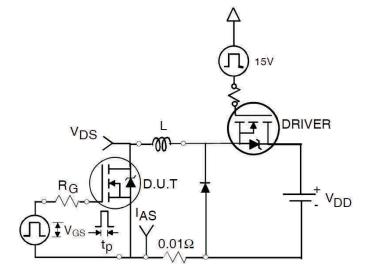


Fig 16a. Unclamped Inductive Test Circuit

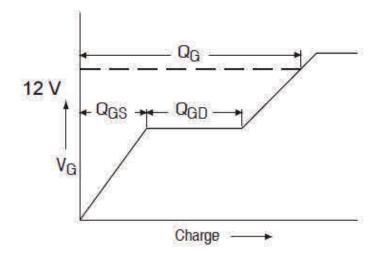


Fig 17a. Gate Charge Waveform

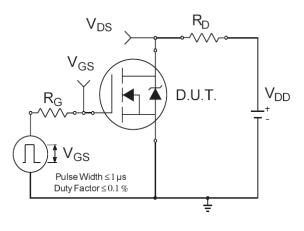
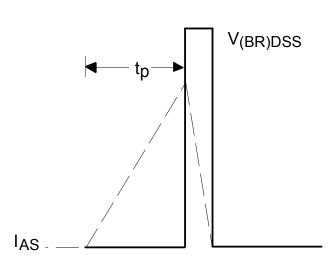
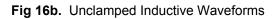


Fig 18a. Switching Time Test Circuit





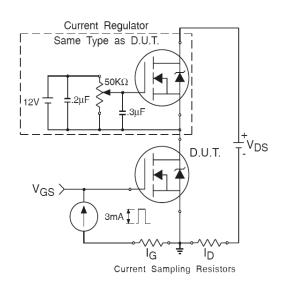


Fig 17b. Gate Charge Test Circuit

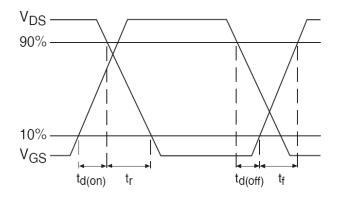
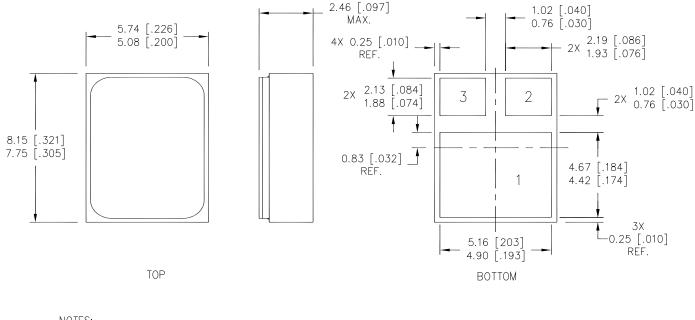


Fig 18b. Switching Time Waveforms



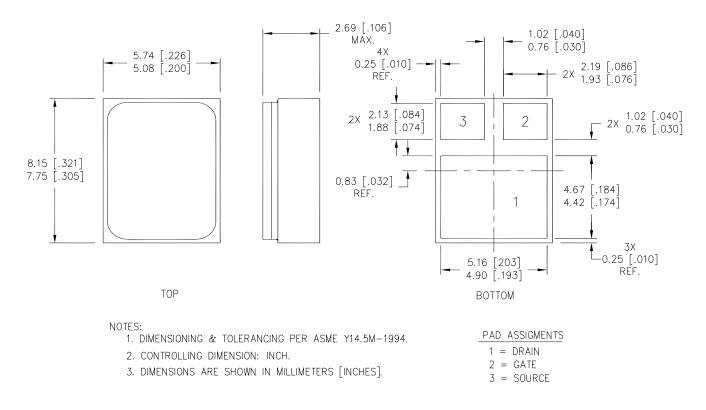
Case Outline and Dimensions - SMD-0.2 (Metal Lid)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.	PAD ASSIGMENTS
2. CONTROLLING DIMENSION: INCH.	1 = DRAIN
3. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].	2 = GATE
o. Dimensiona vice shown in include [imelimenents].	3 = SOURCE

Case Outline and Dimensions - SMD-0.2 (Ceramic Lid)





Additional Product Summary (continued from pages 1 and 3)

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number	\langle
IRHNMC57110	100 kRads(Si)	0.22Ω	6.9A	JANSR2N7503U8C	SMD-0.2
IRHNMC53110	300 kRads(Si)	0.22Ω	6.9A	JANSF2N7503U8C	(CERAMIC LID)
IRHNMC55110	500 kRads(Si)	0.22Ω	6.9A	JANSG2N7503U8C	
IRHNMC58110	1000 kRads(Si)	0.22Ω	6.9A	JANSH2N7503U8C	



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Infineon Technologies Service Center: USA Tel: +1 (866) 951-9519 and International Tel: +49 89 234 65555 Leominster, Massachusetts 01453, USA Tel: +1 (978) 534-5776 San Jose, California 95134, USA Tel: +1 (408) 434-5000 Data and specifications subject to change without notice.



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