2.5V/3.3V 1.5GHz Low Skew 1-to-10 Differential to LVPECL Fanout Buffer with 2 to 1 Differential Clock Input Mux

Features

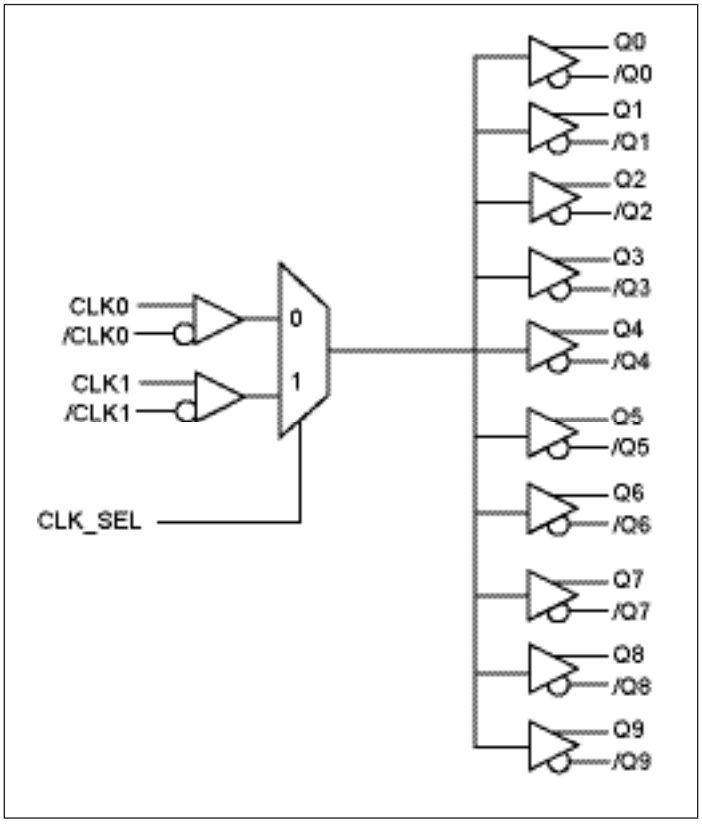
- ➔ F_{MAX} < 1.5GHz
- ➔ 10 pairs of differential LVPECL outputs
- ➔ Low additive jitter, < 0.03ps (typ)
- ➔ Selectable differential input pairs with single ended input option
- ➔ Input CLK accepts: LVPECL, LVDS, CML, SSTL input level
- ➔ Output skew: 40ps (typ)
- ➔ Operating Temperature: -40°C to 85°C
- ➔ Core Power supply: 2.5V ±5% & 3.3V ±10%, Output Power supply: 2.5V ±5% & 3.3V ±10%
- ➔ Packaging (Pb-free & Green):
- ➔ 32-pin QFN and TQFP available

Description

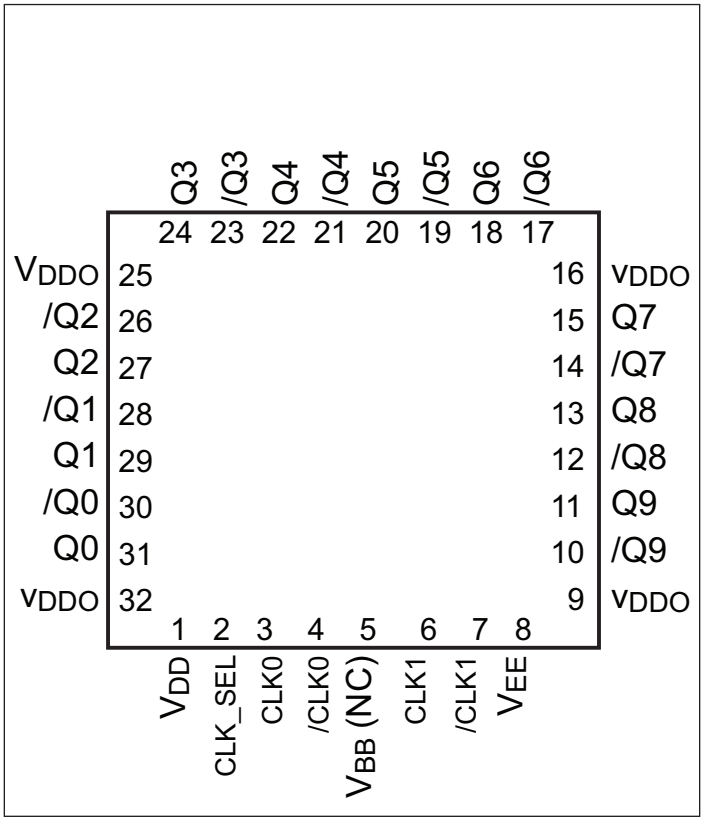
The PI6C4911510 is a high-performance low-skew 1-to-10 LVPECL fanout buffer. The PI6C4911510 features two selectable differential clock inputs and translates to ten LVPECL outputs. The CLK inputs accept LVPECL, LVDS, CML and SSTL signals.

PI6C4911510 is ideal for clock distribution applications such as providing fanout for low noise SaRonix-eCera oscillators.

Block Diagram



Pin Configuration



Pin Description(1)

Pin #	Name	Type	Description
1	V_{DD}	Power	Core Power Supply
2	CLK_SEL	Input	Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50kΩ pull down.
3	CLK0	Input	Differential clock input with pull-down
4	/CLK0	Input	Inverting differential clock input. Defaults to $V_{DD}/2$ if left floating.
5	V_{BB} (NC)	Power	Internal Common Mode Voltage, can be left as not connected if unused.
6	CLK1	Input	Differential clock input with pull-down
7	/CLK1	Input	Inverting differential clock input. Defaults to $V_{DD}/2$ if left floating.
8	V_{EE}	Power	Connect to negative power supply
9, 16, 25, 32	V_{DDO}	Power	Output Power pin
11, 10	Q9, /Q9	Output	Differential output pair, LVPECL interface level.
13,12	Q8, /Q8	Output	Differential output pair, LVPECL interface level.
15,14	Q7, /Q7	Output	Differential output pair, LVPECL interface level.
18,17	Q6, /Q6	Output	Differential output pair, LVPECL interface level.
20,19	Q5, /Q5	Output	Differential output pair, LVPECL interface level.
22,21	Q4, /Q4	Output	Differential output pair, LVPECL interface level.
24, 23	Q3, /Q3	Output	Differential output pair, LVPECL interface level.
27,26	Q2, /Q2	Output	Differential output pair, LVPECL interface level.
29,28	Q1, /Q1	Output	Differential output pair, LVPECL interface level.
31,30	Q0, /Q0	Output	Differential output pair, LVPECL interface level.

Note:
1. I = Input, O = Output, P = Power supply connection.

Control Input Function Table

CLK_SEL	Outputs
0	CLK0
1	CLK1

Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{DD}+0.5V	V
IOUT	Surge Current				100	mA
T_{STG}	Storage temperature		-55		150	°C
V_{BB}	Sink/source Current, I_{BB}		-0.5		+0.5	mA
T_j	Junction Temperature				125	°C

Note:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Core Power Supply Voltage		2.375		3.6	V
V_{DDO}	Output Power Supply Voltage		2.375		3.6	V
T_A	Ambient Temperature		-40		85	°C
I_{DD}	Core Power Supply Current			70	95	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded		110	200	

LVCMOS/LVTTL DC Characteristics (TA = -40°C to +85°C, VDD = 3.3V ±10%, VDDO = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage	CLK_SEL		1.7		V_{DD}+0.3	V
V_{IL}	Input Low Voltage	CLK_SEL		-0.3			
I_{IH}	Input High Current	CLK_SEL	$V_{IN} = V_{DD} = 3.6V$			150	µA
I_{IL}	Input Low Current	CLK_SEL	$V_{IN} = 0V, V_{DD} = 3.6V$	-150			µA
R	Input Pullup/Pulldown Resistance				50		kΩ

LVPECL DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
		/CLK0, /CLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
		/CLK0, /CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{CMR}	Common Mode Input Voltage(1)			V_{EE}+0.5		V_{DD}	V
V_{OH}	Output High Voltage(2)		V_{DDO} = 2.5V or 3.3V	V_{DDO}-1.5	V_{DDO}-1.4	V_{DDO}-0.9	V
V_{OL}	Output Low Voltage(2)		V_{DDO} = 2.5V or 3.3V	V_{DDO}-2.2	V_{DDO}-2.0	V_{DDO}-1.7	V
R	Input Pullup/Pulldown Resistance				50		kΩ

Notes:

1. For single-ended applications, the maximum input voltage for CLK and /CLK is V_{DD}+0.3V
2. Outputs terminated with 50Ω to V_{DD}-2.0V

AC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency				1500	MHz
t_{pd}	Propagation Delay(1)			1200		ps
Tsk	Output-to-output Skew(2)			40		ps
t_r/t_f	Output Rise/Fall time	20% - 80%		150		ps
t_{odc}	Output duty cycle	f ≤ 650 MHz	48		52	%
V_{PP}	Output Swing	LVPECL outputs	0.6	1.0		V
t_j	Buffer additive jitter RMS	156.25MHz (12KHz-20MHz integration range) Input condition per Phase Noise and Additive Jitter Plot below		0.03	0.05	ps

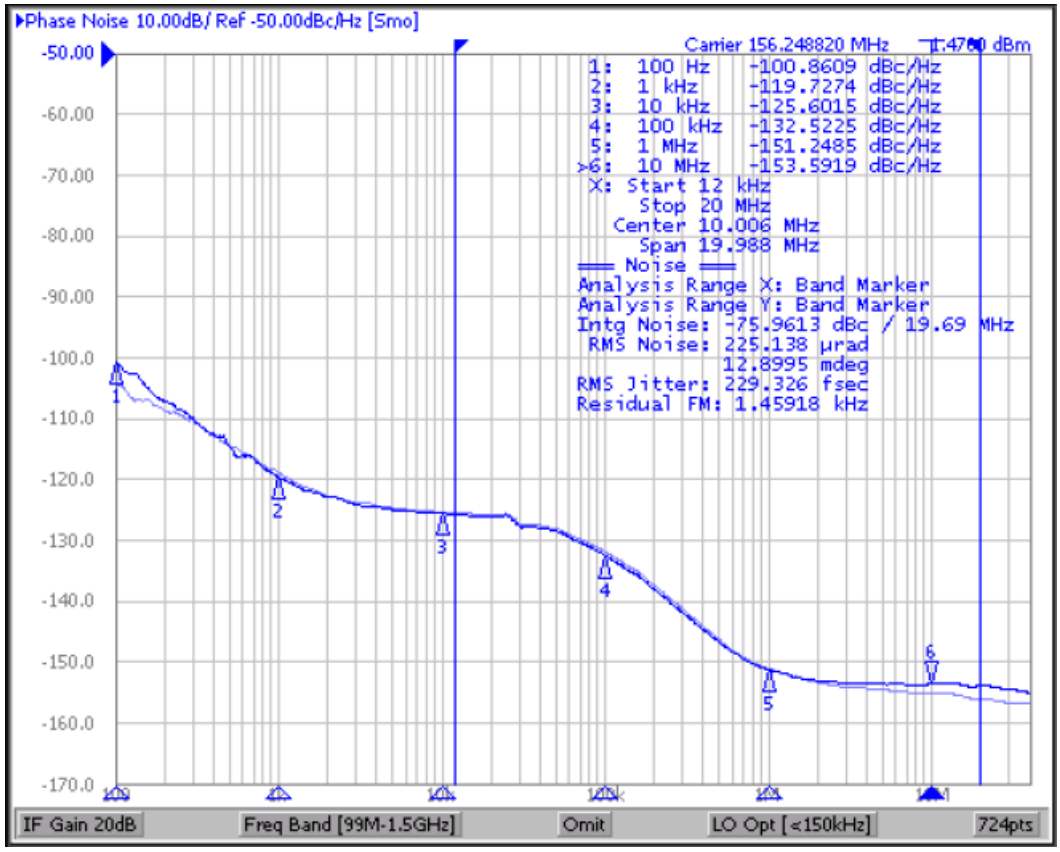
Notes:

1. Measured from the differential input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point

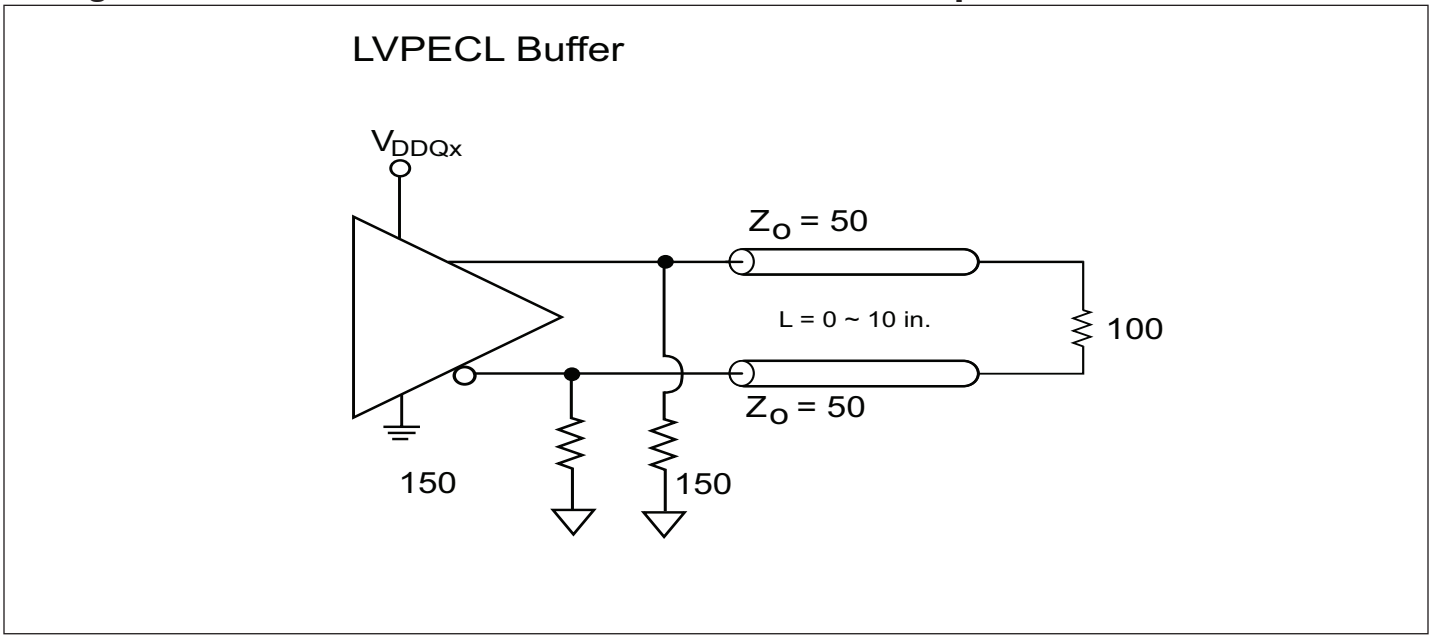
Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at ~27fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



Configuration Test Load Board Termination for LVPECL Outputs



Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

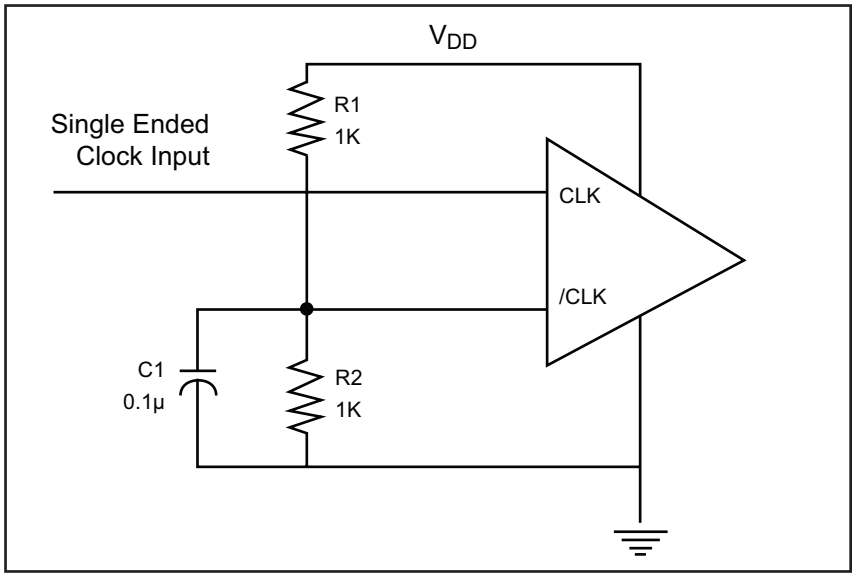
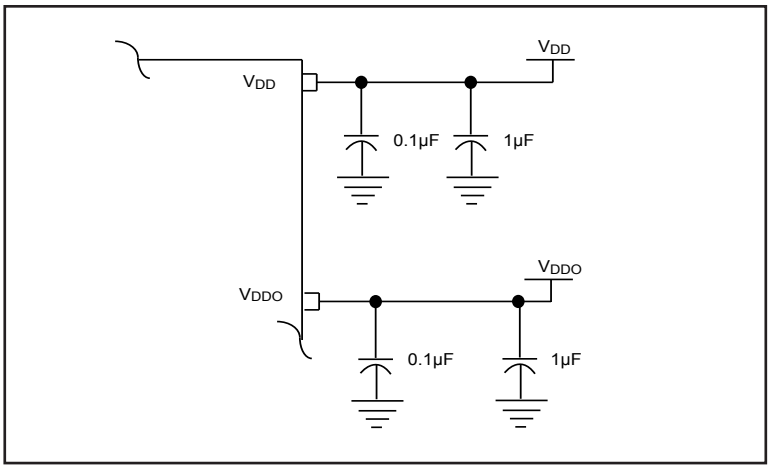


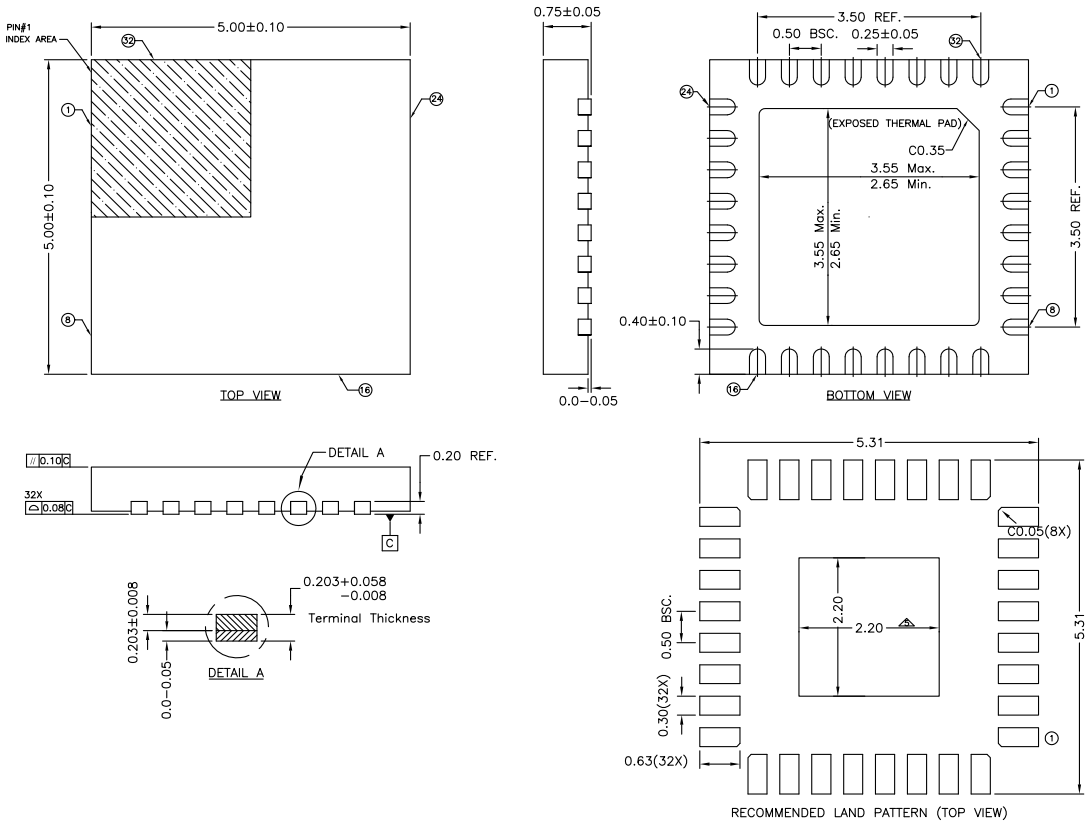
Figure 1. Single-ended input to Differential input device

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.



Packaging Mechanical: 32-pin QFN (ZH)



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area (mesh stencile design is recommended)

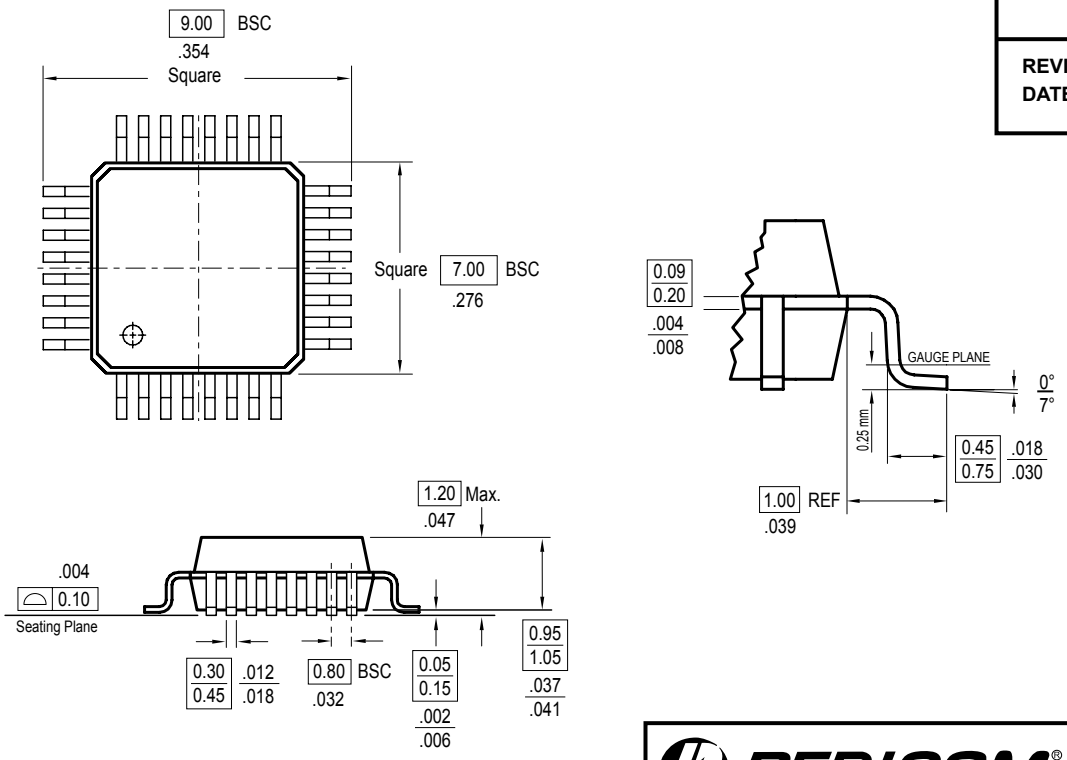
PERICOM Enabling Serial Connectivity	DATE: 06/30/11
DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZH32	
DOCUMENT CONTROL #: PD-2070	REVISION: B

11-0147

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	44.70 °C/W
Θ_{JC}	Junction-to-case thermal resistance		21.70 °C/W

Packaging Mechanical: 32-pin TQFP (FA)



DOCUMENT CONTROL NO.
PD - 1814

REVISION: C
DATE: 03/09/05

X.XX
X.XX DENOTES DIMENSIONS IN MILLIMETERS

Notes:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-026D/ABA
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM®
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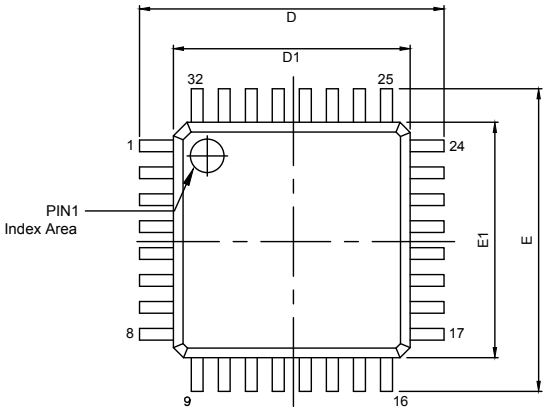
DESCRIPTION: 32-Pin, Thin Quad Flat Package, TQFP

PACKAGE CODE: FA

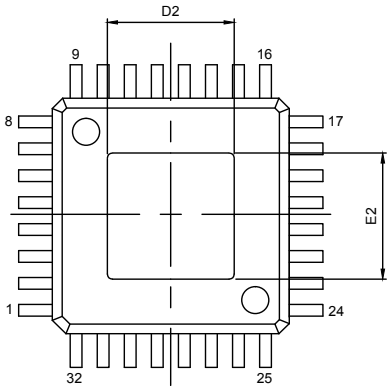
Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	86 °C/W
Θ_{JC}	Junction-to-case thermal resistance		12.7 °C/W

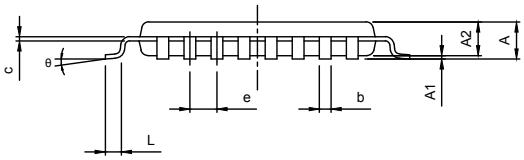
Packaging Mechanical: 32-pin TQFP with E-Pad (FAE)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOLS	MIN.	MAX.
A	-	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.09	0.20
D	8.75	9.25
D1	6.90	7.10
E	8.75	9.25
E1	6.90	7.10
e	0.80 BSC	
L	0.45	0.75
D2	3.19	3.90
E2	3.19	3.90
θ	0°	7°

NOTES:
1.Ref: JEDEC MS-026 ABA-HD

PERICOM Enabling Serial Connectivity

DATE: 03/24/15

DESCRIPTION: 32-Pin, TQFP, 7X7, Exposed Pad

PACKAGE CODE: FAE (FAE32)

DOCUMENT CONTROL #: PD-2196 REVISION: --

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	45 °C/W
Θ_{JC}	Junction-to-case thermal resistance		15 °C/W

Ordering Information[1,2,3]

Ordering Code	Package Code	Package Description
PI6C4911510ZHIE	ZH	Pb-free & Green, 32-pin QFN
PI6C4911510ZHIEX	ZH	Pb-free & Green, 32-pin QFN, Tape & Reel
PI6C4911510FAIE	FA	Pb-free & Green, 32-pin TQFP
PI6C4911510FAIEX	FA	Pb-free & Green, 32-pin TQFP, Tape & Reel
PI6C4911510FAEIE	FAE	Pb-free & Green, 32-pin TQFP E-Pad
PI6C4911510FAEIEX	FAE	Pb-free & Green, 32-pin TQFP E-Pad, Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. X suffix = Tape/Reel