

## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## Bare Die

OptiMOS™3 Power MOS Transistor Chip  
IPC302N20N3

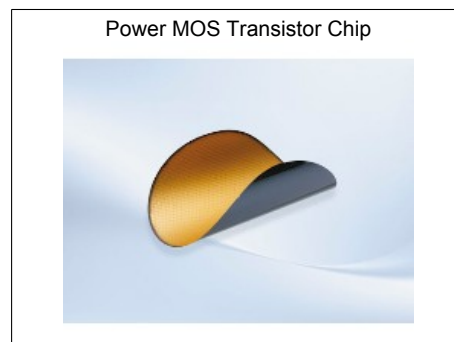
## Data Sheet

Rev. 2.6  
Final

Industrial & Multimarket

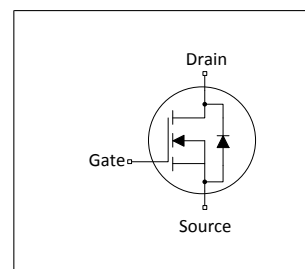
## 1 Description

- N-channel enhancement mode
- For additional characteristic and max ratings refer to the datasheet of IPP110N20N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride (only on edge structure)



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{(BR)DSS}$	200	V
$R_{DS(on)}$	12 <sup>1)</sup>	mΩ
Die size	6.7 x 4.5	mm <sup>2</sup>
Thickness	250	μm



Type / Ordering Code	Package	Marking	Related Links
IPC302N20N3	Chip	not defined	-

## 2 Electrical Characteristics on Wafer Level

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}, I_D=260\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	1	μA	$V_{GS}=0\text{ V}, V_{DS}=160\text{ V}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on- resistance	$R_{DS(on)}$	-	9.2 <sup>2)</sup>	100 <sup>3)</sup>	mΩ	$V_{GS}=10\text{ V}, I_D=2.0\text{ A}$
Reverse diode forward on-voltage	$V_{SD}$	-	1.0	1.2	V	$V_{GS}=0\text{ V}, I_F=1\text{ A}$
Avalanche energy, single pulse	$E_{AS}$	-	47 <sup>4)</sup>	-	mJ	$I_D=30\text{ A}, R_{GS}=25\text{ }\Omega$

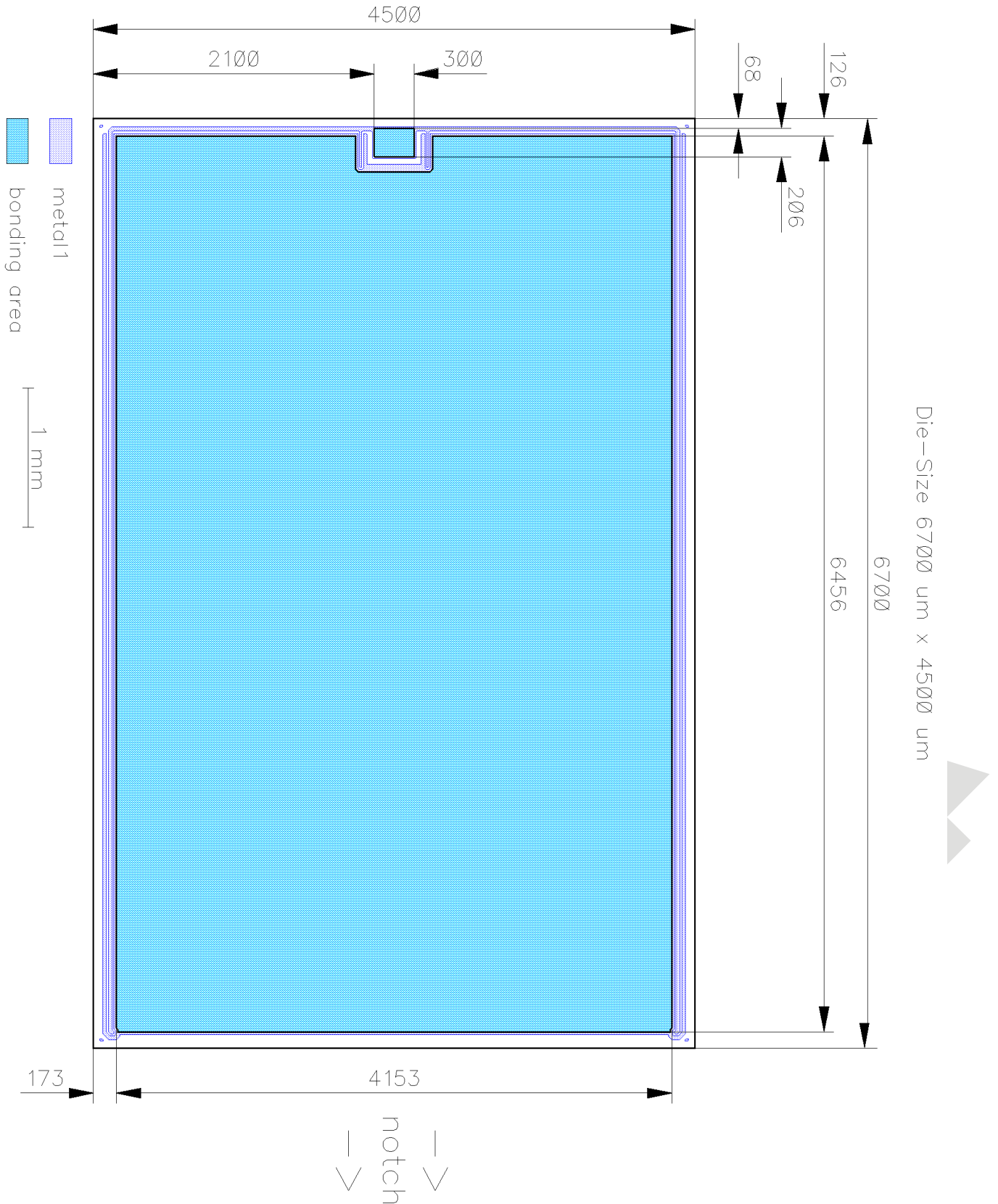
<sup>1)</sup> packaged in a P-TO220-3 (see ref. product)

<sup>2)</sup> typical bare die  $R_{DS(on)}$ ;  $V_{GS}=10\text{ V}$

<sup>3)</sup> limited by wafer test-equipment

<sup>4)</sup> Wafer tested. For general avalanche capability refer to the datasheet of IPP110N20N3 G

### 3 Package Outlines



**Figure 1 Outline Chip, dimensions in  $\mu\text{m}$**

## Revision History

IPC302N20N3

**Revision: 2015-04-08, Rev. 2.6**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.6	-	Release Final Version

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