

OptiMOS™3 Power MOS Transistor Chip

Type	$V_{(BR)DSS}$	$R_{DS(on)}$	Die size	Thickness
IPC300N20N3	200 V	11 mΩ ¹⁾	6 * 5 mm ²	250 μm

DESCRIPTION

- N-channel enhancement mode
- For additional characteristics and max rating refer to the datasheet of IPP110N20N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AISiCu system
- Passivation: nitride + imide (only on edge structure)
- Package: sawn on foil

Electrical Characteristics on Wafer Level

at $T_j = 25\text{ °C}$, unless otherwise specified.

Parameter	Symbol	Value			Unit	Conditions
		min.	typ.	max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	$V_{GS} = 0V$ $I_D = 1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS} = V_{GS}$ $I_D = 270\text{ μA}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{GS} = 0V$ $V_{DS} = 160\text{ V}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS} = 20\text{ V}$ $V_{DS} = 0\text{ V}$
Drain-source on-resistance	$R_{DS(on)}$	-	9.2 ³⁾	100 ²⁾	mΩ	$V_{GS} = 10\text{ V}$ $I_D = 2.0\text{ A}$
Reverse diode forward on-voltage	V_{SD}	-	1.0	1.2	V	$V_{GS} = 0\text{ V}$ $I_F = 1\text{ A}$
Avalanche energy, single pulse	E_{AS}	-	40 ⁴⁾	-	mJ	$I_D = 30\text{ A}$, $R_{GS} = 25\text{ Ω}$

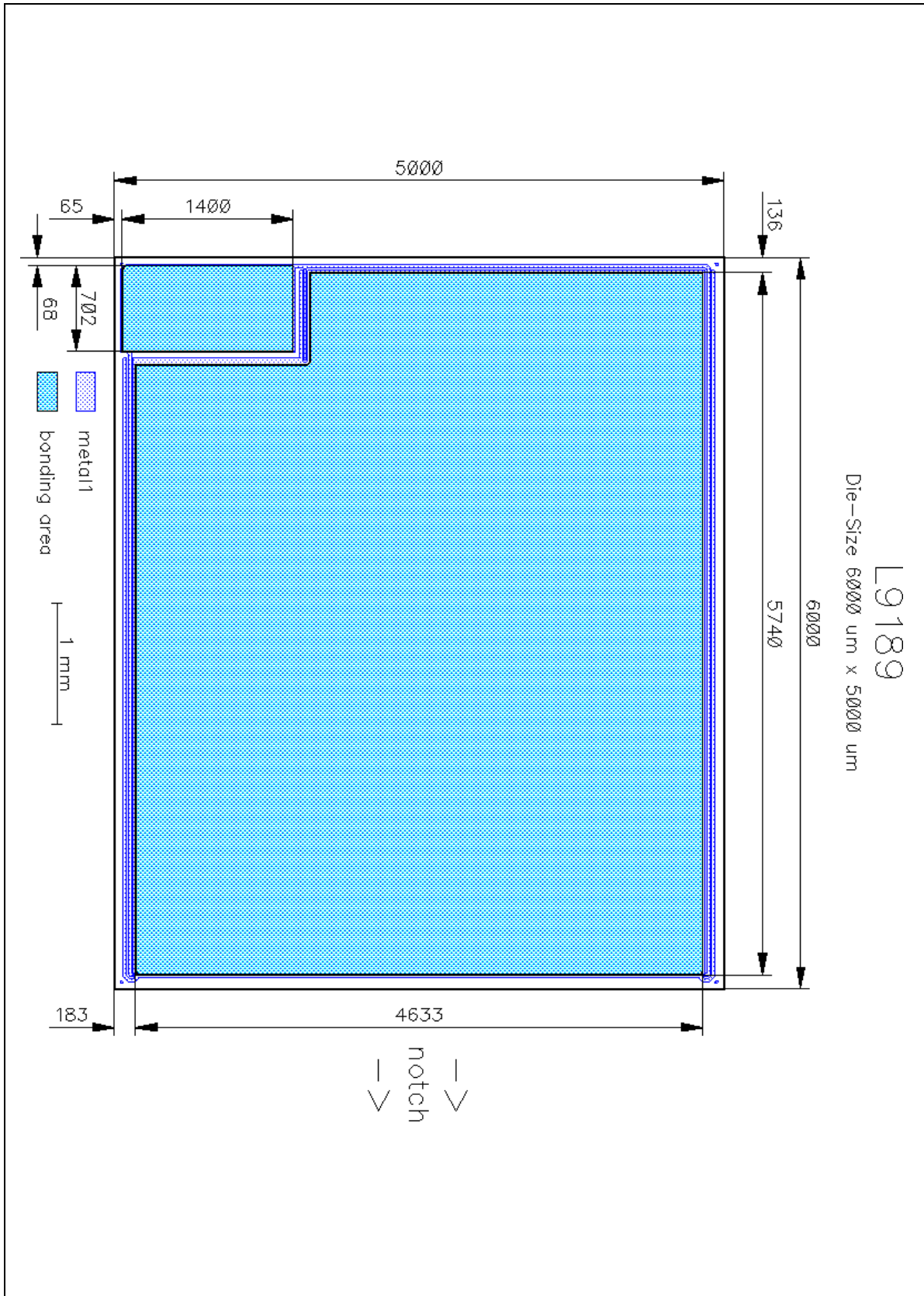
¹⁾ packaged in a P-TO220-3 (see ref. product)

²⁾ limited by wafer test-equipment

³⁾ typical bare die $R_{DS(on)}$; $V_{GS} = 10V$

⁴⁾ Wafer tested. For general avalanche capability refer to the datasheet of IPP110N20N3 G

Chip-Layout:





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