IOR HiRel
An Infineon Technologies Company

IRFE9130
JANTX2N6849U
JANTXV2N6849U

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET® TRANSISTORS

100V, P-CHANNEL
REF: MIL-PRF-19500/564

LCC-18

Product Summary

Part Number	BVDSS	$R_{DS(on)}$	I_D
IRFE9130	-100V	0.30Ω	-6.5A

Description

The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. Designed to be a close replacement for the TO-39 package, the LCC will give designers the extra flexibility they need to increase circuit board density. IR HiRel has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

Features

- Surface Mount
- Small Footprint
- Alternative to TO-39 Package
- Hermetically Sealed
- Dynamic dv/dt Rating
- Avalanche Energy Rating
- Simple Drive Requirements
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-6.5	A
I_{D2} @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-4.1	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	-25	
P_D @ T_C = 25°C	Maximum Power Dissipation	25	W
	Linear Derating Factor	0.20	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	165	mJ
I_{AR}	Avalanche Current ①	-6.5	A
E_{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temp.	300 (for 5 s)	
	Weight	0.42 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.10	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	V_{GS} = -10V, I_{D2} = -4.1A ④
		—	—	0.320		V_{GS} = -10V, I_{D1} = -6.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	µA	V_{DS} = -80V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	34.8	nC	I_{D1} = -6.5A
Q_{GS}	Gate-to-Source Charge	—	—	6.8		V_{DS} = -50V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	23.1		V_{GS} = -10V
$t_{d(on)}$	Turn-On Delay Time	—	—	60	ns	V_{DD} = -40V
tr	Rise Time	—	—	140		I_{D1} = -6.5A
$t_{d(off)}$	Turn-Off Delay Time	—	—	140		R_G = 7.5Ω
t_f	Fall Time	—	—	140		V_{GS} = -10V
Ls +L_D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	790	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	340	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	71	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-6.5	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-25		
V_{SD}	Diode Forward Voltage	—	—	-4.3	V	T_J = 25°C,I_S = -6.5A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = -6.5A, V_{DD} ≤ -50V
Q_{rr}	Reverse Recovery Charge	—	—	3.0	µC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.0	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC Board	—	—	19	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -25V, starting T_J = 25°C, Peak I_L = -6.5A

③ I_{SD} ≤ -6.5A, di/dt ≤ -390A/µs, V_{DD} ≤ -100V, T_J ≤ 150°C, Suggested R_G = 7.5 Ω

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

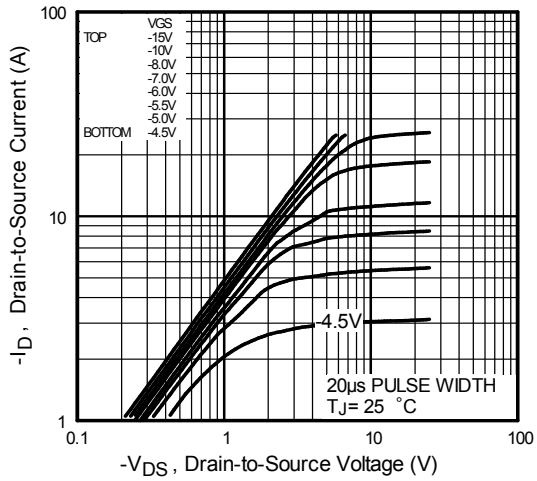


Fig 1. Typical Output Characteristics

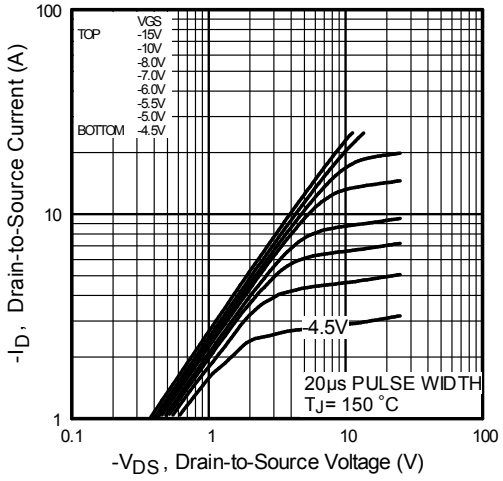


Fig 2. Typical Output Characteristics

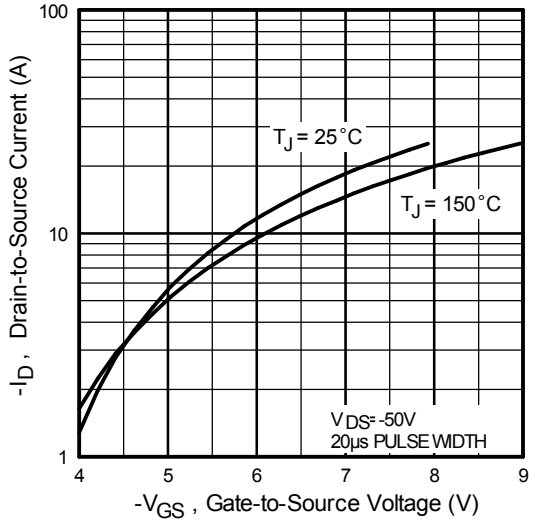


Fig 3. Typical Transfer Characteristics

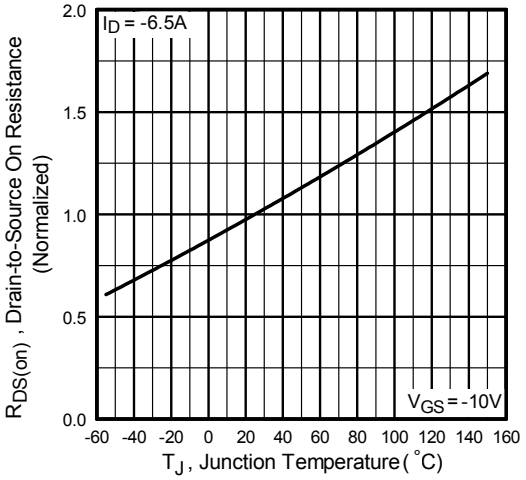


Fig 4. Normalized On-Resistance Vs. Temperature

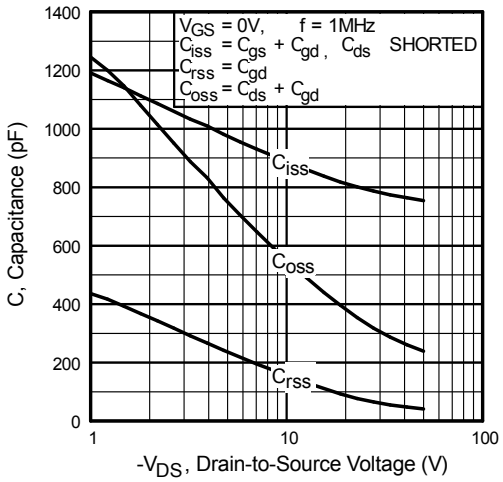


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

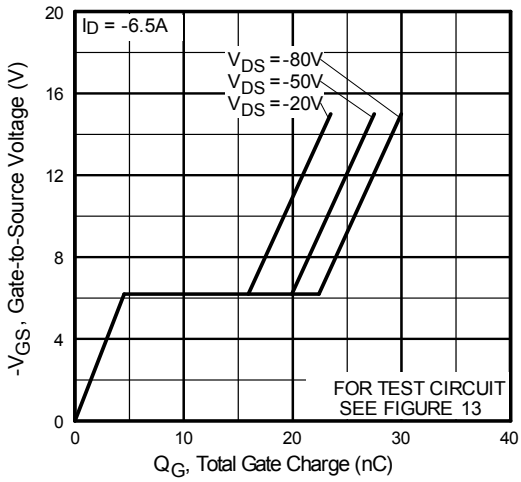


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

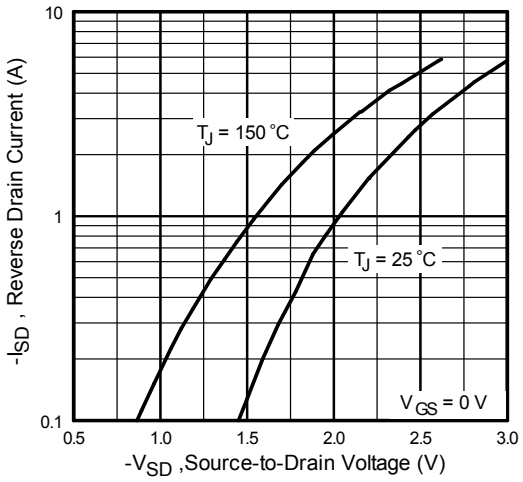


Fig 7. Typical Source-Drain Diode Forward Voltage

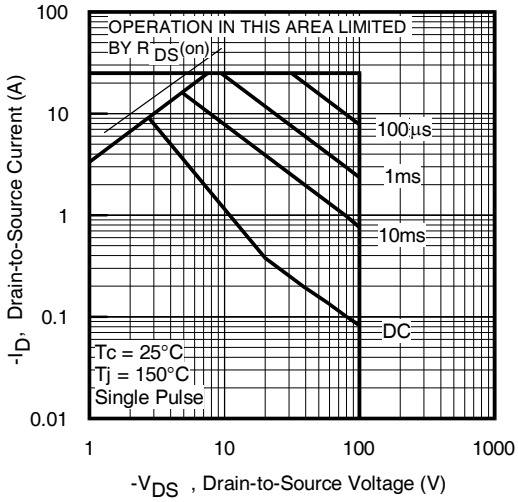


Fig 8. Maximum Safe Operating Area

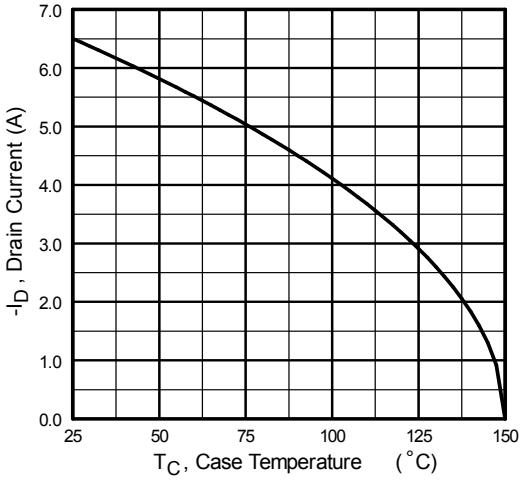


Fig 9. Maximum Drain Current Vs. Case Temperature

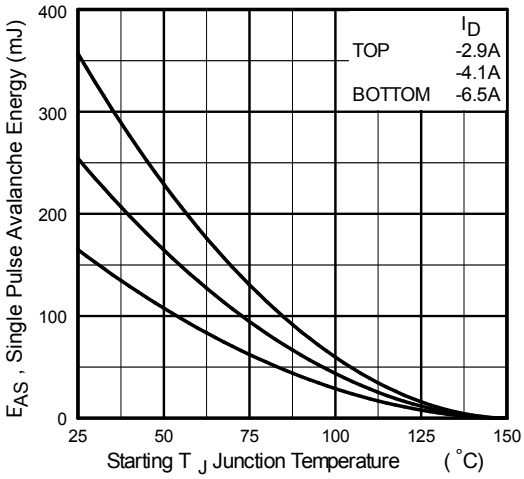


Fig 10. Maximum Avalanche Energy Vs. Drain Current

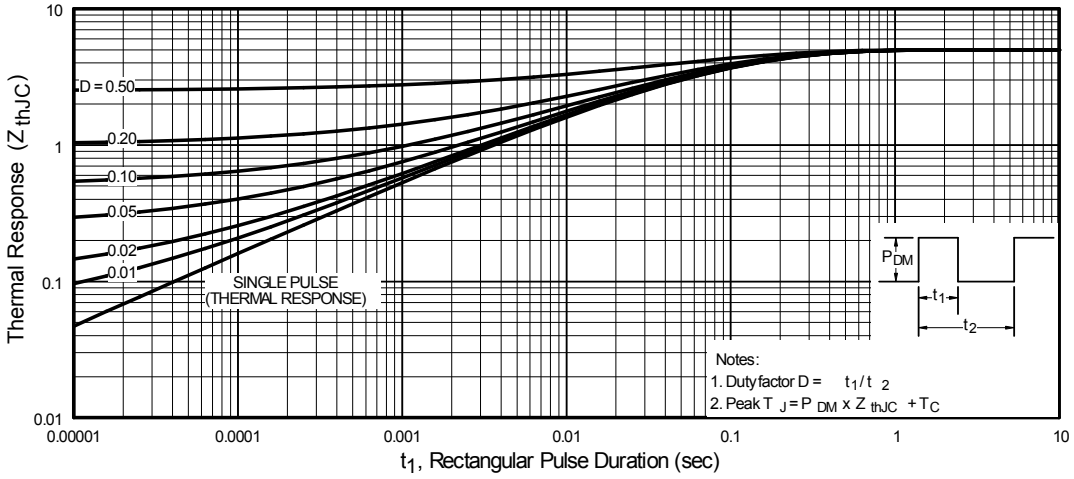


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

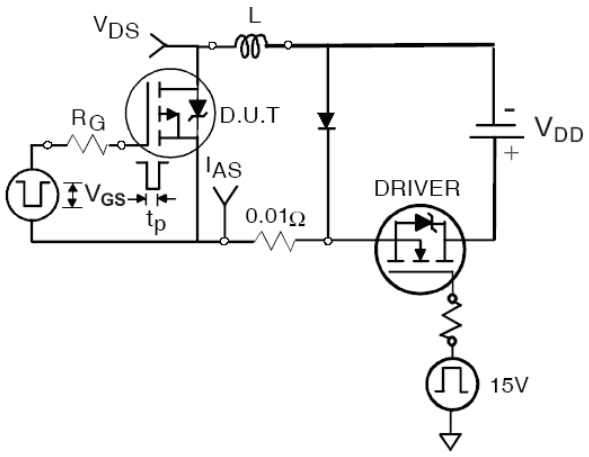


Fig 12a. Unclamped Inductive Test Circuit

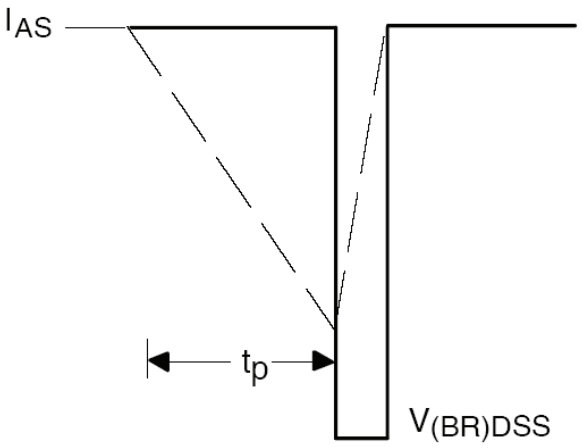


Fig 12b. Unclamped Inductive Waveforms

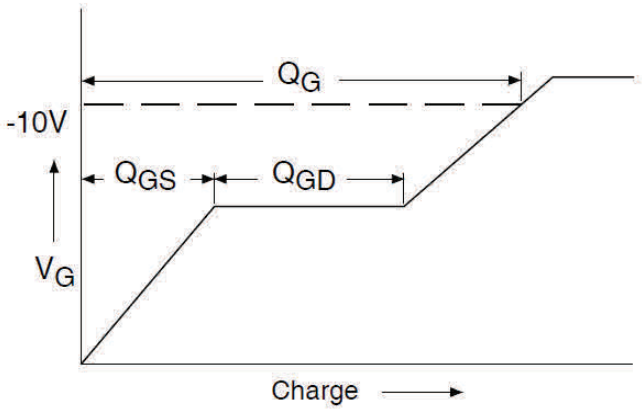


Fig 13a. Gate Charge Waveform

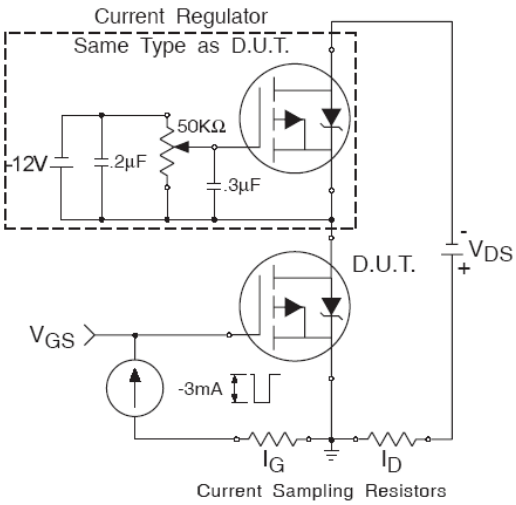


Fig 13b. Gate Charge Test Circuit

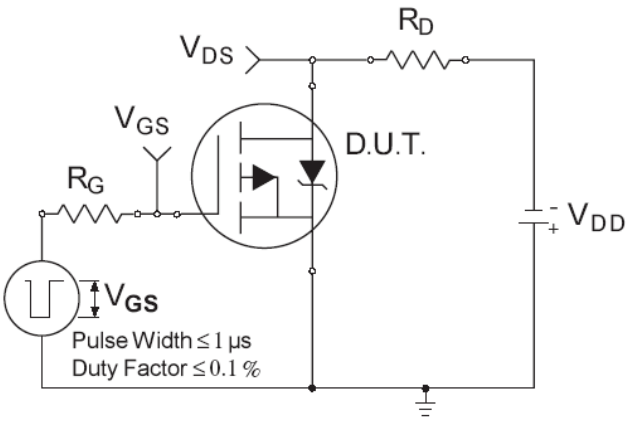


Fig 14a. Switching Time Test Circuit

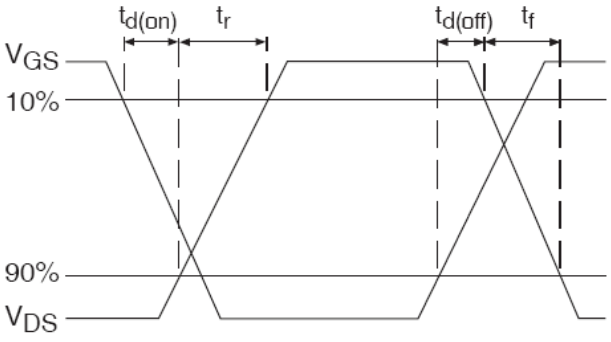
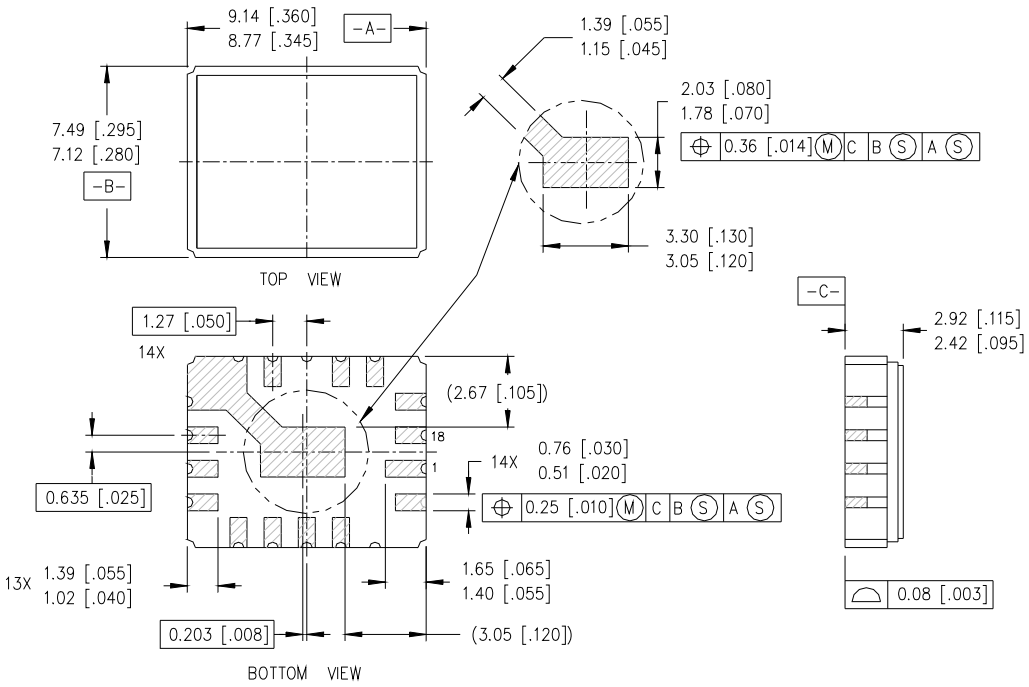
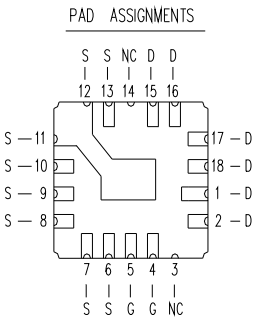


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - LCC-18





LEGEND

G = GATE
D = DRAIN
S = SOURCE
NC = NO CONNECTION

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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