

Typical Applications

- Industrial Motor Drive

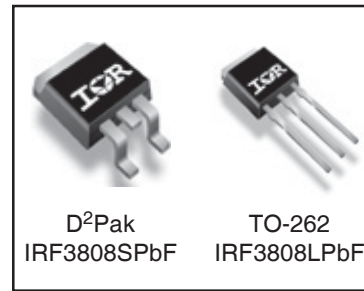
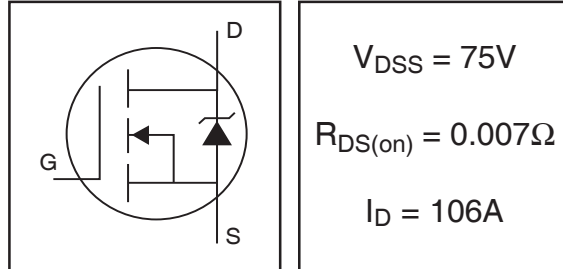
Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

Description

This Advanced Planar Stripe HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, low RθJC, fast switching speed and improved repetitive avalanche rating. This combination makes the design an extremely efficient and reliable choice for use in a wide variety of applications.

HEXFET® Power MOSFET



Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF3808LPbF	TO-262	Tube	50	IRF3808LPbF
		Tube	50	IRF3808SPbF
IRF3808SPbF	D²Pak	Tape and Reel Left	800	IRF3808STRLPbF
		Tape and Reel Right	800	IRF3808STRRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	106	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	75	
I_{DM}	Pulsed Drain Current ①	550	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	430	mJ
I_{AR}	Avalanche Current①	82	A
E_{AR}	Repetitive Avalanche Energy③	See Fig.12a, 12b, 15, 16	mJ
dv/dt	Peak Diode Recovery dv/dt ④	5.5	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}			
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, Steady State)②	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

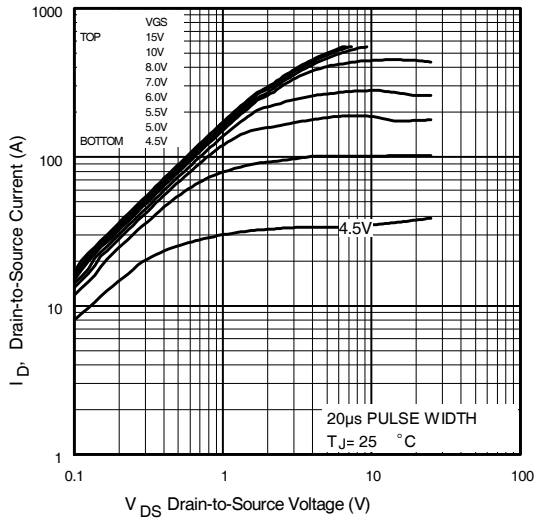
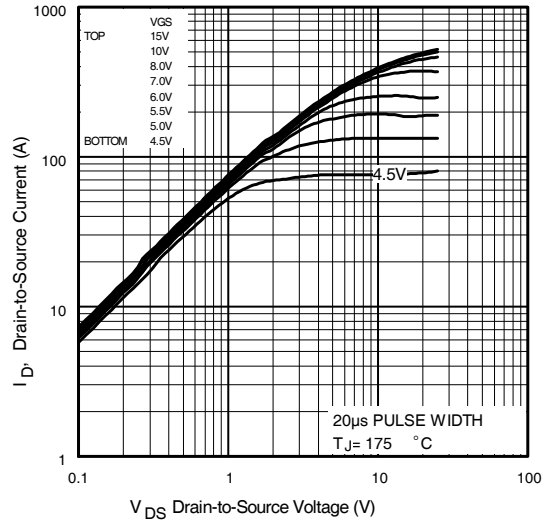
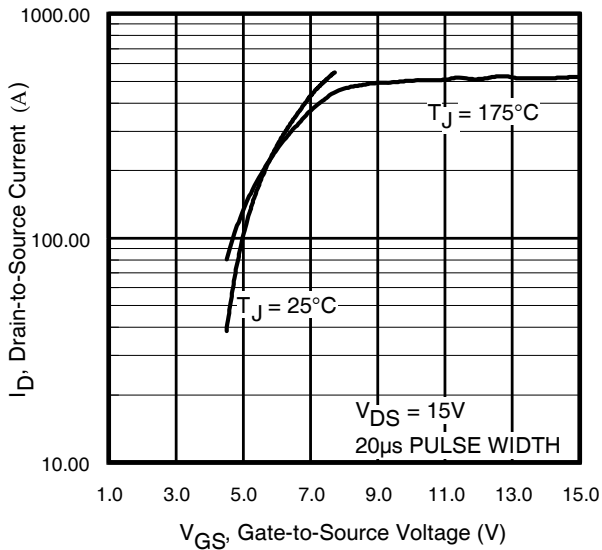
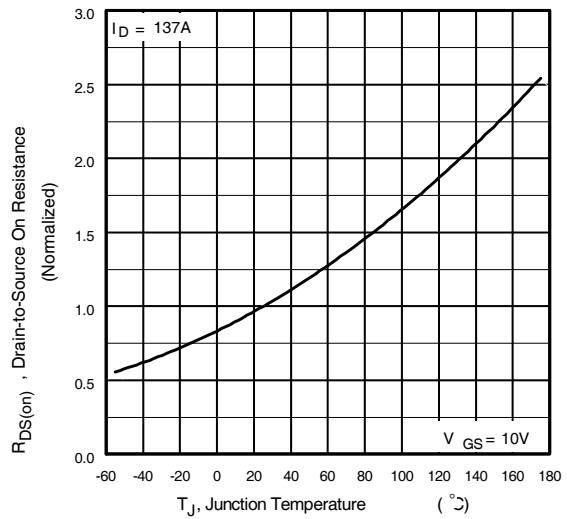
	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.086	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	5.9	7.0	mΩ	V _{GS} = 10V, I _D = 82A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	100	—	—	S	V _{DS} = 25V, I _D = 82A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	150	220	nC	I _D = 82A
Q _{gs}	Gate-to-Source Charge	—	31	47		V _{DS} = 60V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	50	76		V _{GS} = 10V ④
t _{d(on)}	Turn-On Delay Time	—	16	—	ns	V _{DD} = 38V
t _r	Rise Time	—	140	—		I _D = 82A
t _{d(off)}	Turn-Off Delay Time	—	68	—		R _G = 2.5Ω
t _f	Fall Time	—	120	—		V _{GS} = 10V ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	5310	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	890	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	6010	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	570	—		V _{GS} = 0V, V _{DS} = 60V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	1140	—		V _{GS} = 0V, V _{DS} = 0V to 60V

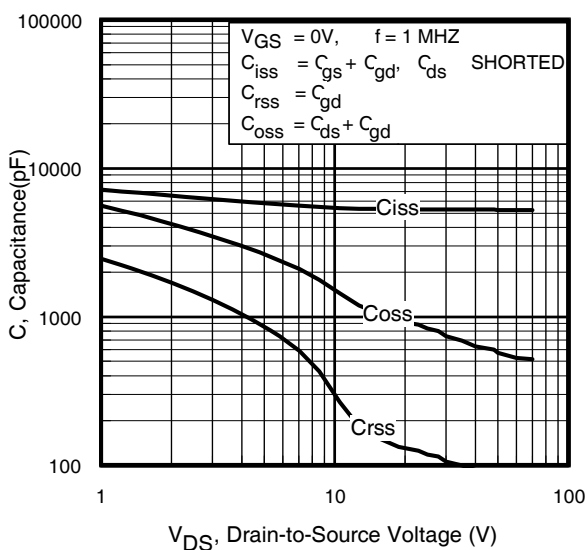
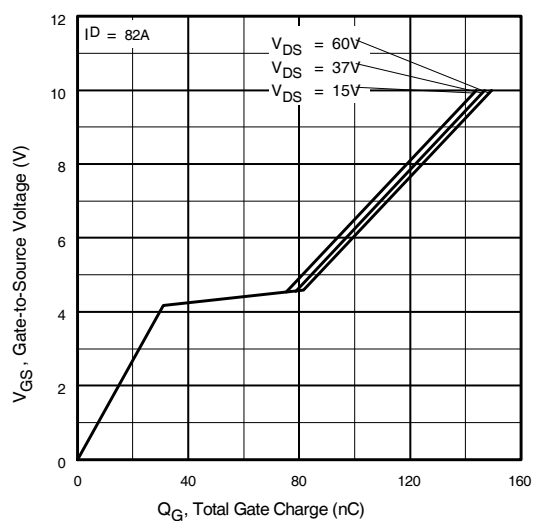
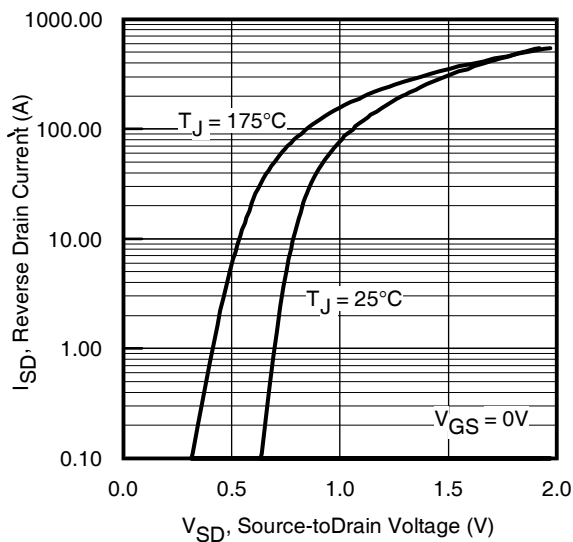
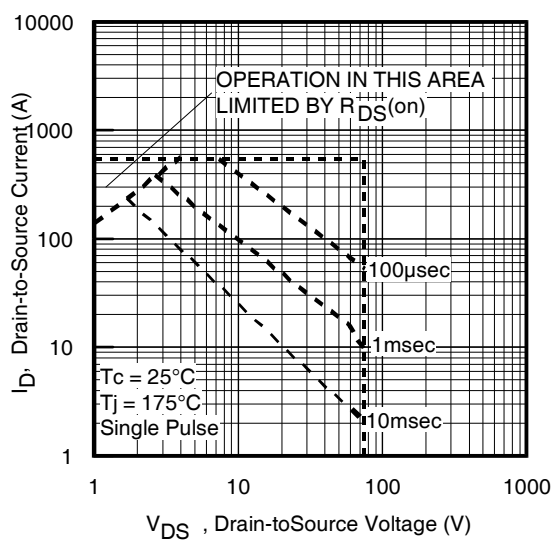
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	106	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	550		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 82A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	93	140	ns	T _J = 25°C, I _F = 82A
Q _{rr}	Reverse Recovery Charge	—	340	510	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T_J = 25°C, L = 0.130mH
R_G = 25Ω, I_{AS} = 82A. (See Figure 12).
- ③ I_{SD} ≤ 82A, di/dt ≤ 310A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance Vs. Temperature


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

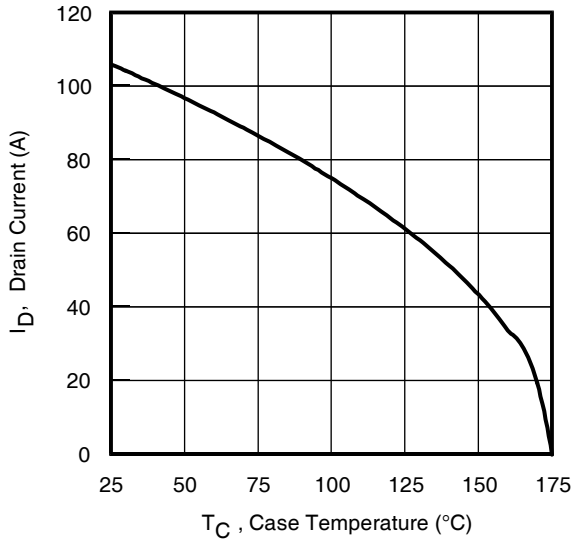


Fig 9. Maximum Drain Current Vs. Case Temperature

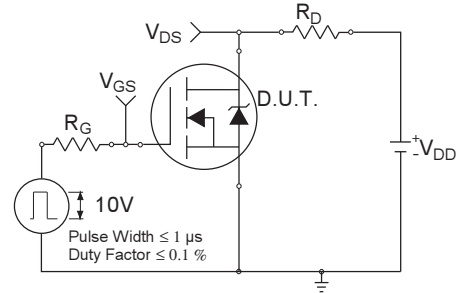


Fig 10a. Switching Time Test Circuit

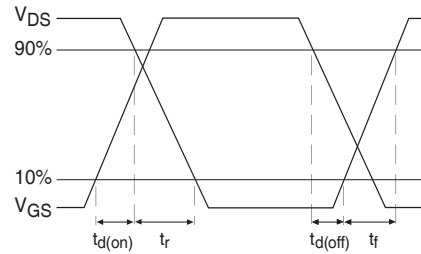


Fig 10b. Switching Time Waveforms

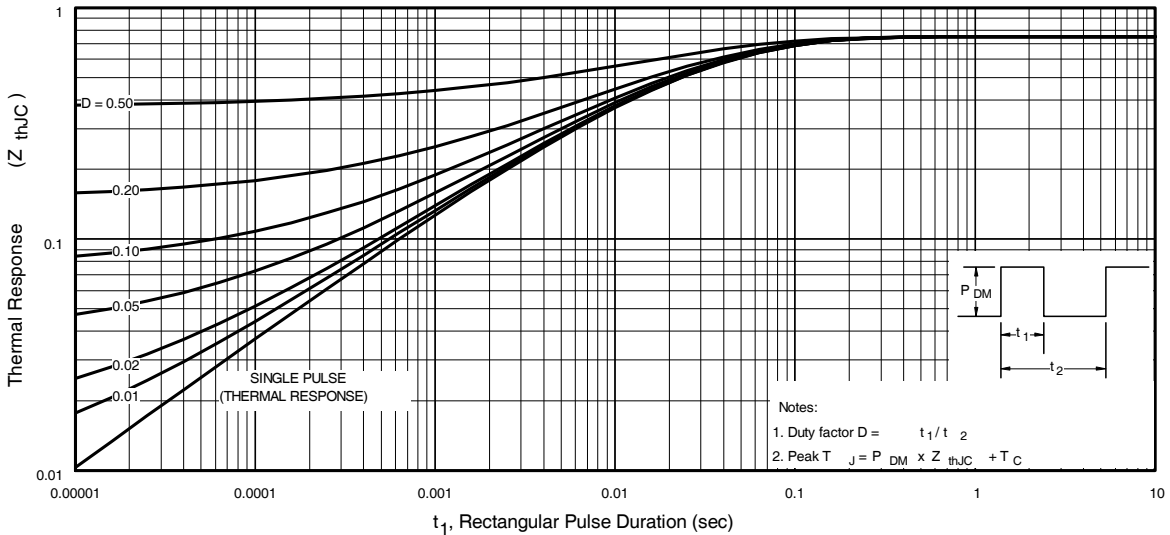
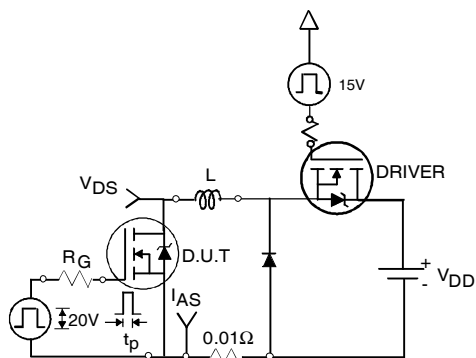
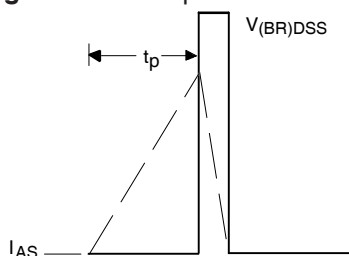
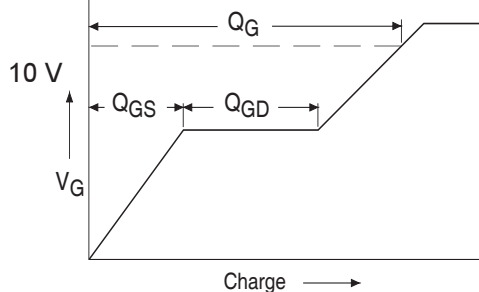
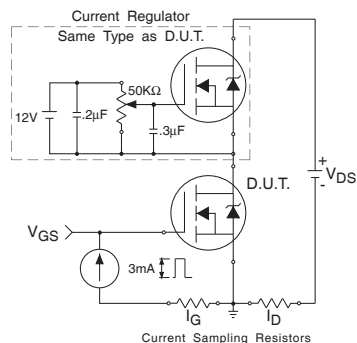
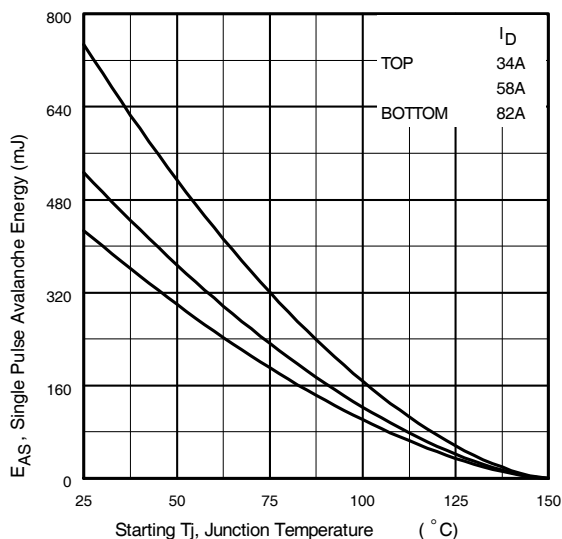
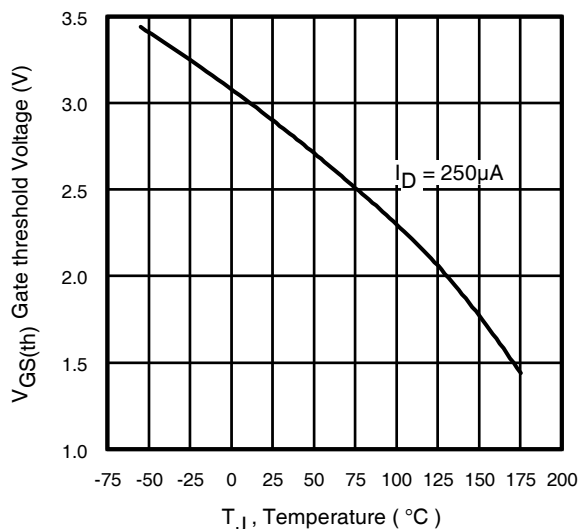
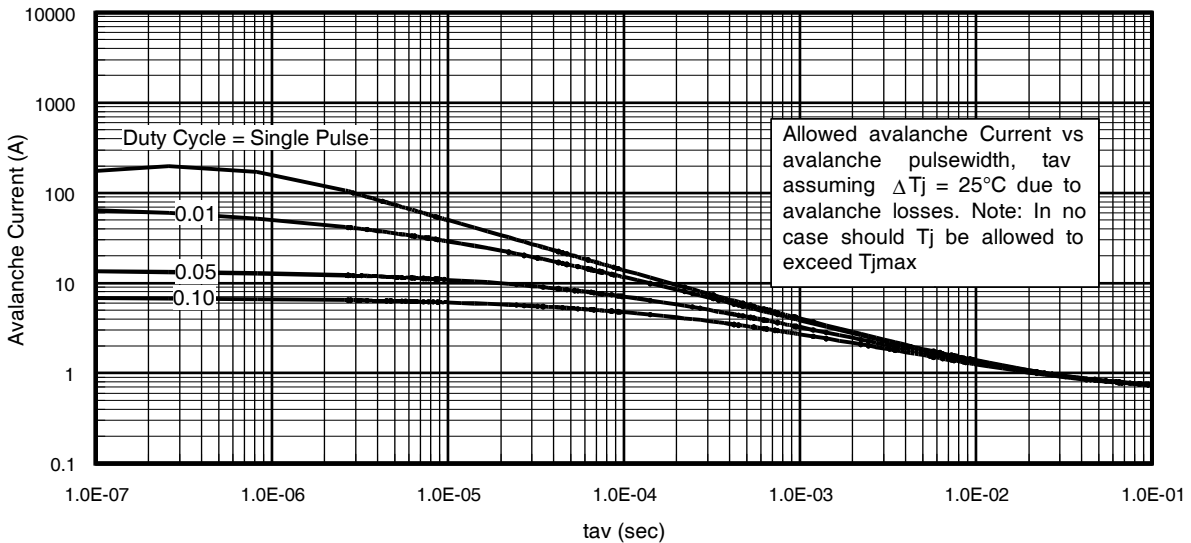
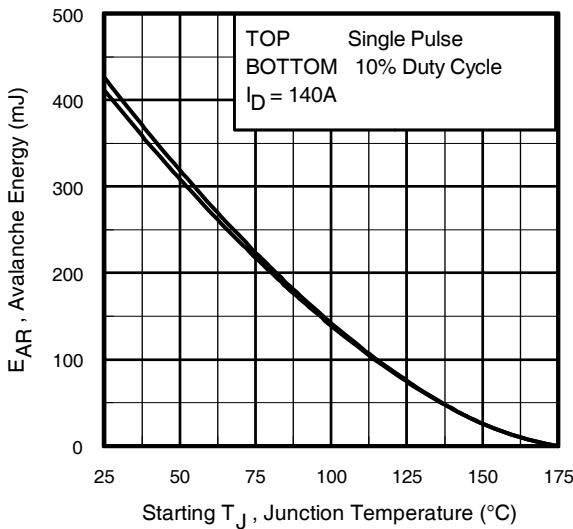


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 14. Threshold Voltage Vs. Temperature

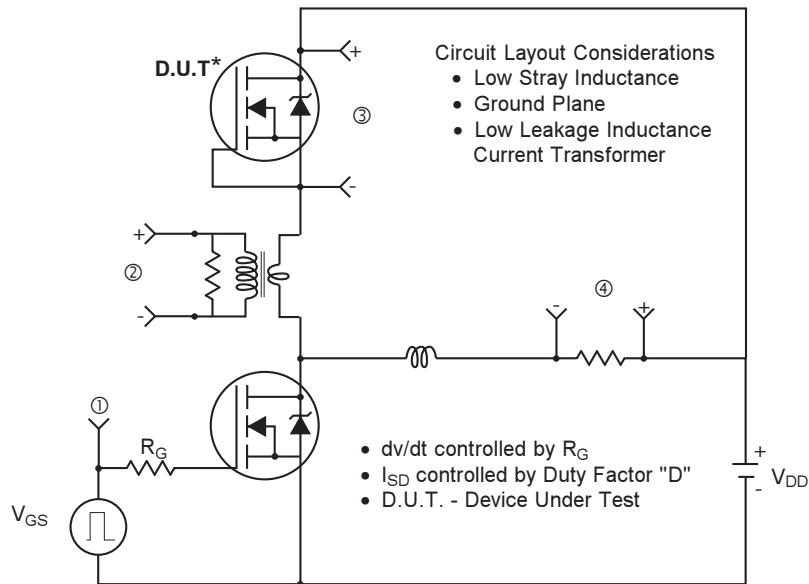

Fig 15. Typical Avalanche Current Vs.Pulsewidth

Fig 16. Maximum Avalanche Energy Vs. Temperature
Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

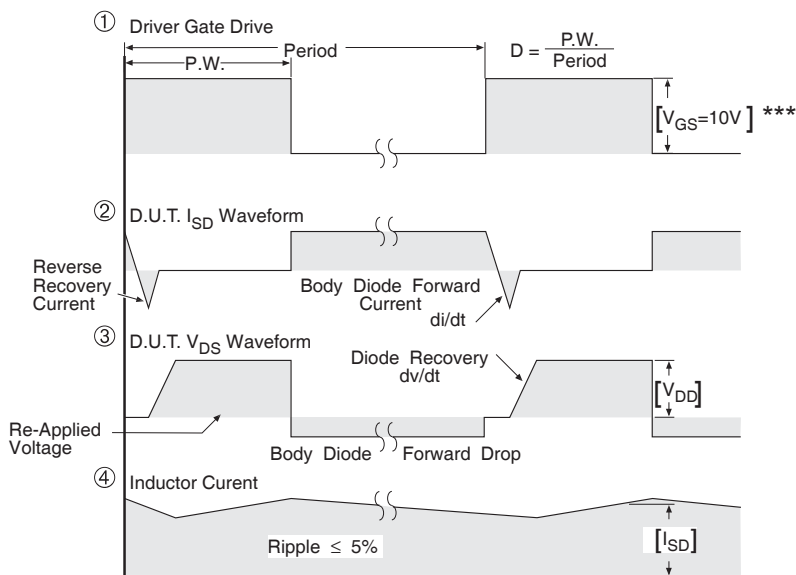
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit


* Reverse Polarity of D.U.T for P-Channel

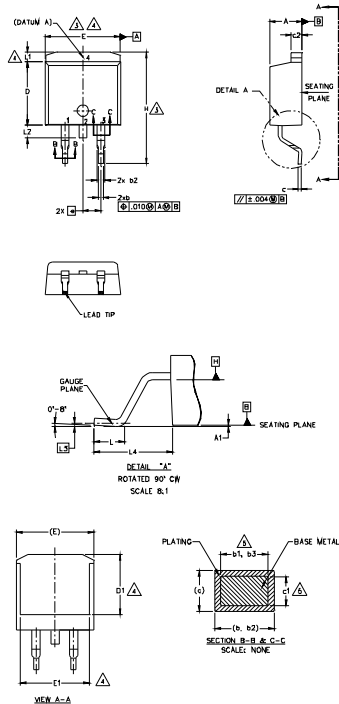


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET[®] power MOSFETs

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



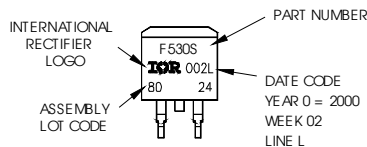
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	5
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	4
L1	-	1.65	-	.066	
L2	-	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

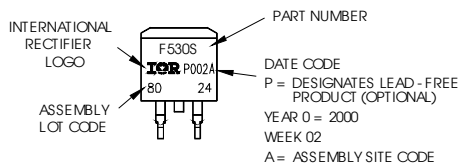
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"



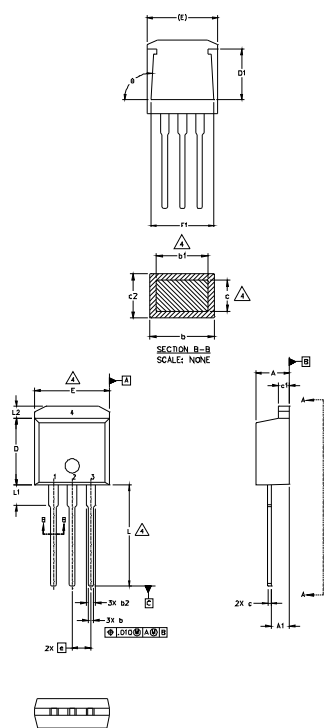
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33	10.67	.210	.420	3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

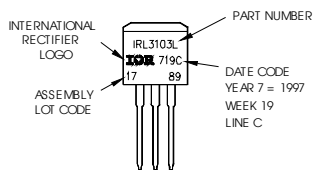
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT

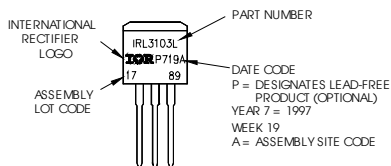
- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
 Note: "P" in assembly line
 position indicates "Lead-Free"

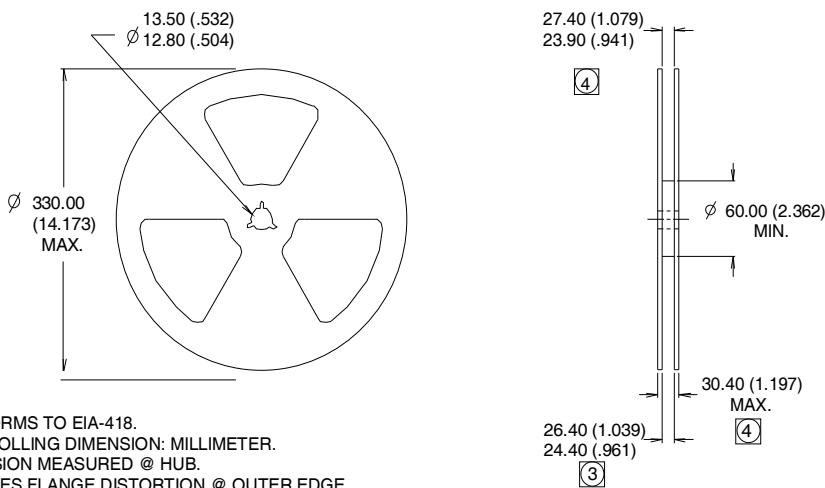
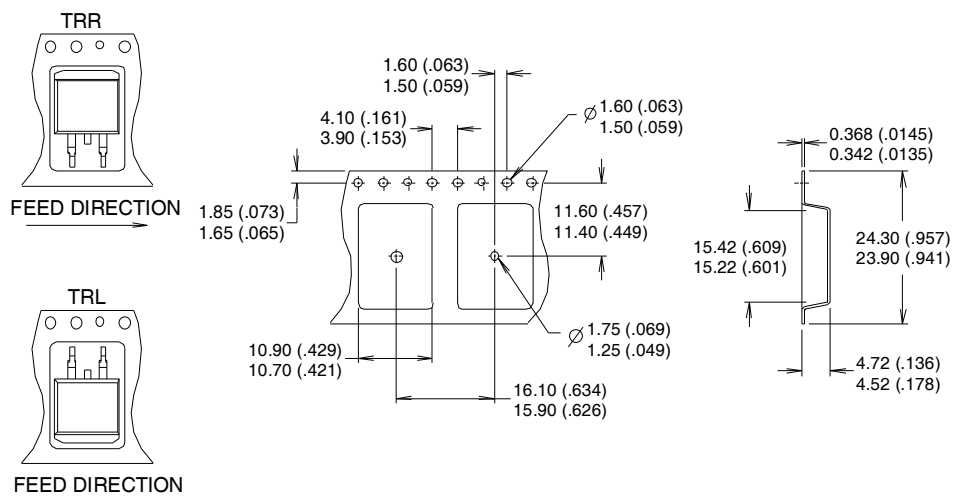


OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak Tape & Reel Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	TO-262 PAK	N/A
	D2-PAK	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

^{††} Applicable version of JEDEC standard at the time of product release

Revision History

Date	Comments
11/1/2013	<ul style="list-style-type: none"> • Updated datasheet with New IR corporate template • Removed note6 because update package ID from "75A" to "106A"-page 1 & 2 • Added Odering information table-page 1 • Corrected fig9-page 5 • Added Qualification information table-page 12

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