

Automotive Grade AUIRS2302S(TR) HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 5V to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High-side output in phase with IN input
- Logic and power ground $\pm 5V$ offset
- Internal 540ns deadtime
- Lower di/dt gate driver for better noise immunity
- Shutdown input turns off both channels
- Leadfree, RoHS compliant
- Automotive qualified*

Typical Applications

- Braking Pump
- Compressor
- Electric Stability program
- power steering
- MOSFET and IGBT gate drivers

Product Summary

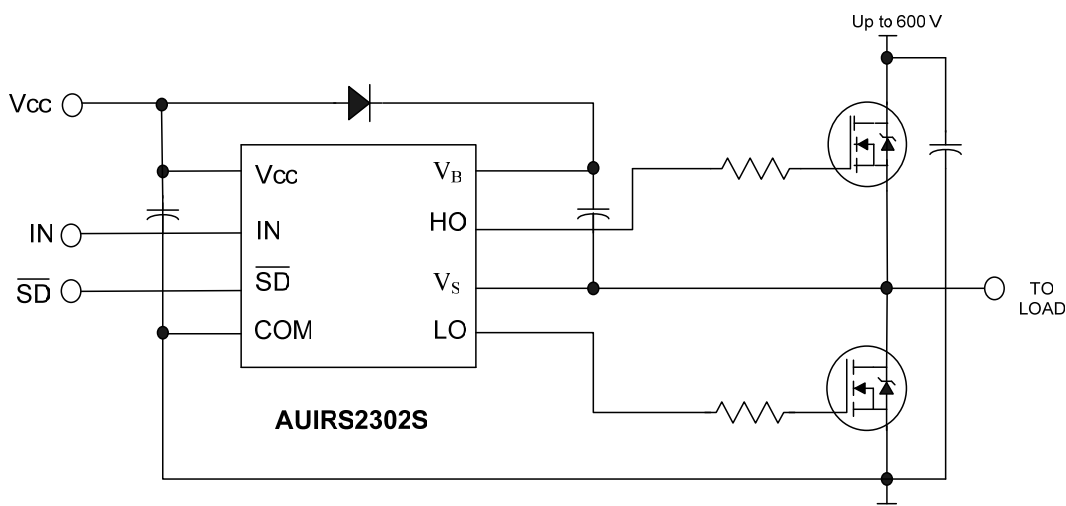
| | |
|---|---------------|
| V_{OFFSET} | 600V Max |
| V_{OUT} | 5V – 20V |
| $I_{\text{o+}} \& I_{\text{o-}}$ (min) | 120mA / 250mA |
| $t_{\text{ON}} \& t_{\text{OFF}}$ (typical) | 720ns / 250ns |
| Delay Matching (max.) | 60ns |

Package Options



8-Lead SOIC

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

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Description

The AUIRS2302S is a high voltage, high speed power MOSFET and IGBT driver with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

Feature Comparison

| Part Numbers | Input Logic | Cross-conduction prevention logic | Deadtime (ns) | Ground Pins | t _{on} /t _{off} (ns) |
|--------------|------------------------------|-----------------------------------|-------------------------|----------------------|--|
| 2106/2301 | HIN/LIN | no | none | COM | 220/200 |
| 21064 | | | | V _{SS} /COM | |
| 2108 | HIN/ $\overline{\text{LIN}}$ | yes | Internal 540 | COM | 220/200 |
| 21084 | | | Programmable 540 – 5000 | V _{SS} /COM | |
| 2109/2302 | IN/ $\overline{\text{SD}}$ | yes | Internal 540 | COM | 720/250 |
| 21094 | | | Programmable 540 - 5000 | V _{SS} /COM | |
| 2304 | HIN/LIN | yes | Internal 100 | COM | 160/140 |

Qualification Information[†]

| | | | |
|-----------------------------------|----------------------|---|--|
| Qualification Level | | Automotive (per AEC-Q100 ^{††}) | |
| | | Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | SOIC8 | MSL3 ^{†††} 260°C (per IPC/JEDEC J-STD-020) |
| ESD | Machine Model | Class M2 (per AEC-Q100-003) | |
| | Human Body Model | Class H1C (per AEC-Q100-002) | |
| | Charged Device Model | Class C5 (per AEC-Q100-011) | |
| IC Latch-Up Test | | Class II, Level A (per AEC-Q100-004) | |
| RoHS Compliant | | Yes | |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Condition” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units |
|------------|---|-------------|----------------|--------------------|
| V_B | High-side floating absolute voltage | -0.3 | 625 | V |
| V_S | High-side floating supply offset voltage | $V_B - 25$ | $V_B + 0.3$ | |
| V_{HO} | High-side floating output voltage | $V_S - 0.3$ | $V_B + 0.3$ | |
| V_{CC} | Low-side and logic fixed supply voltage | -0.3 | 25 | |
| V_{LO} | Low-side output voltage | -0.3 | $V_{CC} + 0.3$ | |
| V_{IN} | Logic input voltage (IN & \overline{SD}) | COM -0.3 | $V_{CC} + 0.3$ | |
| dV_S/dt | Allowable offset supply voltage transient | — | 50 | V/ns |
| P_D | Package power dissipation @ $T_A \leq 25^\circ\text{C}$ | — | 0.625 | W |
| R_{thJA} | Thermal resistance, junction to ambient | — | 200 | $^\circ\text{C/W}$ |
| T_J | Junction temperature | — | 150 | $^\circ\text{C}$ |
| T_S | Storage temperature | -50 | 150 | |
| T_L | Lead temperature (soldering, 10 seconds) | — | 300 | |

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units |
|----------|---|-----------|------------|------------------|
| V_B | High-side floating supply absolute voltage | $V_S + 5$ | $V_S + 20$ | V |
| V_S | High-side floating supply offset voltage | † 1 | 600 | |
| V_{HO} | High-side floating output voltage | V_S | V_B | |
| V_{CC} | Low-side and logic fixed supply voltage | 5 | 20 | |
| V_{LO} | Low-side output voltage | 0 | V_{CC} | |
| V_{IN} | Logic input voltage (IN & \overline{SD}) | COM | V_{CC} | |
| T_A | Ambient temperature | -40 | 150 | $^\circ\text{C}$ |

†: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$.
(Please refer to the Design Tip DT97 -3 for more details).

Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of V_{BIAS} (V_{CC} or V_{BS}) = 15V. The V_{IN} , V_{TH} parameters are referenced to COM and are applicable to all logic input leads: IN and \overline{SD} . The V_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|----------------------------|--|------|-----|-----|---------------|---|
| V_{IH} | Logic "1" input voltage for HO & logic "0" for LO | 2.5 | — | — | V | $V_{CC} = 10\text{V to } 20\text{V}$ |
| V_{IL} | Logic "0" input voltage for HO & logic "1" for LO | — | — | 0.8 | | |
| $V_{SD,TH+}$ | \overline{SD} input positive going threshold | 2.5 | — | — | | |
| $V_{SD,TH-}$ | \overline{SD} input negative going threshold | — | — | 0.8 | | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | — | — | 0.2 | | $I_O = 2\text{mA}$ |
| V_{OL} | Low level output voltage, V_O | — | — | 0.1 | | |
| I_{LK} | Offset supply leakage current | — | — | 50 | μA | $V_B = V_S = 600\text{V}$ |
| I_{QBS} | Quiescent V_{BS} supply current | 20 | 180 | 300 | | $V_{IN} = 0\text{V or } 5\text{V}$ |
| I_{QCC} | Quiescent V_{CC} supply current | 0.4 | 1.0 | 1.6 | mA | |
| I_{IN+} | Logic "1" input bias current | — | 5 | 20 | μA | $V_{IN} = 5\text{V}, \overline{SD} = 0\text{V}$ |
| I_{IN-} | Logic "0" input bias current | — | — | 5 | | $V_{IN} = 0\text{V}, \overline{SD} = 5\text{V}$ |
| V_{CCUV+} V_{BSUV+} | V_{CC} and V_{BS} supply undervoltage positive going threshold | 3 | 4.1 | 5.2 | V | |
| V_{CCUV-} V_{BSUV-} | V_{CC} and V_{BS} supply undervoltage negative going threshold | 2.8 | 3.8 | 4.8 | | |
| V_{CCUVH} V_{BSUVH} | Hysteresis | 0.05 | 0.3 | — | | |
| I_{O+} | Output high short circuit pulsed current ^(†) | 120 | 200 | — | mA | $V_O = 0\text{V},$ $PW \leq 10\mu\text{s}$ |
| I_{O-} | Output low short circuit pulsed current ^(†) | 250 | 350 | — | | $V_O = 15\text{V},$ $PW \leq 10\mu\text{s}$ |

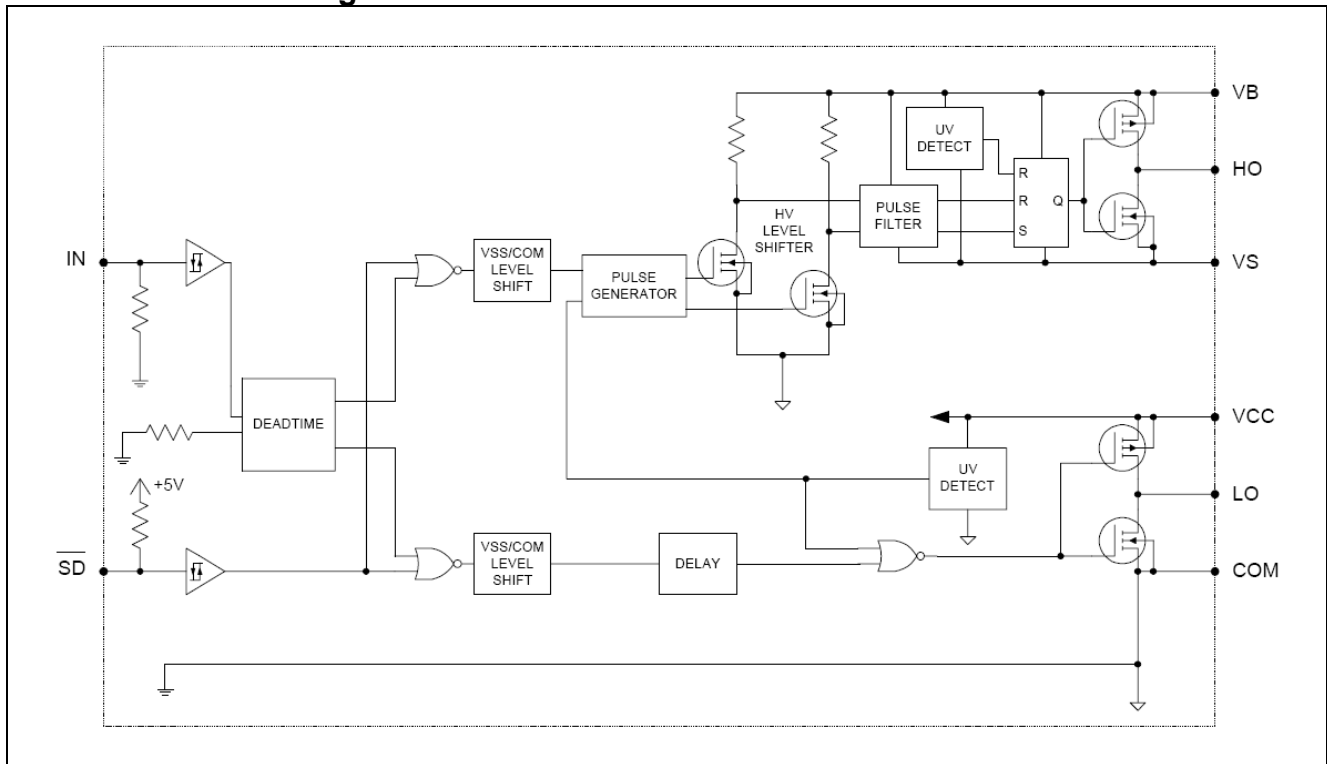
(†) Guaranteed by design

Dynamic Electrical Characteristics

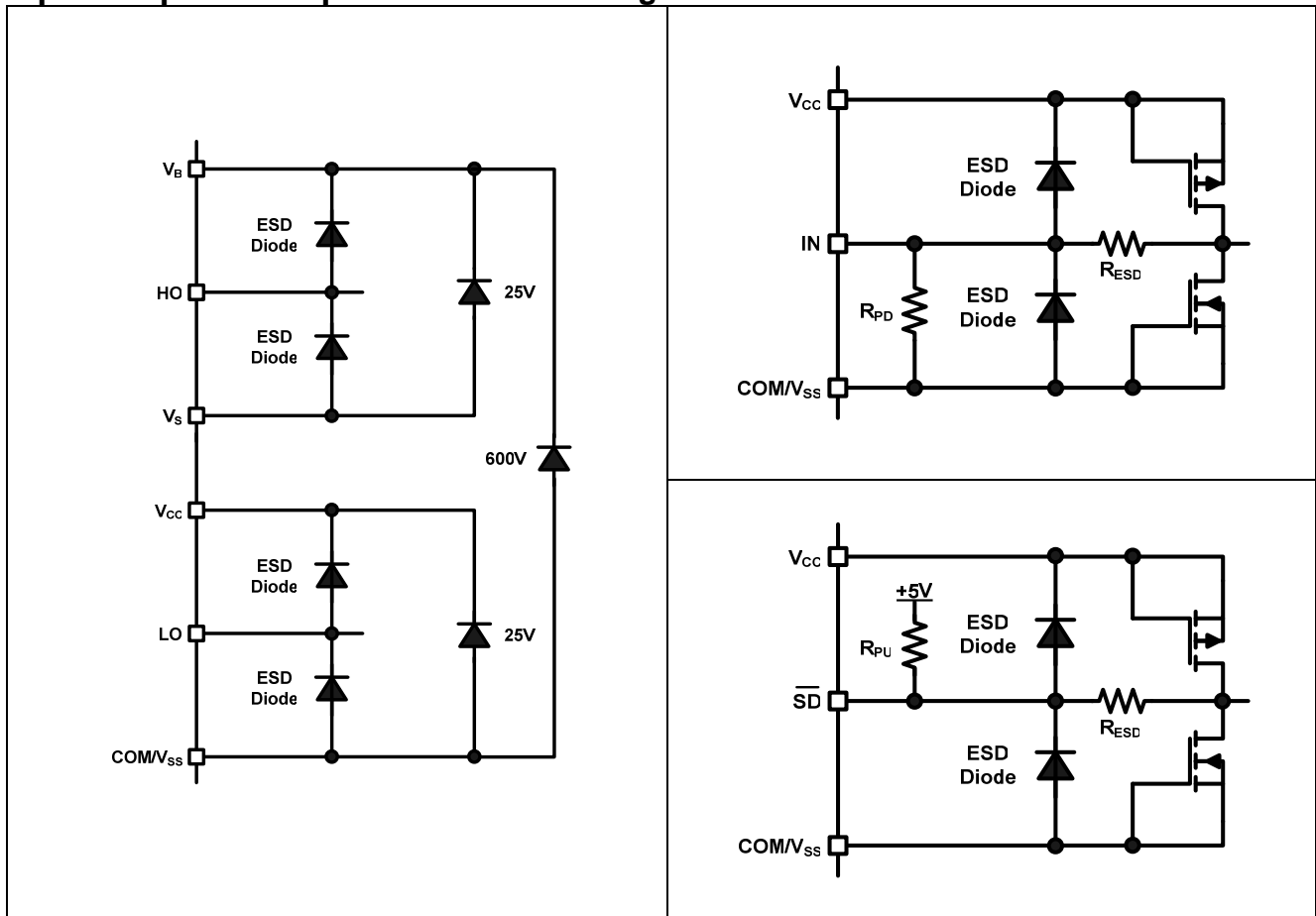
Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of V_{BIAS} (V_{CC} , V_{BS}) = 15V, $CL = 1000$ pF. The dynamic electrical characteristics are measured using the test definitions shown in Figure 2.

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|-----------|---|-----|-----|-----|-------|-----------------------------------|
| t_{on} | Turn-on propagation delay | 550 | 720 | 950 | ns | $V_S = 0\text{V}$ |
| t_{off} | Turn-off propagation delay | — | 250 | 300 | | $V_S = 0\text{V or } 600\text{V}$ |
| t_{sd} | Shutdown propagation delay | — | 240 | 280 | | |
| MT | Delay matching, HS & LS turn-on/off | — | 0 | 50 | | |
| t_r | Turn-on rise time | — | 100 | 220 | | $V_S = 0\text{V}$ |
| t_f | Turn-off fall time | — | 25 | 80 | | |
| DT | Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO}) | 300 | 440 | 580 | | |
| MDT | Delay matching = $DT_{LO-HO} - DT_{HO-LO}$ | — | 0 | 60 | | |

Functional Block Diagram: AUIRS2302S



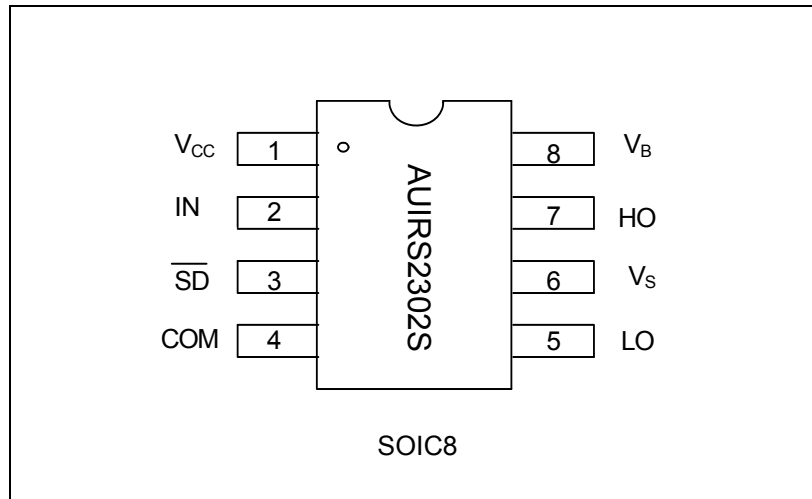
Input/Output Pin Equivalent Circuit Diagrams:



Lead Definitions:

| Symbol | Description |
|-----------------|---|
| V_{CC} | Low-side and logic fixed supply |
| IN | Logic input for high and low side gate driver outputs (HO and LO), in phase with HO |
| \overline{SD} | Logic input for shutdown |
| COM | Low-side return |
| LO | Low-side gate drive output |
| V_S | High-side floating supply return |
| HO | High-side gate drive output |
| V_B | High-side floating supply |

Lead Assignments



Application Information and Additional Details

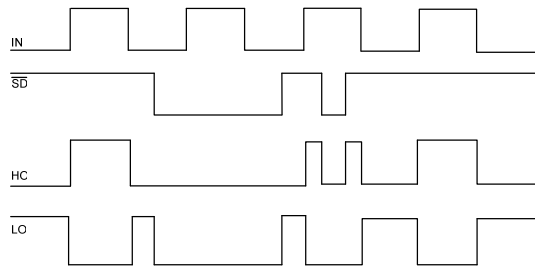


Figure 1: Input/Output Timing Diagram

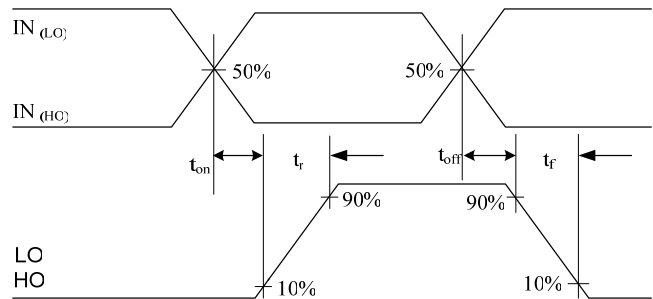


Figure 2: Switching Time Waveform Definitions

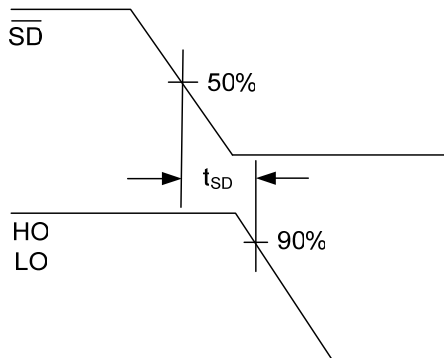


Figure 3: Delay Matching Waveform Definitions

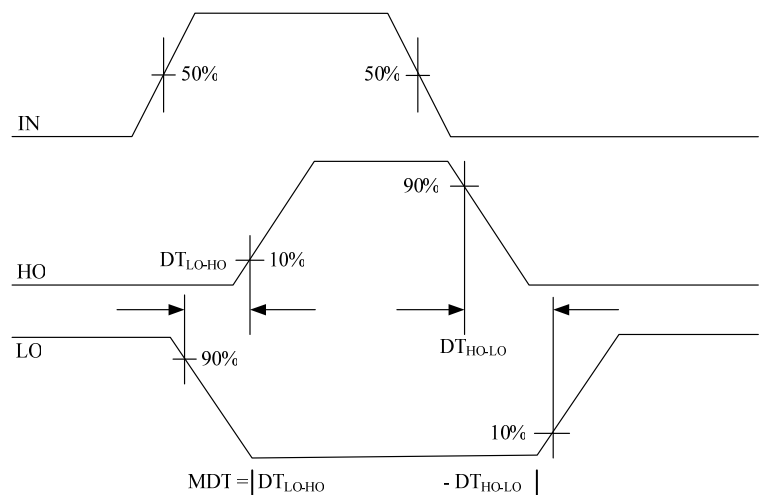


Figure 4: Deadtime Waveform Definitions

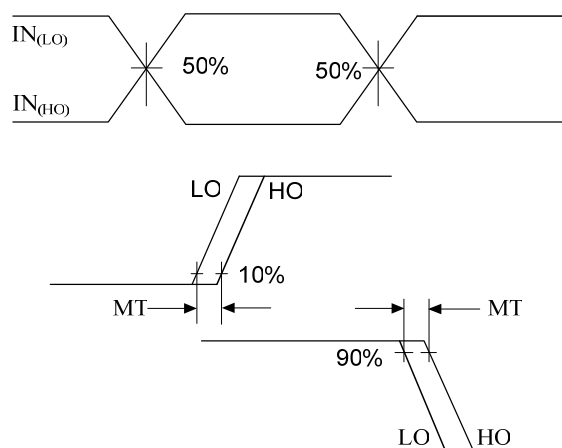


Figure 5: Delay Matching Waveform Definitions

Tolerability to Negative VS Transients

The AUIRS2302S has been seen to withstand negative V_s transient conditions on the order of -25V for a period of 100 ns (V_{BIAS} (V_{CC} , V_{BS}) = 15V and $T_A = 25^\circ\text{C}$).

An illustration of the AUIRS2302S performance can be seen in Figure 6.

Even though the AUIRS2302S have been shown able to handle these negative V_s transient conditions, it is highly recommended that the circuit designer always limit the negative V_s transients as much as possible by careful PCB layout and component use.

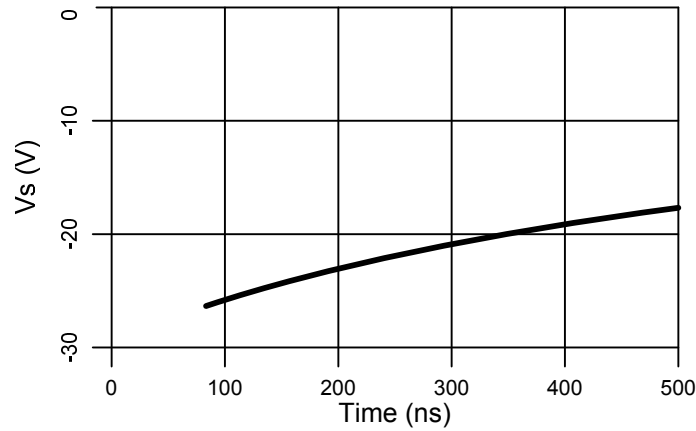


Figure 6: -Vs Transient results

Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2302S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

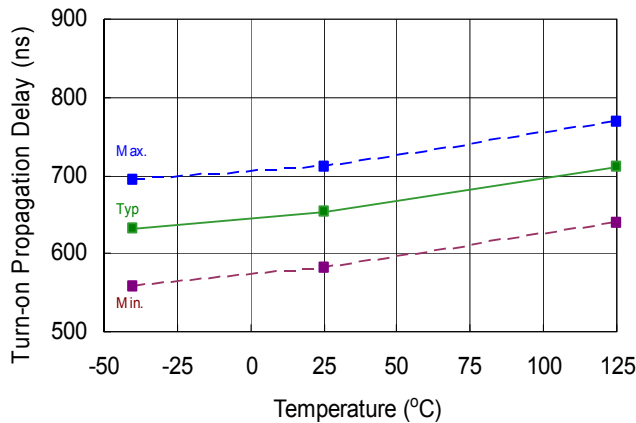


Figure 7. Turn-On Time vs. Temperature

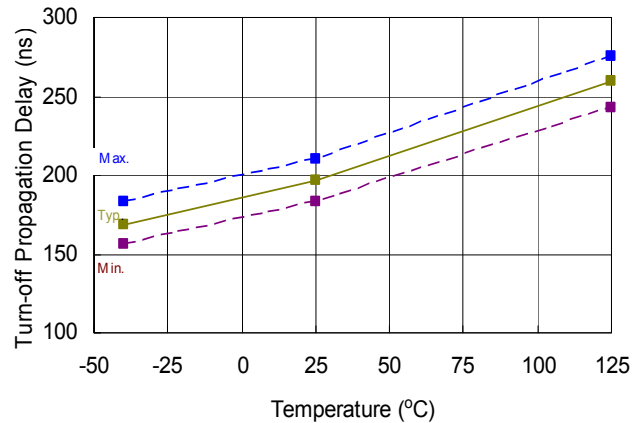


Figure 8. Turn-Off Time vs. Temperature

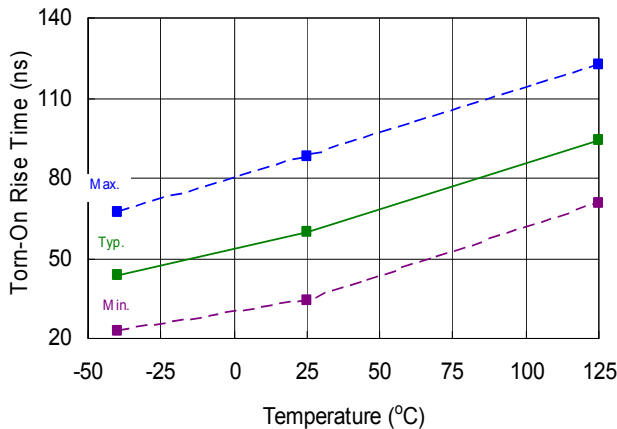


Figure 9. Turn-On Rise Time vs. Temperature

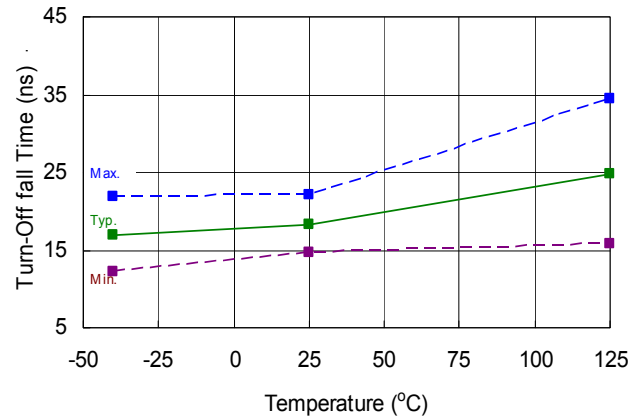


Figure 10. Turn-Off Fall Time vs. Temperature

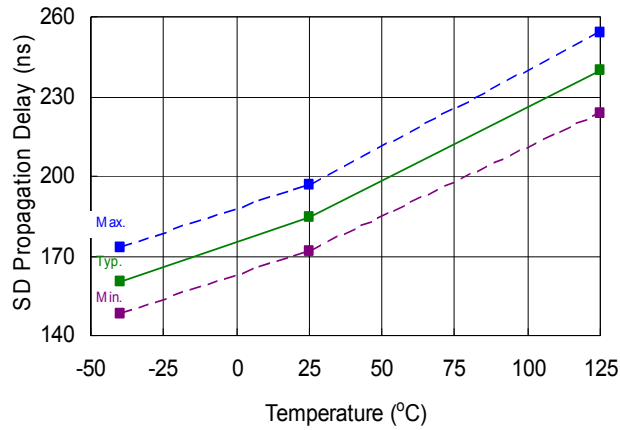


Figure 11. Shutdown Time vs. Temperature

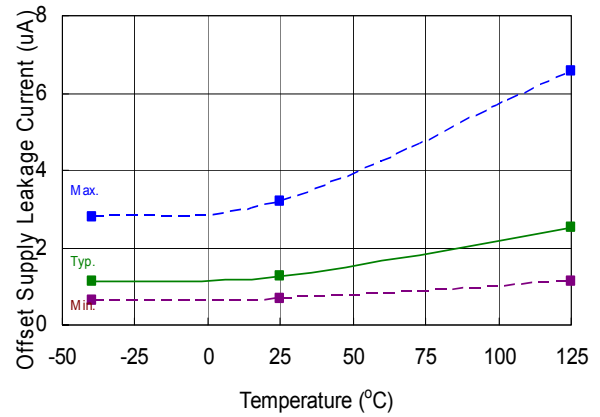


Figure 12. Offset Supply Current vs. Temperature

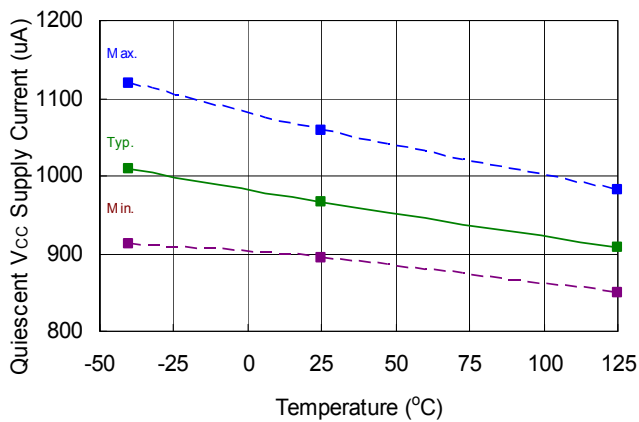


Figure 13. V_{CC} Supply Current vs. Temperature

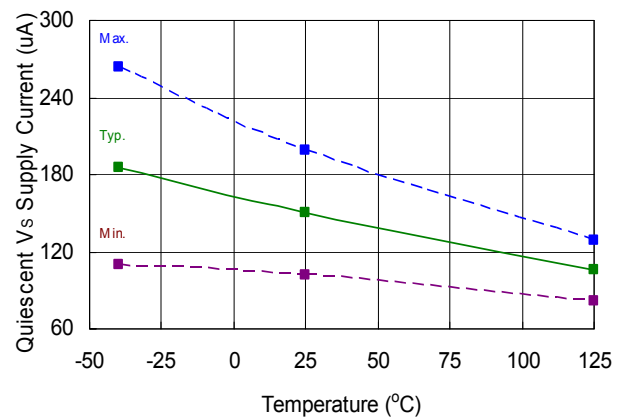


Figure 14. V_{BS} Supply Current vs. Temperature

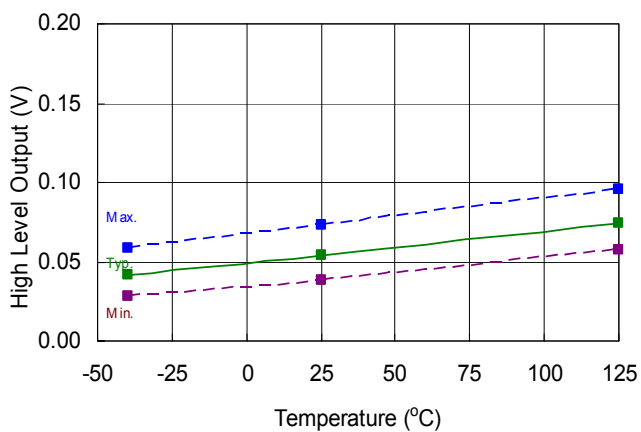


Figure 15. High Level Output Voltage vs. Temperature
(I_o = 2mA)

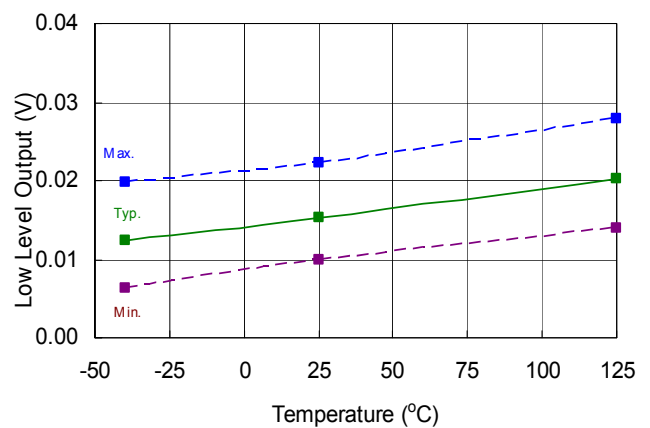


Figure 16. Low Level Output Voltage vs. Temperature
(I_o = 2mA)

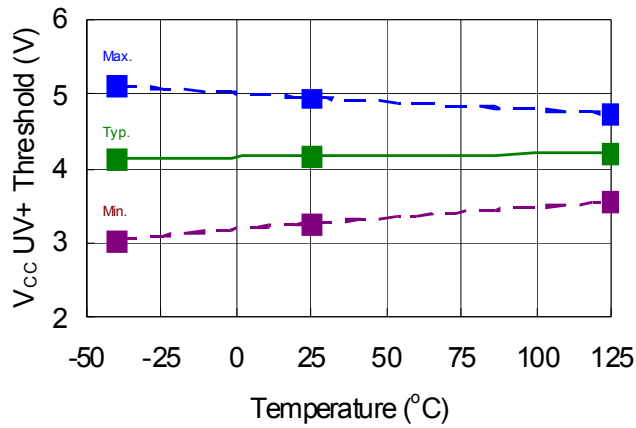


Figure 17. V_{CC} UV+ Threshold Voltage vs. Temperature

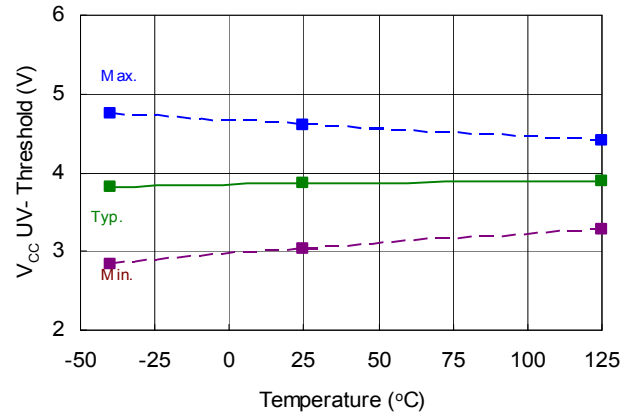


Figure 18. V_{BS} UV- Threshold Voltage vs. Temperature

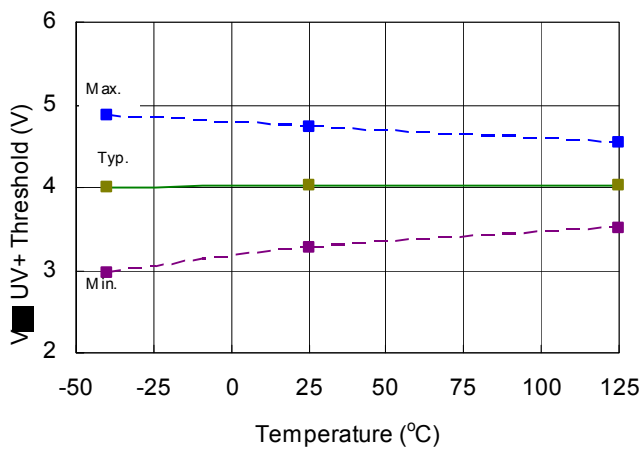


Figure 19. V_{BS} UV+ Threshold Voltage vs. Temperature

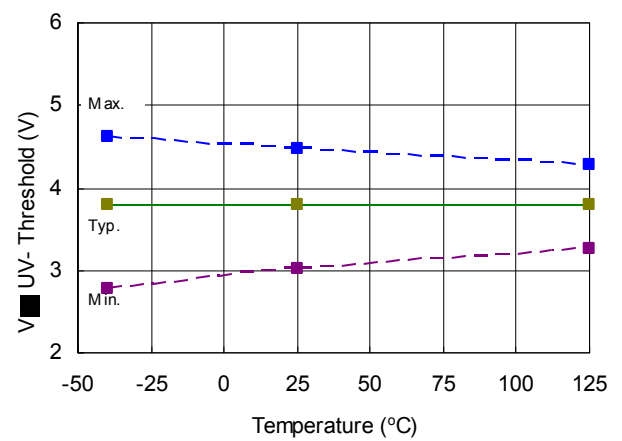
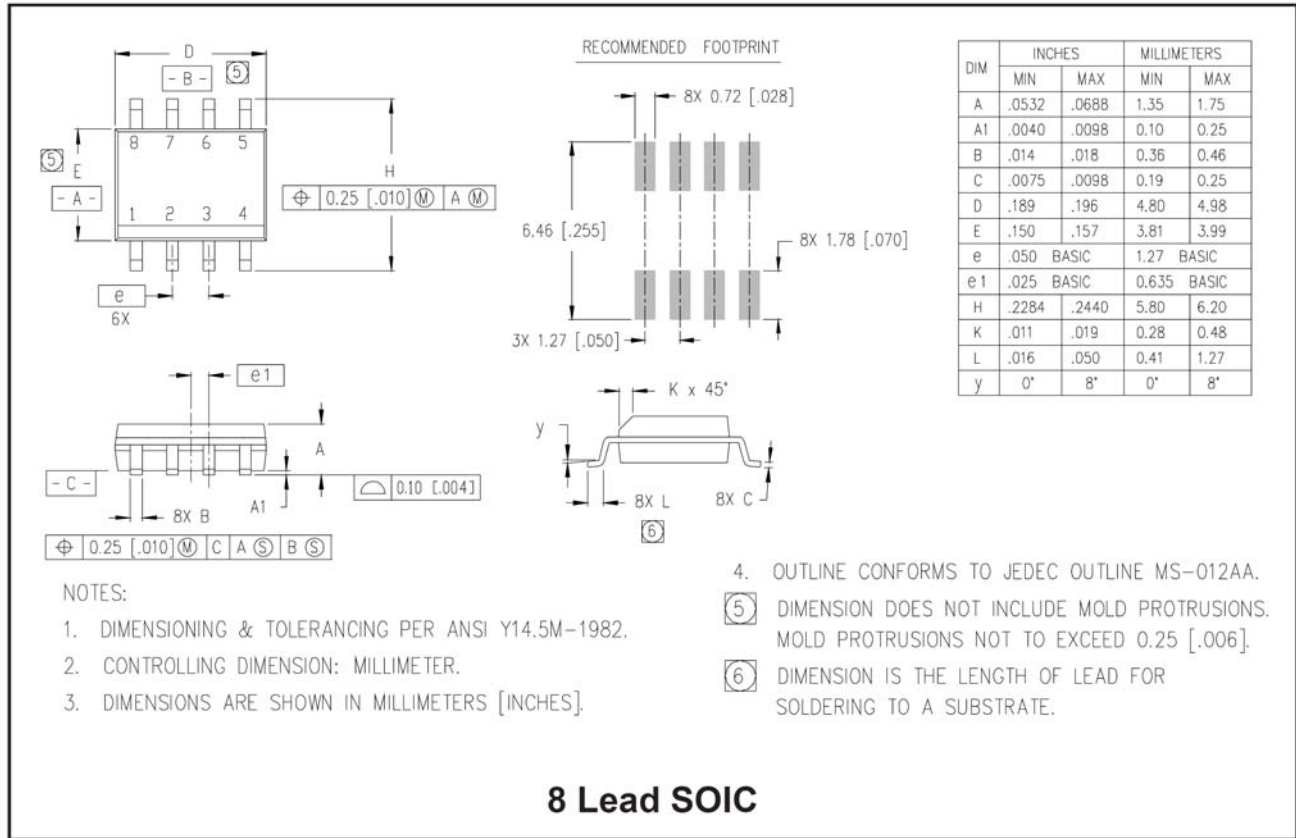
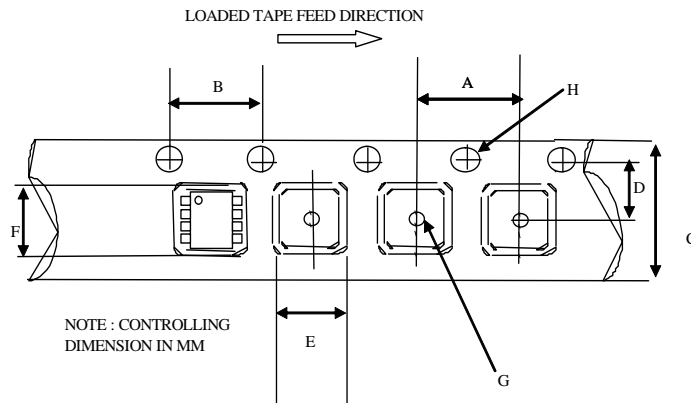


Figure 20. V_{BS} UV- Threshold Voltage vs. Temperature

Package Details

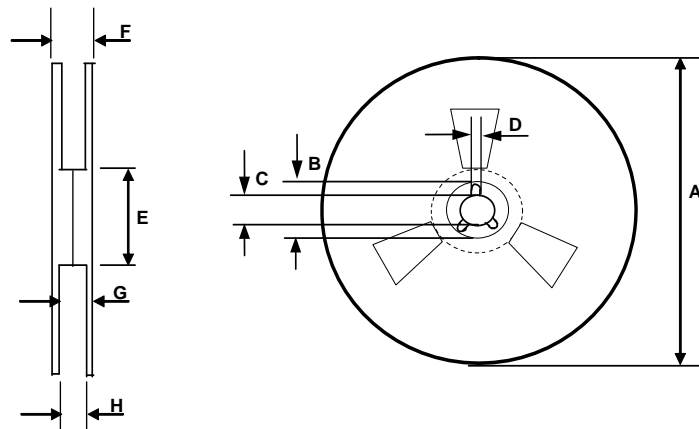


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

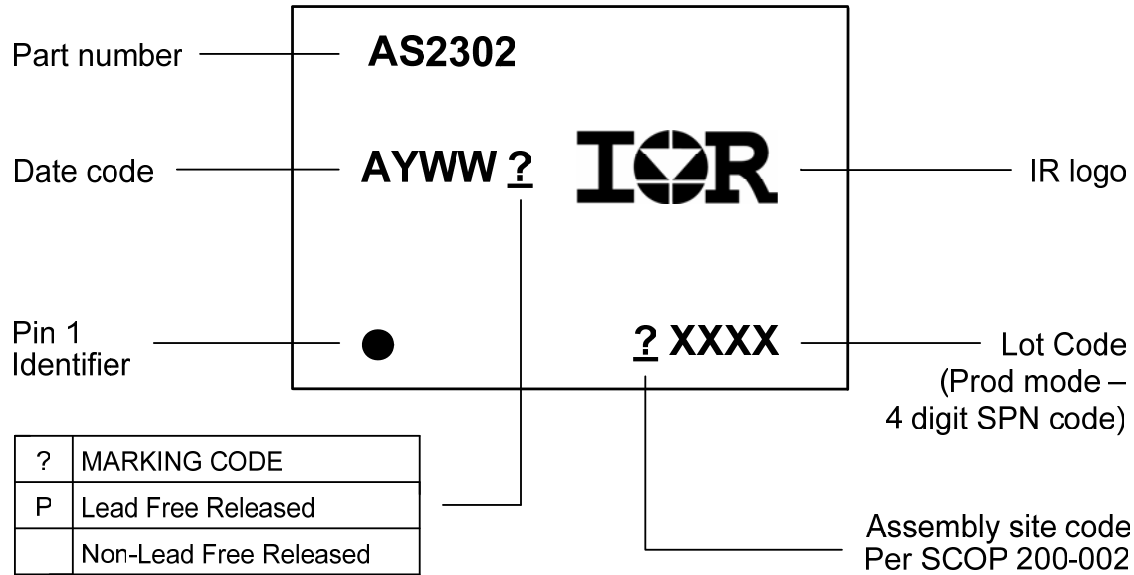
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 8SOICN

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

Part Marking Information



* Qualification standards can be found on IR's web site ww.irf.com

Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
| | | Form | Quantity | |
| AUIRS2302S | SOIC8 | Tube/Bulk | 95 | AUIRS2302S |
| | | Tape and Reel | 2500 | AUIRS2302STR |

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