PD-91400D

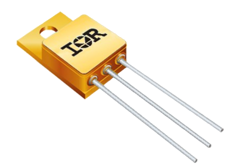
IRHY9130CM
JANSR2N7382

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-257AA)

100V, P-CHANNEL
REF: MIL-PRF-19500/615
RAD Hard™HEXFET ® TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHY9130CM	100 kRads(Si)	0.30Ω	-11A	JANSR2N7382
IRHY93130CM	300 kRads(Si)	0.30Ω	-11A	JANSF2N7382



TO-257AA

Description

IR HiRel RADHard™ HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low $R_{DS(on)}$
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Light Weight
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-11	A
I_{D2} @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-7.0	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	-44	
P_D @T_C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	150	mJ
I_{AR}	Avalanche Current ①	-11	A
E_{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-16	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	4.3 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to 25°C, I_D = 1-.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	V_{GS} = -12V, I_{D2} = -7.0A ④
		—	—	0.35		V_{GS} = -12V, I_{D1} = -11A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
gfs	Forward Transconductance	2.5	—	—	S	V_{DS} = -15V, I_{D2} = -7.0A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	µA	V_{DS} = -80V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	45	nC	I_{D1} = -11A
Q_{GS}	Gate-to-Source Charge	—	—	10		V_{DS} = -50V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	25		V_{GS} = -12V
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	V_{DD} = -50V
t_r	Rise Time	—	—	50		I_{D1} = -11A
$t_{d(off)}$	Turn-Off Delay Time	—	—	70		R_G = 7.5Ω
t_f	Fall Time	—	—	70		V_{GS} = -12V
Ls +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1200	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	310	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	80	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-11	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-3.0	V	T_J=25°C, I_S = -11A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J=25°C, I_F = -11A, V_{DD} ≤ -50V
Q_{rr}	Reverse Recovery Charge	—	—	1.0	µC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	80	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = -25V, starting T_J = 25°C, L = 2.4mH, Peak I_L = -11A, V_{GS} = -12V
③ I_{SD} ≤ -11A, di/dt ≤ -440A/µs, V_{DD} ≤ -100V, T_J ≤ 150°C
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
⑤ Total Dose Irradiation with V_{GS} Bias. -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
⑥ Total Dose Irradiation with V_{DS} Bias. -80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	100 kRads (Si)[1]		Up to 300k - 1000 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	——	-100	——	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	-100	——	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	100	——	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	——	-25	——	-25	µA	V_{DS} = -80V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.30	——	0.30	Ω	V_{GS} = -12V, I_{D2} = -7.0A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-257AA)	——	0.30	——	0.30	Ω	V_{GS} = -12V, I_{D2} = -7.0A
V_{SD}	Diode Forward Voltage ④	——	-3.0	——	-3.0	V	V_{GS} = 0V, I_S = -11A

1. Part number IRHY9130CM (JANSR2N7382)
2. Part number IRHY93130CM (JANSF2N7382)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)				
				@ VGS = 0V	@ VGS = 5V	@ VGS = 10V	@ VGS = 15V	@ VGS = 20V
Cu	28	285	43	-100	-100	-100	-70	-50
Kr	38.8	320	39.6	-100	-100	-75	-50	——
Xe	63.4	348	32.5	-50	——	——	——	——

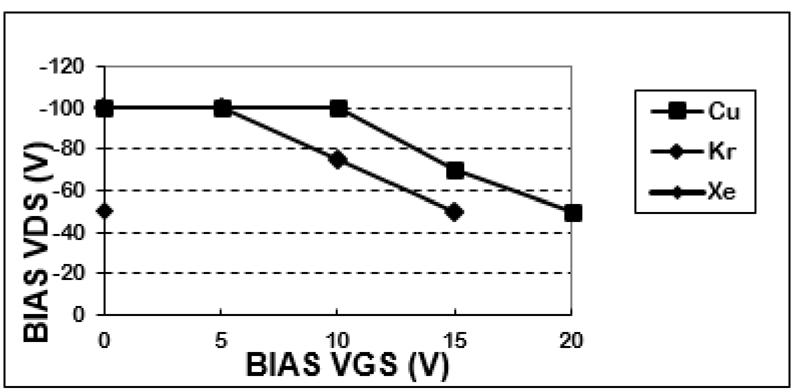


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

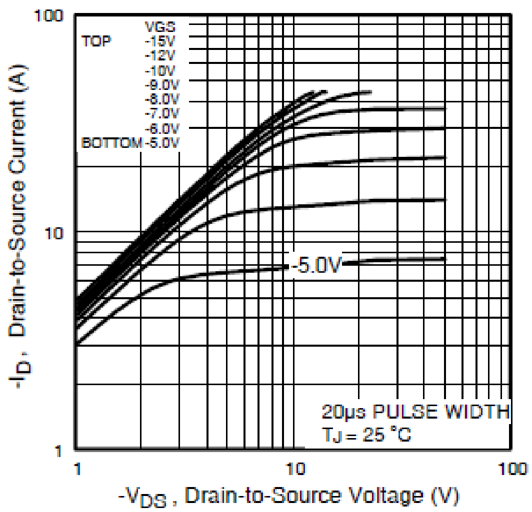


Fig 1. Typical Output Characteristics

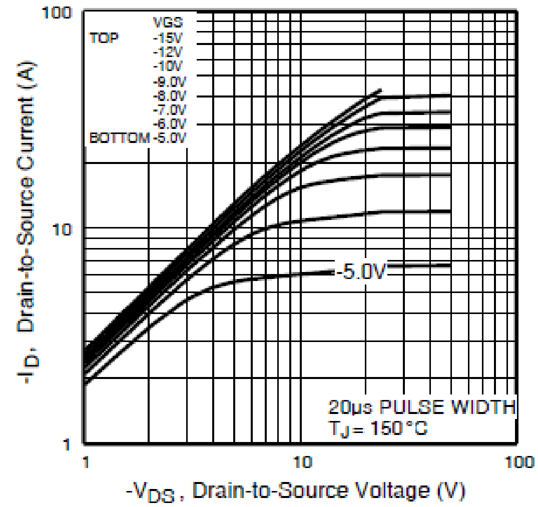


Fig 2. Typical Output Characteristics

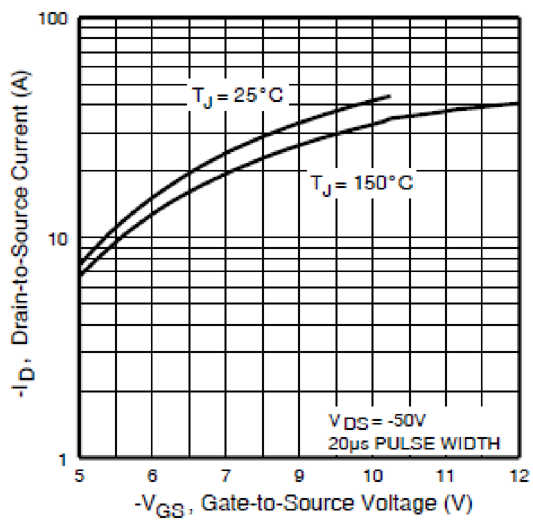


Fig 3. Typical Transfer Characteristics

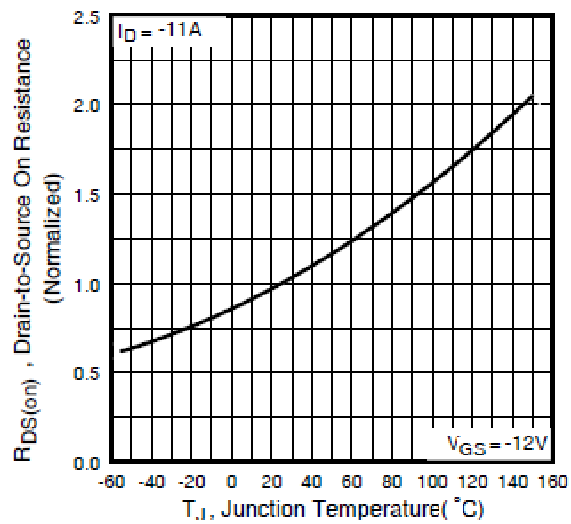


Fig 4. Normalized On-Resistance Vs. Temperature

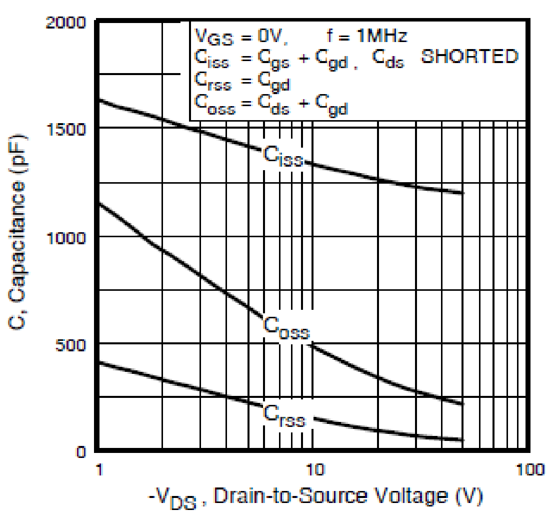


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

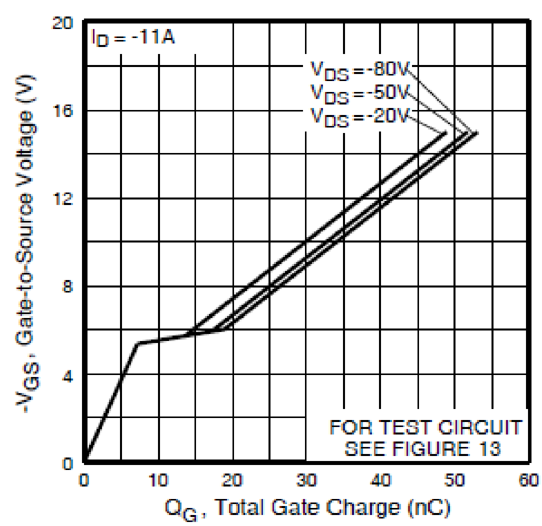


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

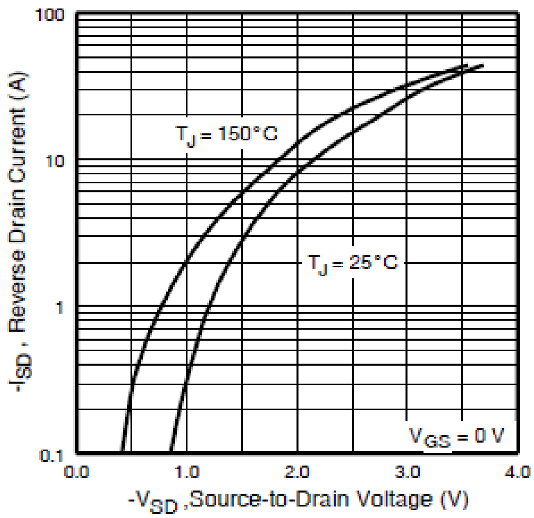


Fig 7. Typical Source-Drain Diode Forward Voltage

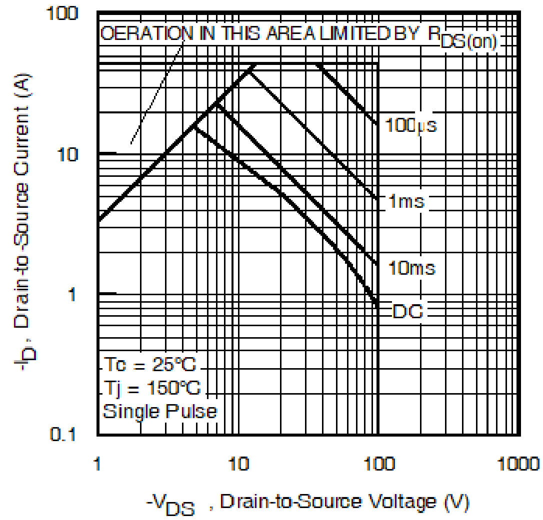


Fig 8. Maximum Safe Operating Area

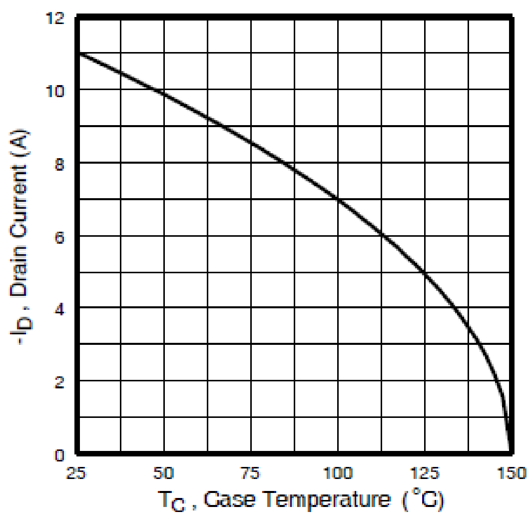


Fig 9. Maximum Drain Current Vs. Case Temperature

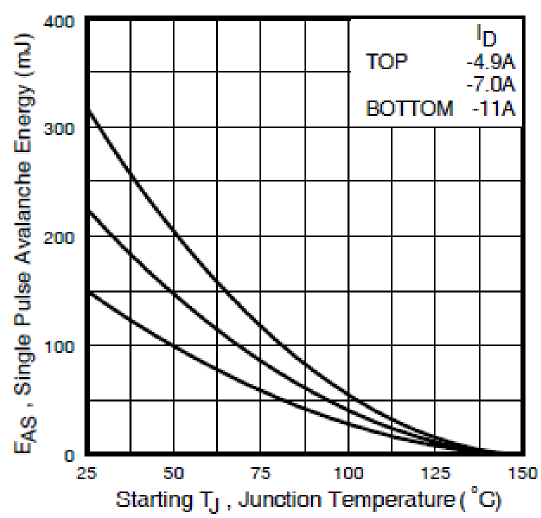


Fig 10. Maximum Avalanche Energy Vs. Drain Current

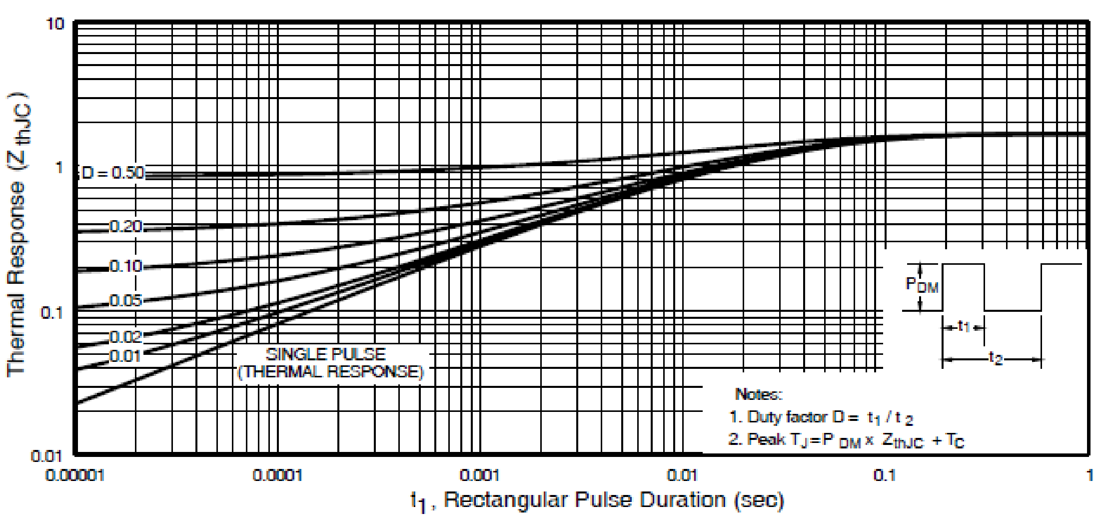


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

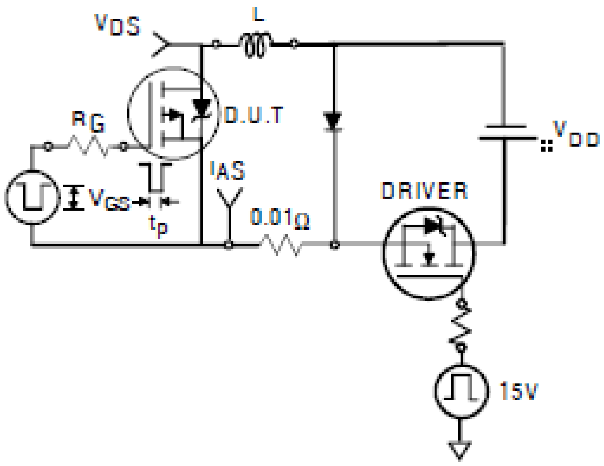


Fig 12a. Unclamped Inductive Test Circuit

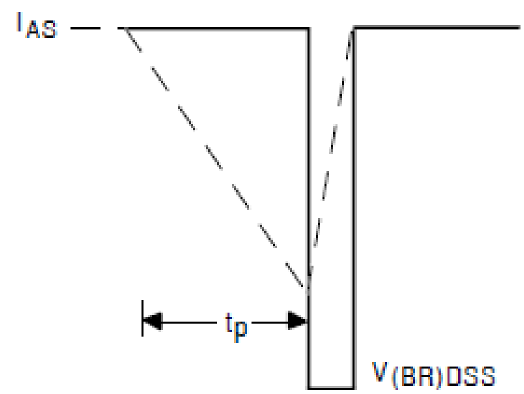


Fig 12b. Unclamped Inductive Waveforms

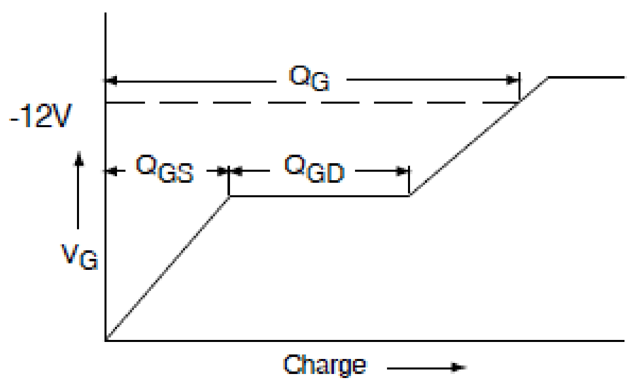


Fig 13a. Gate Charge Waveform

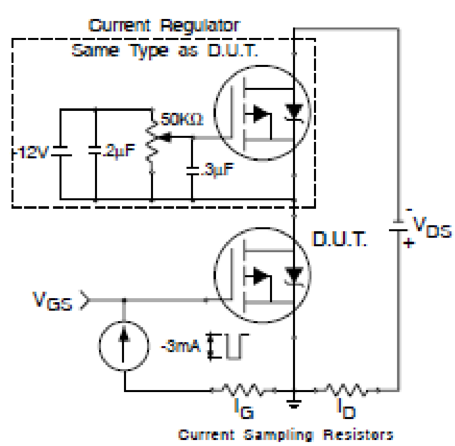


Fig 13b. Gate Charge Test Circuit

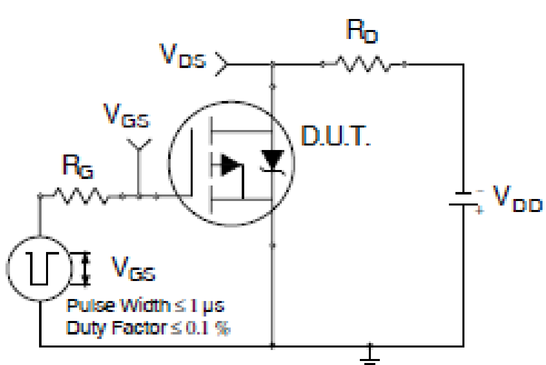


Fig 14a. Switching Time Test Circuit

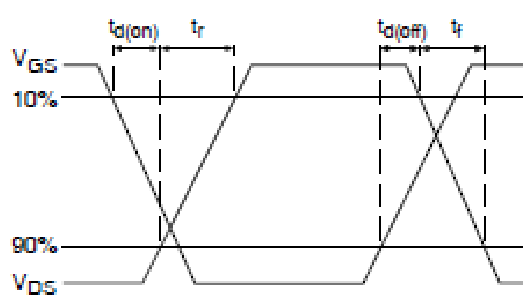
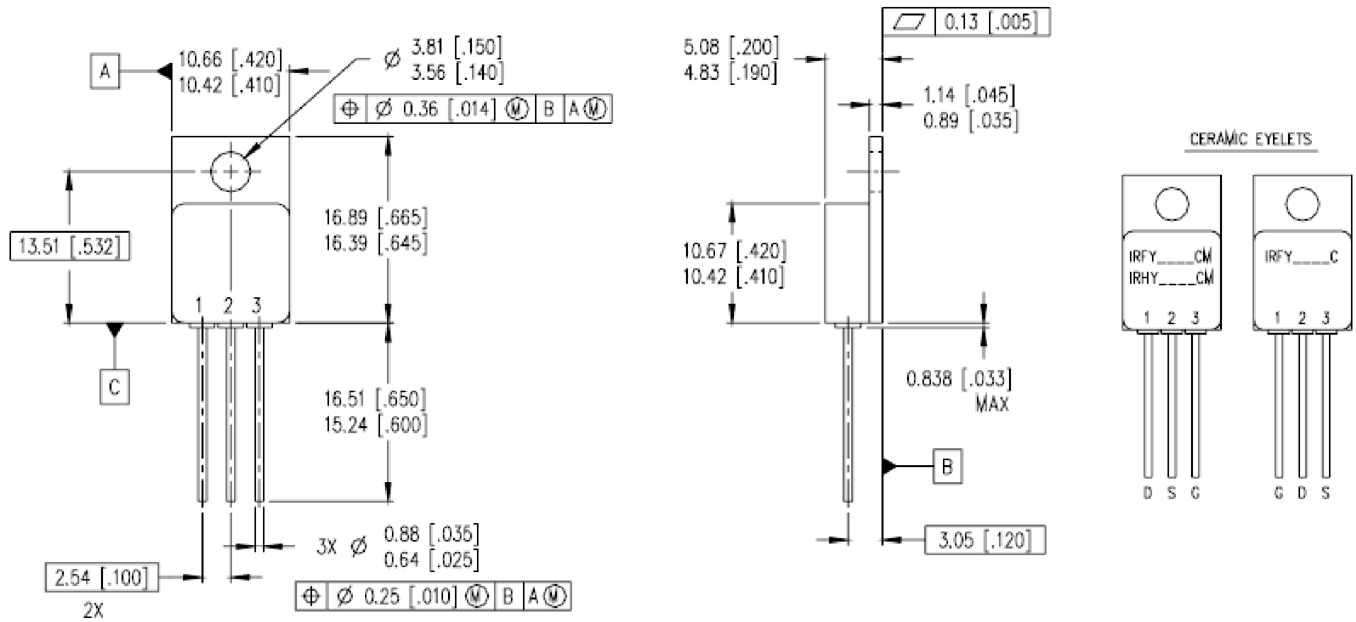


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — TO-257AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

LEGEND

D – DRAIN
S – SOURCE
G – GATE

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