# Technical Note

## Migrating from Macronix's MX66L 512Mb to Micron's MT25Q 512Mb Flash Device

## Introduction

This technical note compares the features of the Micron® MT25Q (512Mb) Flash memory device with the Macronix MX66L51235F Flash memory device. Features compared include memory architecture, package options, signal descriptions, internal registers, command sets, electrical specifications, and device identification.

See the MT25Q data sheet for detailed specifications.

# Memory Array Architecture

### Table 1: Memory Array Architecture

| MT25Q Features | MX66L Features |
|---|---|
| Program 1 to 256 bytes | Program 1 to 256 bytes |
| Uniform sector erase (64KB) | Uniform sector erase (64KB) |
| Uniform subsector erase (32KB and 4KB) | Uniform subsector erase (32KB and 4KB) |
| Cycling endurance 100,000 | Cycling endurance 100,000 |
| Data retention 20 years | Data retention 20 years |

# Package Configurations

### Table 2: Package Configurations

| Package (JEDEC Code) | MT25Q | MX66L |
|---|---|---|
| V-PDFN-8 (8mm x 6mm) | No | Yes |
| SOP2-16/300 mils | Yes | Yes |
| T-PBGA-24b05 (8mm x 6mm, 4 x 6 ball) | Yes | Yes |

# Signal Descriptions

### Table 3: Signal Descriptions

| MT25Q Signal | MX66L Signal | Type | Description | Notes |
|---|---|---|---|---|
| C | SCLK | Input | Serial clock | |
| DQ0 | SI/SIO0 | Input or I/O | Serial data input or I/O | |
| DQ1 | SO/SIO1 | Output or I/O | Serial data output or I/O | |
| S# | CS# | Input | Chip select | |
| W#/DQ2 | WP#/SIO2 | Input or I/O | Write protect/enhanced program supply voltage or I/O | |
| HOLD#/DQ3 | RESET#/SIO3 | Input or I/O | Hold or I/O | 1 |
| $V_{CC}$ | $V_{CC}$ | Input | Supply voltage | |
| $V_{SS}$ | GND | Input | Ground | |
| RESET# | RESET# | – | Reset | 2 |

Notes:
1. Available on the MX66L device WSON package only.
2. On the MT25Q device, the dedicated RESET# pin is available with specific part numbers only. For all other part numbers, RESET# takes the place of HOLD#.

# Registers

### Table 4: Configuration Register

| Name | MT25Q | MX66L | Notes |
|---|---|---|---|
| Nonvolatile | NVCR | – | |
| Dummy cycle | [15:12] | – | |
| XIP at power on | [11:9] | – | |
| Output driver strength | [8:6] | – | |
| Double transfer rate (DTR) protocol | [5] | – | |
| Reset/hold | [4] | – | |
| Quad I/O protocol | [3] | – | |
| Dual I/O protocol | [2] | – | |
| 128Mb segmentation select | [1] | – | |
| 3-byte or 4-byte address | [0] | – | |
| Volatile | VCR | Configuration register bit | |
| Dummy cycle | [7:4] | [7:6] | |
| 3-byte or 4-byte address | – | [5] | 1 |
| Top/bottom area | – | [3] | 2 |
| XIP | [3] | – | |
| Reserved | [2] | – | |
| Wrap | [1:0] | – | |
| Enhanced Volatile | EVCR | Configuration register bit | |
| Quad I/O protocol | [7] | – | |
| Dual I/O protocol | [6] | – | |
| DTR protocol | [5] | – | |
| Reset/hold | [4] | – | |
| Reserved | [3] | – | |
| Output driver strength | [2:0] | [2:0] | |

Notes:
1. Functionality is available in the NVCR register for the MT25Q device.
2. Bit is OTP for the MX66L device. Status register bit 5 has the same functionality for the MT25Q device.

### Table 5: Status Register

| Name | MT25Q | MX66L | Type | Notes |
|---|---|---|---|---|
| Status register write enable/disable | [7] | [7] | Nonvolatile | |
| Quad I/O | N/A | [6] | Nonvolatile | 1 |
| Protect area size | [6,4:2] | [5:2] | Nonvolatile | |
| Top/bottom | [5] | N/A | Nonvolatile | 2 |
| Write enable latch (WEL) | [1] | [1] | Volatile | |

**Table 5: Status Register (Continued)**

| Name | MT25Q | MX66L | Type | Notes |
|---|---|---|---|---|
| Write in progress (WIP) | [0] | [0] | Volatile | |

Notes:
1. Bit 7 in the extended volatile configuration register for the MX66L device.
2. Bit 3 in the configuration register for the MX66L device.

**Table 6: Flag Status Register (MT25Q)/Security Register (MX66L)**

| Bit | MT25Q | MX66L | Notes |
|---|---|---|---|
| [7] | Program/erase controller | Write protection set | 1 |
| [6] | Erase suspend | Erase check | |
| [5] | Erase | Program check | |
| [4] | Program | Reserved | |
| [3] | Reserved | Erase suspend | |
| [2] | Program suspend | Program suspend | |
| [1] | Protection | Protection | 1 |
| [0] | 3-byte or 4-byte addressing | Lock chip | 1 |

Note:
1. Bit is OTP for the MX66L device.

# Commands

### Table 7: Command Set

| Command | MT25Q | MX66L | Notes |
|---|---|---|---|
| **RESET Operations** | | | |
| RESET ENABLE | 66h | 66h | |
| RESET MEMORY | 99h | 99h | |
| NOP | N/A | 00h | |
| PERFORMANCE ENHANCE MODE RESET | N/A | FFh | 1 |
| **IDENTIFICATION Operations** | | | |
| READ ID | 9Eh/9Fh | 9Fh | |
| MULTIPLE I/O READ ID | AFh/9Eh | AFh | |
| READ ELECTRONICS SIGNATURE | N/A | ABh | |
| READ MAN and DEV ID | N/A | 90h | |
| READ SERIAL FLASH DISCOVERY PARAMETER | 5Ah | 5Ah | |
| **READ Operations** | | | |
| READ | 03h | 03h | |
| FAST READ | 0Bh | 0Bh | |
| DUAL OUTPUT FAST READ | 3Bh | 3Bh | |
| DUAL INPUT/OUTPUT FAST READ | BBh | BBh | |
| QUAD OUTPUT FAST READ | 6Bh | 6Bh | 2 |
| QUAD INPUT/OUTPUT FAST READ | EBh | EBh | 2 |
| FAST READ (DTR mode) | 0Dh | N/A | |
| DUAL OUTPUT FAST READ (DTR mode) | 3Dh | N/A | |
| DUAL INPUT/OUTPUT FAST READ (DTR mode) | BDh | N/A | |
| QUAD OUTPUT FAST READ (DTR mode) | 6Dh | N/A | |
| QUAD INPUT/OUTPUT FAST READ (DTR mode) | EDh | N/A | |
| QUAD INPUT/OUTPUT WORD READ | E7h | N/A | |
| **4-BYTE ADDRESS MODE Operations** | | | |
| ENTER 4-BYTE ADDRESSING | B7h | B7h | |
| EXIT 4-BYTE ADDRESSING | E9h | E9h | |
| 4-BYTE READ | 13h | 13h | |
| 4-BYTE FAST_READ | 0Ch | 0Ch | |
| 4-BYTE DUAL OUTPUT FAST READ | 3Ch | 3Ch | |
| 4-BYTE DUAL INPUT/OUTPUT FAST READ | BCh | BCh | |
| 4-BYTE QUAD OUTPUT FAST READ | 6Ch | 6Ch | |
| 4-BYTE QUAD INPUT/OUTPUT FAST READ | ECh | ECh | |
| 4-BYTE FAST READ (DTR mode) | 0Eh | N/A | |
| 4-BYTE DUAL INPUT/OUTPUT FAST READ (DTR mode) | BEh | N/A | |
| 4-BYTE QUAD INPUT/OUTPUT FAST READ (DTR mode) | EEh | N/A | |
| 4-BYTE PAGE PROGRAM | 12h | 12h | |

**Table 7: Command Set (Continued)**

| Command | MT25Q | MX66L | Notes |
|---|---|---|---|
| 4-BYTE QUAD INPUT FAST PROGRAM | 34h | N/A | 3 |
| 4-BYTE QUAD INPUT EXTENDED FAST PROGRAM | 3Eh | 3Eh | |
| 4-BYTE SECTOR ERASE (64KB) | DCh | DCh | |
| 4-BYTE SECTOR ERASE (32KB) | N/A | 5Ch | |
| 4-BYTE SUBSECTOR ERASE (4KB) | 21h | 21h | |
| 4-BYTE READ VOLATILE LOCK BITS | E0h | N/A | |
| 4-BYTE WRITE VOLATILE LOCK BITS | E1h | N/A | |
| **WRITE Operations** | | | |
| WRITE ENABLE | 06h | 06h | |
| WRITE DISABLE | 04h | 04h | |
| **REGISTER Operations** | | | |
| READ STATUS REGISTER | 05h | 05h | |
| WRITE STATUS REGISTER | 01h | 01h | |
| READ FLAG STATUS REGISTER | 70h | 2Bh | 4 |
| CLEAR FLAG STATUS REGISTER | 50h | 2Fh | 4 |
| READ NONVOLATILE CONFIGURATION REGISTER | B5h | N/A | 5 |
| WRITE NONVOLATILE CONFIGURATION REGISTER | B1h | N/A | 5 |
| READ VOLATILE CONFIGURATION REGISTER | 85h | N/A | 5 |
| WRITE VOLATILE CONFIGURATION REGISTER | 81h | N/A | 5 |
| READ ENHANCED VOLATILE CONFIGURATION REGISTER | 65h | N/A | |
| WRITE ENHANCED VOLATILE CONFIGURATION REGISTER | 61h | N/A | |
| READ EXTENDED ADDRESS REGISTER | C8h | C8h | |
| WRITE EXTENDED ADDRESS REGISTER | C5h | C5h | |
| **Miscellaneous Operations** | | | |
| READ CONFIGURATION REGISTER | N/A | 15h | 6 |
| AUTOBOOT REGISTER READ | N/A | 16h | |
| AUTOBOOT REGISTER WRITE | N/A | 17h | |
| AUTOBOOT REGISTER ERASE | N/A | 18h | |
| DYNAMIC PROTECTION BIT READ | E8h | E0h | 7 |
| DYNAMIC PROTECTION BIT WRITE | E5h | E1h | 8 |
| PASSWORD READ | 27h | 27h | |
| PASSWORD PROGRAM | 28h | 28h | |
| PASSWORD ULOCK | 29h | 29h | |
| WRITE PROTECTION SELECTION | N/A | 68h | |
| SET BURST LENGTH | N/A | C0h | |
| GANG BLOCK LOCK | N/A | 7Eh | |
| GANG BLOCK UNLOCK | N/A | 98h | |
| READ SECTOR PROTECTION | 2Dh | 2Dh | 9 |

**Table 7: Command Set (Continued)**

| Command | MT25Q | MX66L | Notes |
|---|---|---|---|
| PROGRAM SECTOR PROTECTION | 2Ch | 2Ch | 10 |
| READ NONVOLATILE LOCK BITS | E2h | E2h | 11 |
| WRITE NONVOLATILE LOCK BITS | E3h | E3h | 12 |
| ERASE NONVOLATILE LOCK BITS | E4h | E4h | 13 |
| READ GLOBAL FREEZE BITS | A7h | A7h | 14 |
| WRITE GLOBAL FREEZE BIT | A6h | A6h | 15 |
| CYCLIC REDUNDANCY CHECK | 9Bh/27h | N/A | |
| **PROGRAM Operations** | | | |
| PAGE PROGRAM | 02h | 02h | |
| DUAL INPUT FAST PROGRAM | A2h | N/A | |
| EXTENDED DUAL INPUT FAST PROGRAM | D2h | N/A | |
| QUAD INPUT FAST PROGRAM | 32h | N/A | |
| EXTENDED QUAD INPUT FAST PROGRAM | 38h | 38h | |
| **ERASE Operations** | | | |
| BULK ERASE | C7h | 60h or C7h | |
| SECTOR ERASE (64KB) | D8h | D8h | |
| SECTOR ERASE (32KB) | 52h | 52h | |
| SUBSECTOR ERASE (4KB) | 20h | 20h | |
| PROGRAM/ERASE SUSPEND | 75h | B0h | |
| PROGRAM/ERASE RESUME | 7Ah | 30h | |
| **ONE-TIME PROGRAMMABLE (OTP) Operations** | | | |
| READ OTP ARRAY | 4Bh | N/A | |
| PROGRAM OTP ARRAY | 42h | N/A | |
| ENTER SECURE OTP | N/A | B1h | 16 |
| EXIT SECURE OTP | N/A | C1h | 16 |
| **DEEP POWER-DOWN Operations** | | | |
| DEEP POWER DOWN | B9h | B9h | |
| RELEASE FROM DEEP POWER DOWN | ABh | ABh | |
| **QUAD Operations** | | | |
| ENTER QUAD | 35h | 35h | |
| EXIT QUAD | F5h | F5h | |

Notes:
1. Execution in place (XIP) device reset. For the MT25Q device, FFh sequence exits from dual or quad protocol (see XIP Mode and XIP Reset).
2. For the MX66L device, the quad enable (QE) bit in the status register must be set to 1 before sending the 4READ command.
3. The MX66L device does not support the configuration opcode: (single) + address (single) + data (quad); the device supports the extended configuration opcode only: (single) + address (quad) + data (quad).
4. For the MX66L device, the flag register is SECURITY and the opcode name is RDSCUR.
5. The MX66L device does not have a nonvolatile configuration register (NVCR).

6. Equivalent register in the MT25Q device is VCR.
7. READ VOLATILE LOCK BITS command for the MT25Q device.
8. WRITE VOLATILE LOCK BITS command for the MT25Q device
9. Protection configurations are identical for the MX66L and MT25Q devices (READ LOCK REGISTER (RDLR) command).
10. WRITE LOCK REGSITER (WRLR) command in the MX66L device.
11. READ SPB STATUS (RDSPB) command in the MX66L device.
12. SPB BIT PROGRAM (WRSPB) command in the MX66L device.
13. ALL SPB BIT ERASE (ESSPB) command in the MX66L device.
14. SPB LOCK REGISTER READ (RDSPBLK) command in the MX66L device.
15. SPB LOCK SET (SPBLK) command in the MX66L device.
16. Not required for enabling access to the OTP array (64KB instead of 4KB in the MX66L device). READ OTP/PROGRAM OTP featured in the MT25Q device.

**Table 8: Different Commands Sharing the Same Code**

| Command Code | MT25Q | MX66L |
|---|---|---|
| ABh | RELEASE FROM DEEP POWER-DOWN | RELEASE FROM DEEP POWER-DOWN and READ ELECTRONIC SIGNATURE |
| B1h | WRITE NVCR | ENTER SECURE OTP |

## READ Commands

The READ/FAST READ commands for the MT25Q and MX66L devices are identical, and both devices follow the standard 3-byte and 4-byte address protocol.

**Table 9: 4-Byte Mode Configuration**

| MT25Q | MX66L |
|---|---|
| Set nonvolatile configuration register bit 0 | Set volatile configuration register bit 5 |
| Set operation code B7h | Set operation code B7h |
| Dedicate command set at 4 bytes | Dedicate command set at 4 bytes |

The MT25Q and MX66L devices have configurable dummy cycles. For the MX66L device, dummy cycles can be set with configuration register bits [7:6]. For the MT25Q device, dummy cycles can be set with nonvolatile configuration register bits [15:12] or with volatile configuration register bits [7:4]. The minimum number of dummy clocks is a function of frequency.

**Note:** The MX66L device does not support double transfer rate (DTR).

**Table 10: STR: Minimum Number of Dummy Cycles Required per Each Frequency**

| Frequency (MHz) | FAST READ | | DUAL OUTPUT FAST READ | | DUAL I/O FAST READ | | QUAD OUTPUT FAST READ | | QUAD I/O FAST READ | |
|---|---|---|---|---|---|---|---|---|---|---|
| | MT25Q | MX66L | MT25Q | MX66L | MT25Q | MX66L | MT25Q | MX66L | MT25Q | MX66L |
| ≤50 | 1 | 6 | 1 | 6 | 1 | 4 | 1 | 6 | 3 | 4 |
| ≤80 | 1 | 6 | 1 | 6 | 3 | 4 | 3 | 6 | 6 | 6 |
| ≤90 | 1 | 6 | 2 | 6 | 4 | 6 | 4 | 8 | 7 | 8 |

**Table 10: STR: Minimum Number of Dummy Cycles Required per Each Frequency (Continued)**

| Frequency (MHz) | FAST READ | | DUAL OUTPUT FAST READ | | DUAL I/O FAST READ | | QUAD OUTPUT FAST READ | | QUAD I/O FAST READ | |
|---|---|---|---|---|---|---|---|---|---|---|
| | MT25Q | MX66L | MT25Q | MX66L | MT25Q | MX66L | MT25Q | MX66L | MT25Q | MX66L |
| ≤104 | 2 | 6 | 3 | 6 | 4 | 6 | 5 | 8 | 8 | 8 |
| ≤133 | 4 | 10 | 6 | 10 | 7 | 10 | 8 | 10 | 11 | 10 |

# XIP Mode

The MT25Q device enters and exits execute-in-place (XIP) mode via the volatile and nonvolatile configuration registers. The nonvolatile configuration register sets XIP mode at device power on. The MX66L device uses two confirmation nibbles to enter or exit XIP mode and is fully compatible with the MT25Q XIP methodology; other bits are "Don't Care". XIP management is identical in both devices.

**Table 11: XIP Mode**

| Protocol | MT25Q | MX66L |
|---|---|---|
| Fast read | Yes | N/A |
| Dual output fast read | Yes | N/A |
| Dual I/O fast read | Yes | N/A |
| Quad output fast read | Yes | N/A |
| Quad I/O fast read | Yes | Yes |

**Figure 1: XIP Timing**

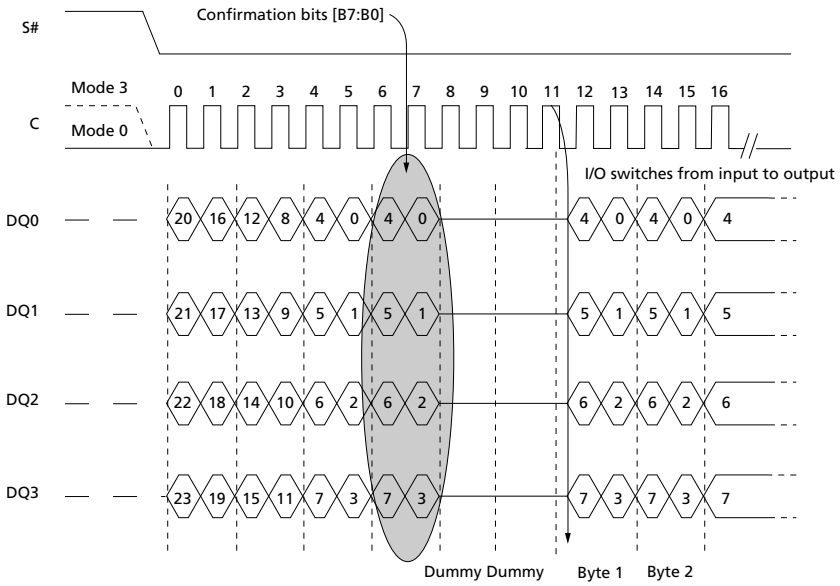


**Table 12: XIP Confirmation Bit Software Commands**

| Description | MT25Q | MX66L |
|---|---|---|
| Enter/confirm XIP mode | B4 = 0 (B7.B5 and B3.B0 = "Don't Care") | B7 ≠ B3 and B6 ≠ B2 and B5 ≠ B1 and B4 ≠ B0 |
| Exit XIP mode | B4 = 1 (B7.B5 and B3.B0 = "Don't Care") | B7 = B3 or B6 = B2 or B5 = B1 or B4 = B0 |

## XIP Reset

This procedure is required because when power loss occurs, the device may start in an indeterminate state (XIP or an unnecessary protocol).

To reset XIP mode for the MX66L device (use command FFh for MT25Q):

1. Perform the XIP exit sequence.
2. Perform the dual SPI protocol exit sequence.

**Note:** During execution of the WRITE NONVOLATILE CONFIGURATION REGISTER command, $^{t}$SHSL2 must be at least 50ns.

**Figure 2: XIP Exit Sequence**

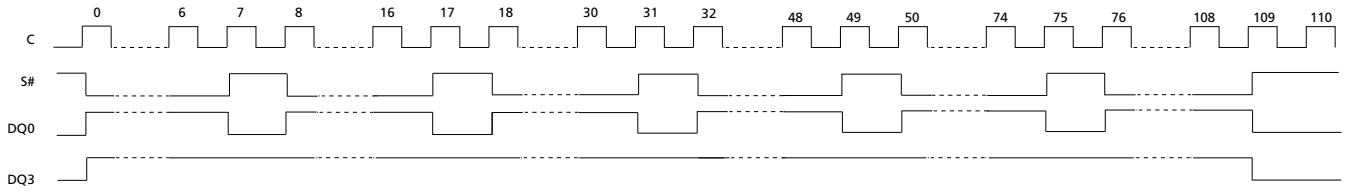
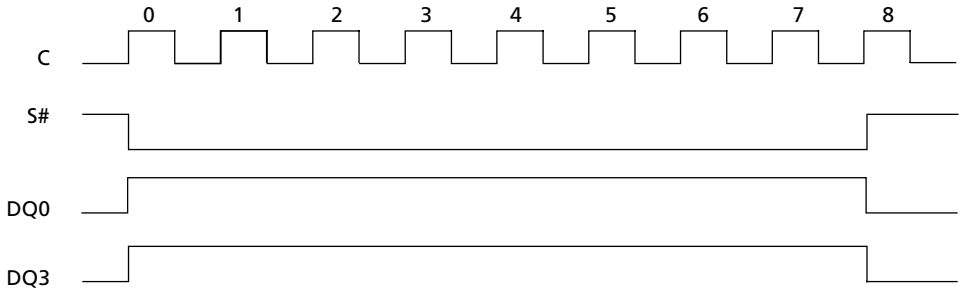



**Figure 3: Dual SPI Protocol Exit Sequence**



# Electrical Characteristics

### Table 13: DC Characteristics

| Parameter | Symbol | MT25Q | | MX66L | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Standby current | $I_{CC1}$ | 60 | 100 | 60 | 200 | µA |
| Operating current (fast read quad I/O) | $I_{CC3}$ | – | 10 | – | 40 | mA |
| Operating current (page program) | $I_{CC4}$ | – | 60 | – | 25 | mA |
| Operating current (write status register) | $I_{CC5}$ | – | 60 | – | 40 | mA |
| Operating current (erase) | $I_{CC6}$ | – | 50 | – | 50 | mA |

### Table 14: DC Voltage

| Parameter | Symbol | MT25Q | | MX66L | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Input low voltage | $V_{IL}$ | –0.5 | 0.3 $V_{CC}$ | –0.5 | 0.8 | V |
| Input high voltage | $V_{IH}$ | 0.7 $V_{CC}$ | $V_{CC}$ + 0.4 | 0.7 $V_{CC}$ | $V_{CC}$ + 0.4 | V |
| Output low voltage | $V_{OL}$ | – | 0.4 | – | 0.2 | V |
| Output high voltage | $V_{OH}$ | $V_{CC}$ – 0.2 | – | $V_{CC}$ – 0.2 | – | V |

### Table 15: AC Specifications

| Parameter | Symbol | Alternate Symbol | MT25Q | | MX66L | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Clock frequency (x1 fast read) | $^{f}C$ | $^{f}C$ | – | 133 | – | 133[1] | MHz |
| Clock frequency (x2, x4 fast read) | $^{f}C$ | $^{f}C$ | – | 133 | – | 84 | MHz |
| Clock frequency (read) | $^{f}R$ | $^{f}R$ | – | 54 | – | 50 | MHz |
| S# active setup time | $^{t}SLCH$ | $^{t}CSS$ | 3.38 | – | 5 | – | ns |
| Data in setup time | $^{t}DVCH$ | $^{t}DSU$ | 1.75 | – | 2 | – | ns |
| Data in hold time | $^{t}CHDX$ | $^{t}DH$ | 2.5 | – | 4 | – | ns |
| S# deselect time after correct read | $^{t}SHSL1$ | $^{t}CSH$ | 20 | – | 7 | – | ns |
| S# deselect time after non-read | $^{t}SHSL2$ | $^{t}CSH$ | 50 | – | 30 | – | ns |
| Output disable time (2.7–3.6V) | $^{t}SZQZ$ | $^{t}DIS$ | – | 7 | – | 8 | ns |
| Clock low to output valid (under 30pF) | $^{t}CLQV$ | $^{t}V$ | – | 6 | – | 9 | ns |
| Output hold time | $^{t}CLQX$ | $^{t}HO$ | 1 | – | 1 | – | ns |
| Hold to output Low-Z | $^{t}HHQX$ | $^{t}LZ$ | N/A | 8 | N/A | N/A | ns |
| Hold to output High-Z | $^{t}HLQZ$ | $^{t}HZ$ | N/A | 8 | N/A | N/A | ns |

Note: 1. 104 MHz clock frequency for the MX66L device.

**Table 16: Program and Erase Specifications**

| Operation | MT25Q | | MX66L | | Unit |
|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | |
| PAGE PROGRAM (256 bytes) | 0.2 | 2.8 | 0.6 | 3 | ms |
| PROGRAM OTP (64 bytes) | 0.12 | 0.8 | – | – | ms |
| 4KB SUBSECTOR ERASE | 0.05 | 0.4 | 0.043 | 0.2 | s |
| 32KB SUBSECTOR ERASE | 0.1 | 1 | 0.19 | 1 | s |
| 64KB SECTOR ERASE | 0.15 | 1 | 0.34 | 2 | s |
| BULK ERASE | 153 | 460 | 120 | 300 | s |

# Memory Map – 512Mb Density

**Table 17: Sectors [1023:0]**

| Sector | 32KB Subsectors | 4KB Subsector | Address Range | |
|---|---|---|---|---|
| | | | Start | End |
| 1023 | 2047 | 16383 | 03FF F000h | 03FF FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | 2046 | ⋮ | ⋮ | ⋮ |
| | | 16368 | 03FF 0000h | 03FF 0FFFh |
| ⋮ | | ⋮ | ⋮ | ⋮ |
| 511 | 1023 | 8191 | 01FF F000h | 01FF FFFFh |
| | | | | |
| | 1022 | ⋮ | ⋮ | ⋮ |
| | | 8176 | 01FF 0000h | 01FF 0FFFh |
| ⋮ | | ⋮ | ⋮ | ⋮ |
| 255 | 511 | 4095 | 00FF F000h | 00FF FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | 510 | ⋮ | ⋮ | ⋮ |
| | | 4080 | 00FF 0000h | 00FF 0FFFh |
| ⋮ | | ⋮ | ⋮ | ⋮ |
| 127 | 255 | 2047 | 007F F000h | 007F FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | 254 | ⋮ | ⋮ | ⋮ |
| | | 2032 | 007F 0000h | 007F 0FFFh |
| ⋮ | | ⋮ | ⋮ | ⋮ |
| 63 | 125 | 1023 | 003F F000h | 003F FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | 124 | ⋮ | ⋮ | ⋮ |
| | | 1008 | 003F 0000h | 003F 0FFFh |
| ⋮ | | ⋮ | ⋮ | ⋮ |
| 0 | 1 | 15 | 0000 F000h | 0000 FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | 0 | ⋮ | ⋮ | ⋮ |
| | | 0 | 0000 0000h | 0000 0FFFh |

# Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the MT25Q and MX66L devices have different manufacturer ID and memory codes even though their memory capacity is identical. To read these codes in both devices, use command 9Fh for single I/O and AFh for quad I/O.

**Table 18: Read Identification**

| Parameter | MT25Q | MX66L |
|---|---|---|
| Manufacturer ID | 20h | C2h |
| Memory type | BAh | 20h |
| Memory capacity | 20h | 1Ah |

The MT25Q device has a unique ID composed of 17 read-only bytes:

- The first byte is set to 20h
- The next two bytes specify device configuration (top, bottom, or uniform architecture and hold/reset functionality)
- The next 14 bytes contain optional customized factory data

# Part Numbers

**Table 19: Device Part Numbers**

Clock frequency for all Macronix devices is 104 MHz (MAX).

| Micron Part Number | Macronix Part Number | Package | Secure | Note |
|---|---|---|---|---|
| MT25QL512ABA1E12-0SIT | | TBGA | No | |
| MT25QL512ABA1ESF-0SIT | | SOP16 | No | |
| MT25QL512ABA1ESF-MSIT | | SOP16 | Yes | 1 |
| MT25QL512ABA8E12-0SIT | MX66L51235FXDI-10G | TBGA | No | 2 |
| MT25QL512ABA8E12-1SIT | | TBGA | No | 2 |
| MT25QL512ABA8ESF-0SIT | MX66L51235FMI-10G | SOP16 | No | 2 |
| | MX66L51235FZ2I-10G | WSON | No | |

Notes: 1. Micron monotonic counter release.
2. Micron part number with reset pin.

# Revision History

## Rev. A – 1/14

- Initial release

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www.micron.com/productsupport Customer Comment Line: 800-932-4992