Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- · Trench MOSFET technology

3. Applications

- Relay driver
- · High-speed line driver
- · High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	٧
V_{GS}	gate-source voltage			-8	-	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-	-2.1	Α
Static characte	eristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -2.1 \text{ A}; T_j = 25 \text{ °C}$		-	55	70	mΩ

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	3	D I
2	S	source		
3	D	drain		G P
				S 017aaa257
			SOT23	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
NXV65UP		plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23			

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
NXV65UP	%5L

^{[1] % =} placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-2.1	А
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-1.3	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-8.4	А
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	340	mW
			[1]	-	480	mW
		T _{sp} = 25 °C		-	2.1	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode					
Is	source current	T _{amb} = 25 °C	[1]	-	-0.4	А

- Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm². Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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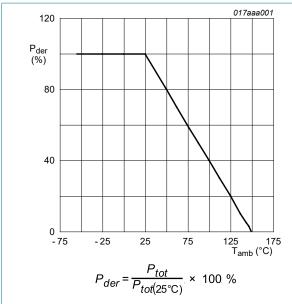


Fig. 1. Normalized total power dissipation as a function of ambient temperature

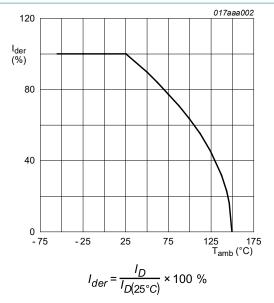


Fig. 2. Normalized continuous drain current as a function of ambient temperature

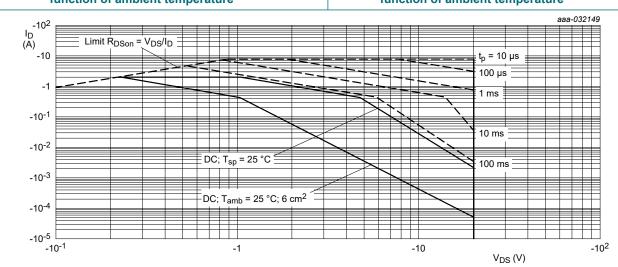


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from	in free air	[1]	-	325	370	K/W
junction to ambient	junction to ambient		[2]	-	230	260	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	50	60	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

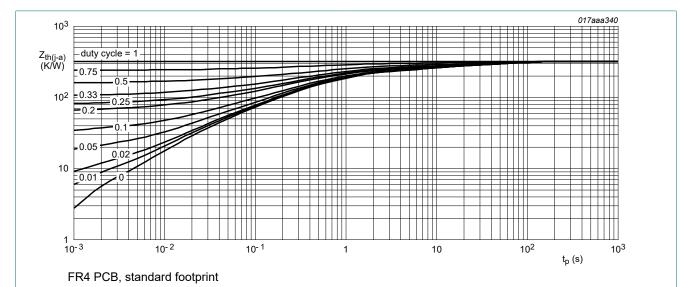


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

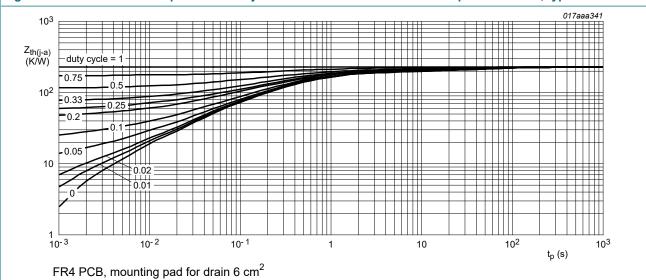


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	-0.5	-0.7	-1	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
I _{GSS}	gate leakage current	V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = -4.5 \text{ V}; I_D = -2.1 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	55	70	mΩ
	resistance	V_{GS} = -4.5 V; I_D = -2.1 A; T_j = 150 °C	-	86	110	mΩ
		$V_{GS} = -2.5 \text{ V}; I_D = -1.7 \text{ A}; T_j = 25 \text{ °C}$	-	74	100	mΩ
		V _{GS} = -1.8 V; I _D = -1.4 A; T _j = 25 °C	-	101	150	mΩ
9 _{fs}	forward transconductance	$V_{DS} = -5 \text{ V}; I_D = -2.1 \text{ A}; T_j = 25 \text{ °C}$	-	6.6	-	S
R _G	gate resistance	f = 1 MHz	-	8.4	-	Ω
Dynamic ch	aracteristics			'		
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -2.1 A; V _{GS} = -4.5 V;	-	5.8	8.7	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	0.7	-	nC
Q _{GD}	gate-drain charge		-	1.8	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V;	-	458	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	70	-	pF
C _{rss}	reverse transfer capacitance		-	62	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -2.1 A; V _{GS} = -4.5 V;	-	6	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 ^{\circ}C$	-	13	-	ns
t _{d(off)}	turn-off delay time		-	46	-	ns
t _f	fall time		-	18	-	ns
Source-drai	n diode		1			
V_{SD}	source-drain voltage	I _S = -0.4 A; V _{GS} = 0 V; T _i = 25 °C	-	-0.7	-1.2	V

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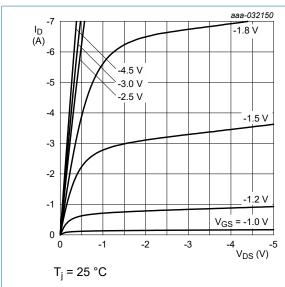


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

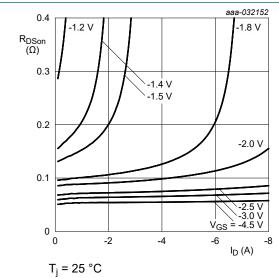


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

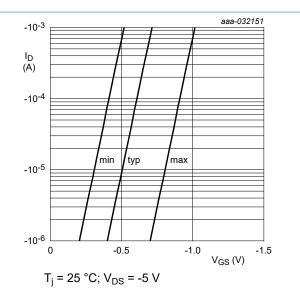


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

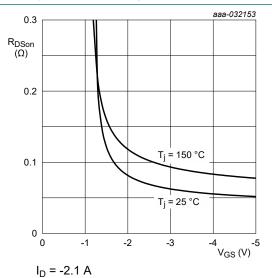


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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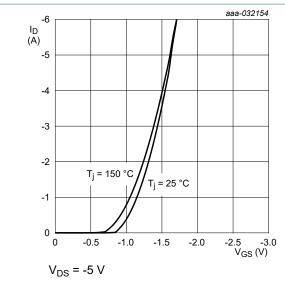


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

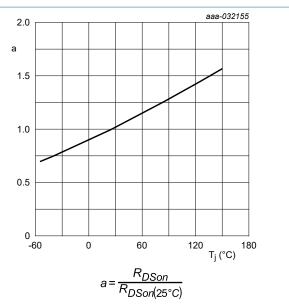


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

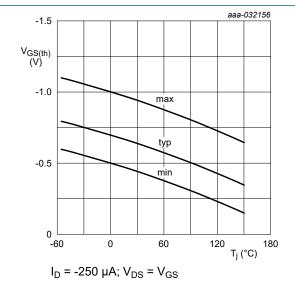
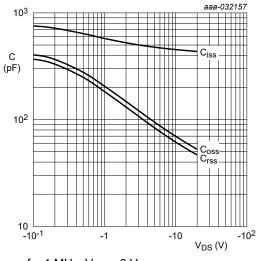


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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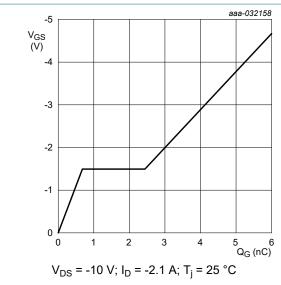


Fig. 14. Gate-source voltage as a function of gate charge; typical values

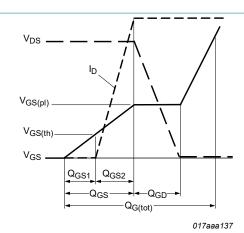


Fig. 15. Gate charge waveform definitions

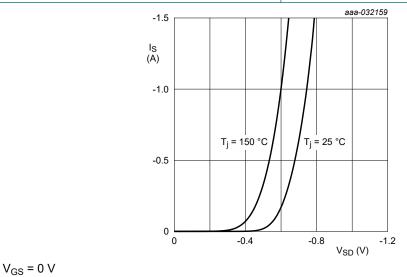
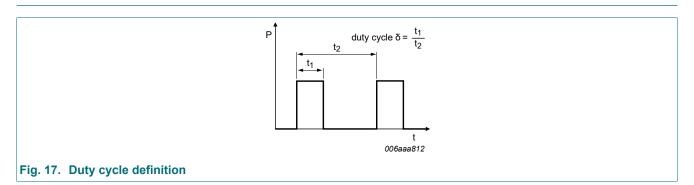


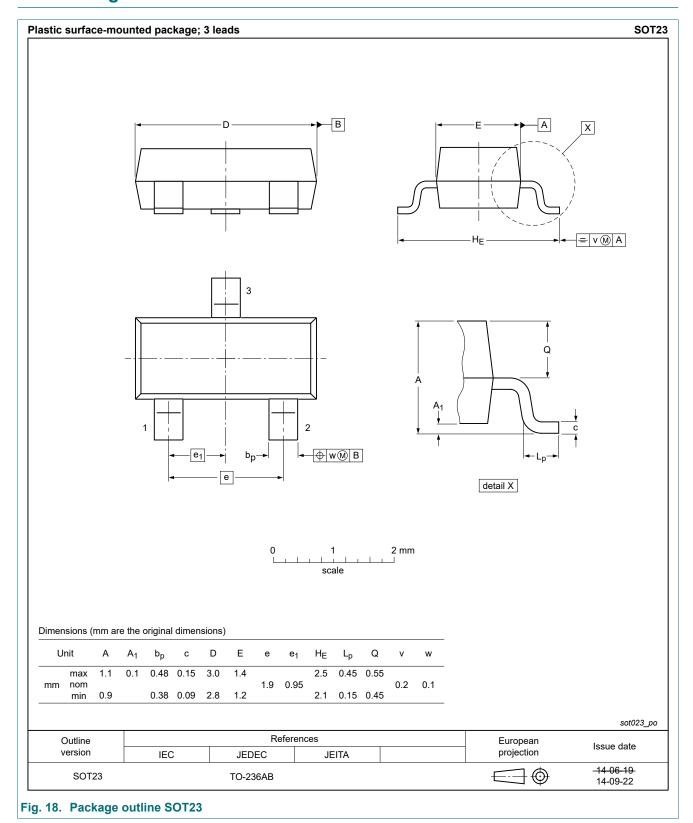
Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information



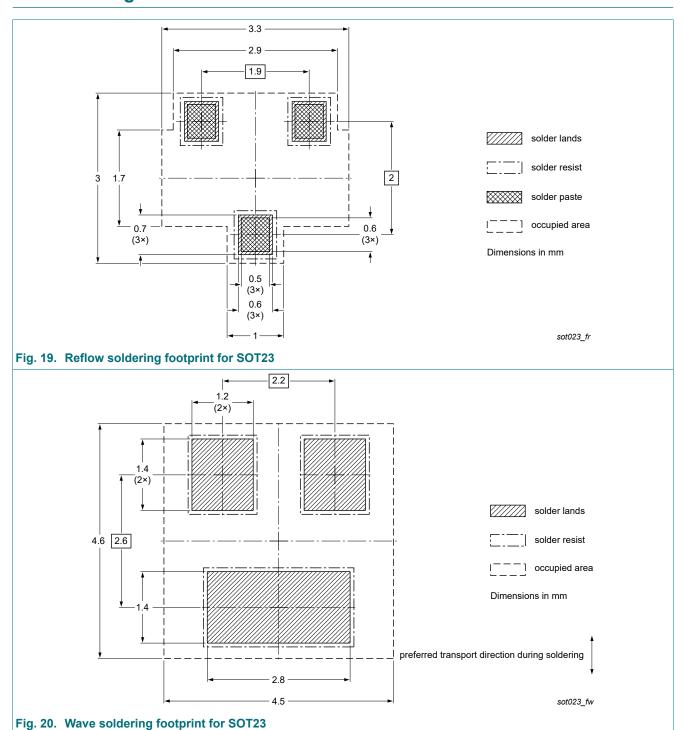
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12. Package outline



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13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NXV65UP v.1	20201019	Product	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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