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Kind regards,

Team Nexperia



PBSS5220V

20 V, 2 A PNP low V_{CEsat} (BISS) transistor Rev. 03 — 14 December 2009

Product data sheet

Product profile 1.

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT666 Surface Mounted Device (SMD) plastic package.

NPN complement: PBSS4220V.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- DC-to-DC conversion
- MOSFET gate driving
- Motor control
- Charging circuits
- Low power switches (e.g. motors, fans)
- Portable applications

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-20	V
I _C	collector current		-	-	-2	Α
I _{CM}	peak collector current	$t_p \leq 300~\mu s$	-	-	-4	Α
R _{CEsat}	collector-emitter saturation resistance	$I_{C} = -1 A;$ $I_{B} = -100 \text{ mA}$	<u>[1]</u> -	140	210	mΩ

^[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.02.$



20 V, 2 A PNP low V_{CEsat} (BISS) transistor

2. **Pinning information**

Table 2. **Pinning**

Pin	Description	Simplified outline	Symbol
1	collector		
2	collector	6 5 4	1, 2, 5, 6
3	base		3 —
4	emitter		Ì
5	collector		4 sym030
6	collector	1 2 3	5,

Ordering information 3.

Table 3. **Ordering information**

Type number	Package		
	Name	Description	Version
PBSS5220V	-	plastic surface mounted package; 6 leads	SOT666

Marking 4.

Table 4. **Marking codes**

Type number	Marking code
PBSS5220V	N7

Limiting values 5.

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	-20	V
V_{CEO}	collector-emitter voltage	open base	-	-20	V
V_{EBO}	emitter-base voltage	open collector	-	-5	V
I _C	collector current		-	-2	Α
I _{CM}	peak collector current	$t_p \leq 300~\mu s$	-	-4	Α
I _B	base current		-	-0.3	Α
I _{BM}	peak base current	$t_p \leq 300~\mu s$	-	-0.6	Α
P _{tot}	total power dissipation	$T_{amb} \leq 25 ^{\circ}C$	[1][4] -	0.3	W
			[2][4]	0.5	W
			[3][4]	0.9	W
T _j	junction temperature		-	150	°C

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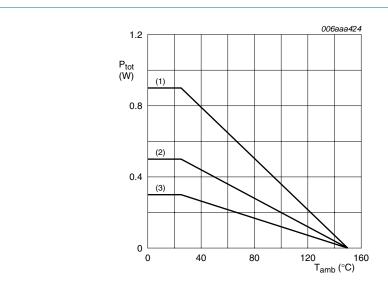
20 V, 2 A PNP low V_{CEsat} (BISS) transistor

Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- Device mounted on a ceramic PCB, Al₂O₃, standard footprint. [3]
- Reflow soldering is the only recommended soldering method.



- (1) Ceramic PCB, Al₂O₃, standard footprint
- (2) FR4 PCB, mounting pad for collector 1 cm²
- (3) FR4 PCB, standard footprint

Fig 1. **Power derating curves**

20 V, 2 A PNP low V_{CEsat} (BISS) transistor

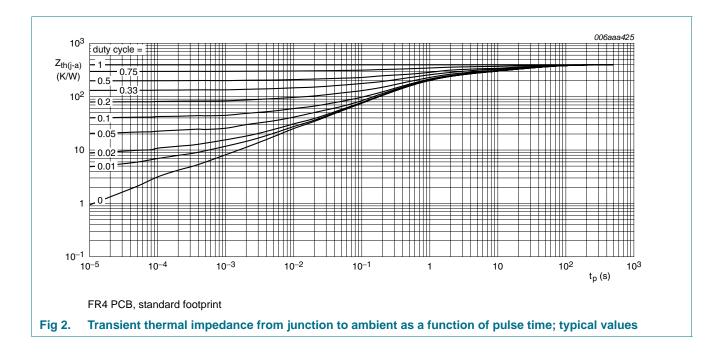
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Thermal characteristics 6.

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Mi	in Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from		[1][4]	-	410	K/W
	junction to ambient		[2][4]	-	250	K/W
			[3][4]	-	140	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	80	K/W

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm². [2]
- Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
- Reflow soldering is the only recommended soldering method.



NXP Semiconductors PBSS5220V

20 V, 2 A PNP low V_{CEsat} (BISS) transistor

7. Characteristics

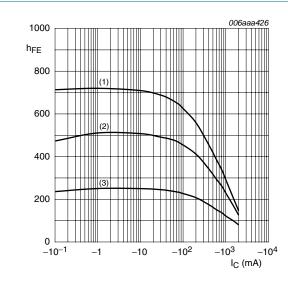
Table 7. Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Uni
I _{CBO}	collector-base cut-off	$V_{CB} = -20 \text{ V}; I_E = 0 \text{ A}$		-	-	-0.1	μΑ
	current	$V_{CB} = -20 \text{ V}; I_E = 0 \text{ A};$ $T_j = 150 \text{ °C}$		-	-	-50	μΑ
I _{CES}	collector-emitter cut-off current	$V_{CE} = -20 \text{ V}; V_{BE} = 0 \text{ V}$		-	-	-0.1	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$		-	-	-0.1	μΑ
h _{FE}	DC current gain	$V_{CE} = -2 \text{ V}; I_{C} = -1 \text{ mA}$		220	495	-	
		$V_{CE} = -2 \text{ V}; I_{C} = -100 \text{ mA}$		220	440	-	
		$V_{CE} = -2 \text{ V}; I_{C} = -500 \text{ mA}$	[1]	220	310	-	
		$V_{CE} = -2 \text{ V}; I_{C} = -1 \text{ A}$	<u>[1]</u>	155	220	-	
		$V_{CE} = -2 \text{ V}; I_{C} = -2 \text{ A}$	<u>[1]</u>	60	120	-	
V_{CEsat}	collector-emitter	$I_C = -100 \text{ mA}; I_B = -1 \text{ mA}$		-	-50	-80	mV
	saturation voltage	$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	-75	-115	mV
		$I_C = -1 A$; $I_B = -50 \text{ mA}$	[1]	-	-155	-220	mV
		$I_C = -1 A$; $I_B = -100 \text{ mA}$	[1]	-	-140	-210	mV
	$I_C = -2 \text{ A}; I_B = -100 \text{ mA}$	[1]	-	-305	-455	mV	
		$I_C = -2 \text{ A}; I_B = -200 \text{ mA}$	<u>[1]</u>	-	-265	-390	mV
R _{CEsat}	collector-emitter saturation resistance	$I_C = -1 A; I_B = -100 \text{ mA}$	[1]	-	140	210	mΩ
V_{BEsat}	base-emitter saturation	$I_C = -1 A$; $I_B = -50 \text{ mA}$	<u>[1]</u>	-	-0.95	-1.1	V
	voltage	$I_C = -1 A$; $I_B = -100 \text{ mA}$	<u>[1]</u>	-	-1	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -5 \text{ V}; I_{C} = -1 \text{ A}$		-	-0.8	-1	V
t _d	delay time	$I_C = -1 A$; $I_{Bon} = -50 \text{ mA}$;		-	8	-	ns
t _r	rise time	$I_{Boff} = 50 \text{ mA}$		-	34	-	ns
t _{on}	turn-on time			-	42	-	ns
ts	storage time			-	140	-	ns
t _f	fall time			-	45	-	ns
t _{off}	turn-off time			-	185	-	ns
f _T	transition frequency	$V_{CE} = -10 \text{ V}; I_{C} = -50 \text{ mA};$ f = 100 MHz		150	185	-	MH
C _c	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	15	20	pF

^[1] Pulse test: $t_p \leq 300~\mu s;~\delta \leq 0.02.$

20 V, 2 A PNP low V_{CEsat} (BISS) transistor



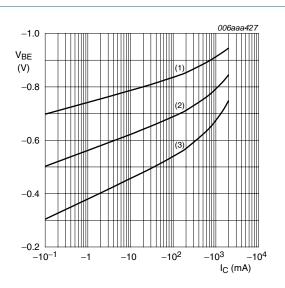
$$V_{CE} = -2 V$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \,^{\circ}C$$

Fig 3. DC current gain as a function of collector current; typical values



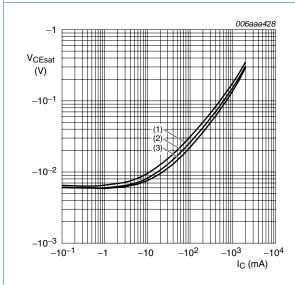
$$V_{CE} = -5 \text{ V}$$

(1)
$$T_{amb} = -55 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = 100 \, ^{\circ}C$$

Fig 4. Base-emitter voltage as a function of collector current; typical values



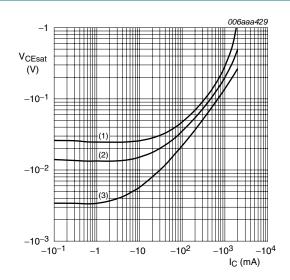
$$I_{\rm C}/I_{\rm B} = 20$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Collector-emitter saturation voltage as a Fig 5. function of collector current; typical values



$$T_{amb} = 25 \, ^{\circ}C$$

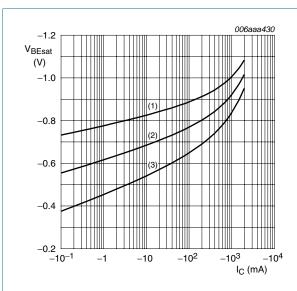
(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Collector-emitter saturation voltage as a Fig 6. function of collector current; typical values

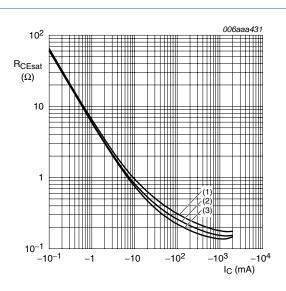
20 V, 2 A PNP low V_{CEsat} (BISS) transistor



$$I_{\rm C}/I_{\rm B} = 20$$

- (1) $T_{amb} = -55 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

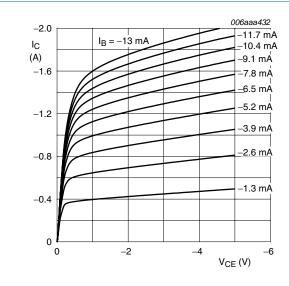
Base-emitter saturation voltage as a function Fig 7. of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

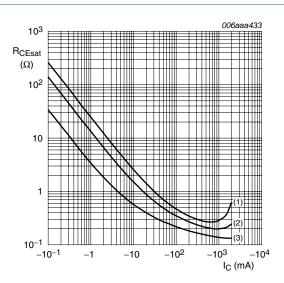
- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

Collector-emitter saturation resistance as a Fig 8. function of collector current; typical values



T_{amb} = 25 °C

Fig 9. Collector current as a function of collector-emitter voltage; typical values



T_{amb} = 25 °C

- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

Fig 10. Collector-emitter saturation resistance as a function of collector current; typical values

8. **Test information**

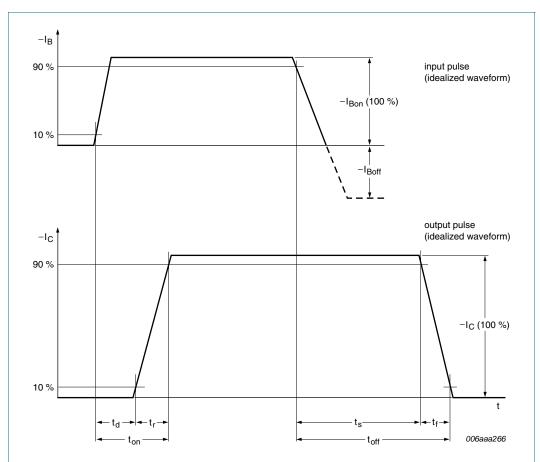
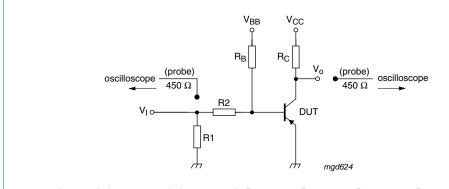


Fig 11. BISS transistor switching time definition



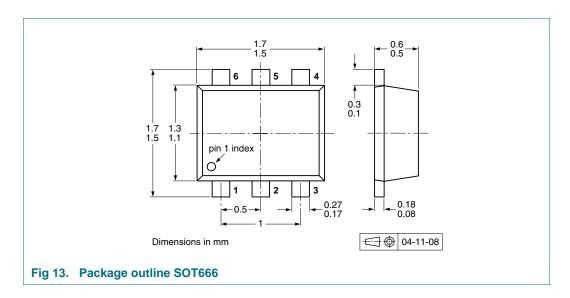
 I_C = –1 A; I_{Bon} = –50 mA; I_{Boff} = 50 mA; R1 = open; R2 = 45 $\Omega;$ R_B = 145 $\Omega;$ R_C = 10 Ω

Fig 12. Test circuit for switching times

NXP Semiconductors PBSS5220V

20 V, 2 A PNP low V_{CEsat} (BISS) transistor

9. Package outline



10. Packing information

Table 8. Packing methods

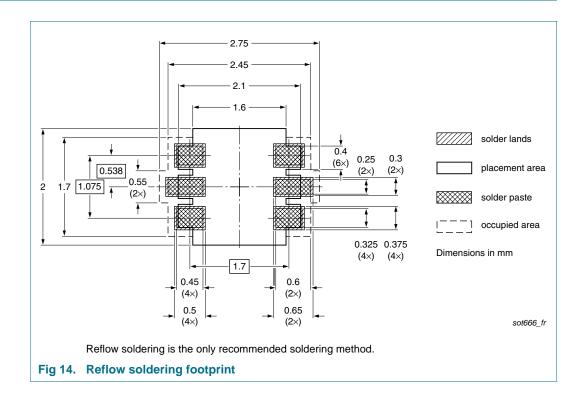
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	mber Package Description		Packing quantity	
			4000	8000
PBSS5220V SOT666		2 mm pitch, 8 mm tape and reel	-	-315
		4 mm pitch, 8 mm tape and reel	-115	-

^[1] For further information and the availability of packing methods, see Section 14.

20 V, 2 A PNP low V_{CEsat} (BISS) transistor

11. Soldering



20 V, 2 A PNP low V_{CEsat} (BISS) transistor

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5220V_3	20091214	Product data sheet	-	PBSS5220V_2
Modifications:	 This data sheet was changed to reflect the new company name NXP Semiconductor including new legal definitions and disclaimers. No changes were made to the tech content. 			
		eflow soldering footprint":	undated	
	• Figure 14 "R	eflow soldering footprint": u	ıpdated	
PBSS5220V_2		eflow soldering footprint": u	pdated	PBSS5220V_1

NXP Semiconductors PBSS5220V

20 V, 2 A PNP low V_{CEsat} (BISS) transistor

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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PBSS5220V

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