Technical Note

Migrating from Micron's N25Q to Micron's MT25Q

Introduction

This technical note describes the process for converting a system design from the Micron® N25Q Flash memory device to the Micron® MT25Q Flash memory device.

This document is written based on device information available at publication time. In case of inconsistency, information contained in the relevant N25Q or MT25Q data sheet supersedes the information in this technical note. This technical note does not provide detailed device information. The standard density specific device data sheet provides a complete description of device functionality, operating modes, and specifications.

General feature differences

Table 1: Feature Differences

Features	N25Q	MT25Q
Densities Monolithic	8Mb - 256Mb [1]	128Mb - 512Mb
Densities Stacked	512Mb (2 stack) 1Gb (4 stack)	1Gb (2 stack) 2Gb (4 stack)
Program	1 to 256 bytes	1 to 256 bytes
Sector architecture	Uniform sector (64KB)	Uniform sector (64KB)
Subsector	Uniform subsector (4KB)	Uniform subsector (4KB, 32KB)
Endurance	100,000 cycle	100,000 cycle
Retention	20 years	20 years
Industrial temp range	–40 to +85°C	–40 to +85°C
Automotive temp range	–40 to +125°C	–40 to +105°C

Note: 1. This TN compares only densities from 128Mb to 1Gb

Stacked device

In the table below a summary of stacked device for N25Q and MT25Q.

Table 2: Stack Summary Table

Micron Part Number	Maximum Monolithic Density	Density	Number of Stacks
N25Q512Axxx	256Mb	512Mb	2
N25Q00AAxxx		1Gb	4
MT25Qx01Gxxx	512Mb	1Gb	2
MT25Qx02Gxxx		2Gb	4

A dedicate technical note describes the features of stacked devices for N25Q and MT25Q. See Micron TN-25-05: N25Q and MT25Q Serial Flash Stacked Devices.

Package Configurations

Table 3: Package Configurations

Package	Shorted name	Part Nr code	N25Q	MT25Q	Notes
8-pin SOP2, 208 mils	SO8W	SE	Yes	Yes	1
16-pin SOP2, 300 mils	SO16W	SF	Yes	Yes	
24-ball T-PBGA, 05/6mm x 8mm (5 x 5 array)	T-PBGA 24	12	Yes	Yes	
24-ball T-PBGA, 05/6mm x 8mm (4 x 6 array)	T-PBGA 24	14	Yes	Yes	2
V-PDFN-8 6mm x 5mm Sawn (MLP8 6mm x 5mm)	DFN/6x5	F7	Yes	No	1,3
V-PDFN-8 8mm x 6mm (MLP8 8mm x 6mm)	DFN/8x6	F8	Yes	No	4
W-PDFN-8 6mm x 5mm (MLP8 6mm x 5mm)	WDFN/6x5	W7	No	Yes	1,3
W-PDFN-8 8mm x 6mm (MLP8 8mm x 6mm)	WDFN/8x6	W9	No	Yes	4
Wafer level chip-scale package, 15 balls, 9 active balls	XFWLBGA 0.5P	54	No	Yes	5
Wafer level chip-scale package, 15 balls, 9 active balls	XFWLBGA 0.5P	55	No	Yes	6
Wafer level chip-scale package, 27 balls, 9 active balls	XFWLBGA 0.5P	56	No	Yes	7

Notes:
1. Only for 128Mb density
2. N25Q device: Only for 128Mb density
3. Package F7 for N25Q and W7 for MT25Q is similar the only differences is seated height (see figures in datasheets)
4. Package F8 for N25Q and W9 is similar the only differences is seated height (see figures in datasheets)
5. Only for 128Mb 1.8V
6. Only for 256Mb 1.8V
7. Only for 512Mb 1.8V

Signal Descriptions

Table 4: Signal Differences

N25Q Signal	MT25Q Signal	Type	Description	Notes
S#	S#	Input	Chip select	
C	C	Input	Serial clock	
W#	W#	Input	Write protect	1
V_{PP}	-	Input	Enhanced program supply voltage	1
HOLD#	HOLD#	Input	HOLD or I/O	2
RESET#	RESET#	–	Reset	2,3
DQ[3:0]	DQ[3:0]	I/O	Serial data input or I/O	
V_{CC}	V_{CC}	Input	Supply voltage	
V_{SS}	V_{SS}	Input	Ground	

Notes: 1. Signal shared with DQ2.
2. Signal shared with DQ3.
3. For N25Q devices dedicated RESET# pin is available only for 256Mb and 512Mb (selected MPN) and it must be connected to an external pull-up resistor.

For MT25Q devices dedicated RESET# pin is available for every memory size (selected MPN). This signal has an internal pull-up resistor and may be left unconnected if not used.

Protocols, Commands, Addressing, and Transfer Rate

Table 5: Command Set Differences

Command	Command Code		Notes
	N25Q	**MT25Q**	**Notes**
QUAD INPUT/OUTPUT WORD READ	N/A	E7h	–
4-BYTE FAST READ (DTR mode)	N/A	0Eh	–
4-BYTE DUAL INPUT/OUTPUT FAST READ (DTR mode)	N/A	BEh	–
4-BYTE QUAD INPUT/OUTPUT FAST READ (DTR mode)	N/A	EEh	–
4-BYTE QUAD INPUT EXTENDED FAST PROGRAM	N/A	3Eh	–
32KB SUBSECTOR ERASE	N/A	52h	–
BULK ERASE	C7h	C7h/60h	3
ENTER DEEP POWER DOWN	B9h	B9h	2
RELEASE FROM DEEP POWER DOWN	ABh	ABh	2
READ SECTOR PROTECTION	N/A	2Dh	–
PROGRAM SECTOR PROTECTION	N/A	2Ch	–
4-BYTE READ VOLATILE LOCK BITS	N/A	E0h	–
4-BYTE WRITE VOLATILE LOCK BITS	N/A	E1h	–
READ NONVOLATILE LOCK BITS	N/A	E2h	–
WRITE NONVOLATILE LOCK BITS	N/A	E3h	–
ERASE NONVOLATILE LOCK BITS	N/A	E4h	–
READ GLOBAL FREEZE BIT	N/A	A7h	–
WRITE GLOBAL FREEZE BIT	N/A	A6h	–
READ PASSWORD	N/A	27h	–
WRITE PASSWORD	N/A	28h	–
UNLOCK PASSWORD	N/A	29h	–
CYCLIC REDUNDANCY CHECK	N/A	9Bh/27h	–

Notes: 1. Only differences between device commands are included. See the N25Q and MT25Q data sheets for a complete list of commands.
2. Available on both MT25Q 3V and 1.8V devices and on the N25Q 1.8V device. Not available on the N25Q 3V device.
3. Only for monolithic device (see table Stack Summary Table). For stacked the command is die erase (C4h) for both

Table 6: Addressing, Transfer Rate, and Protocol Differences

STR/DTR	Protocol	Reading Pattern	N25Q	MT25Q
STR	Extended SPI	READ, FASTREAD, DUAL OUTPUT FAST READ, DUAL INPUT/OUTPUT FAST READ, QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ,	Yes	Yes
	Dual input/ output SPI	All dual input/output commands	Yes	Yes
	Quad input/ output SPI	All quad input/output commands	Yes	Yes
DTR	Extended SPI	DUAL OUTPUT FAST READ, DUAL INPUT/ OUTPUT FAST READ, QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ,	Yes[1,2]	Yes[3]
	Dual input/ output SPI	All dual input/output commands	Yes[1,2]	Yes[3]
	Quad input/ output SPI	All quad input/output commands	Yes[1,2]	Yes[3]

Notes: 1. For N25Q 128Mb DTR mode are not supported
2. For N25Q (256Mb and higher) dedicated DTR commands are available allowing read operations working in DTR mode
3. For MT25Q dedicated DTR commands are available and, in addition, full DTR protocols are available to be enabled by relevant volatile or nonvolatile registers

Read dummy clocks tables

Table 7: Number of default dummy clocks 1.8V and 3.0V

SPI Proto-col	STR/DTR	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
		N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
Extended	STR	8	8	8	8	8	8	8	8	8	10
Extended	DTR	6	6	6	6	6	6	6	6	8	8
Dual	STR	8	8	8	8	8	8	-	-	-	-
Dual	DTR	6	6	6	6	6	6	-	-	-	-
Quad	STR	10	10	-	-	-	-	10	10	10	10
Quad	DTR	8	8	-	-	-	-	8	8	8	8

Note: 1. On N25Q 128Mb DTR mode are not supported

Table 8: STR – Dummy clock Cycles Required per Frequency (1.8V parts)

Number of Dummy Clock Cycles	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
1	90	94	80	79	50	60	43	44	30	39
2	100	112	90	97	70	77	60	61	40	48
3	108	129	100	106	80	86	75	78	50	58
4	108	146	105	115	90	97	90	97	60	69
5	108	162	108	125	100	106	100	106	70	78
6	108	166	108	134	105	115	105	115	80	86
7	108	166	108	143	108	125	108	125	86	97
8	108	166	108	152	108	134	108	134	95	106
9	108	166	108	162	108	143	108	143	105	115
10	108	166	108	166	108	152	108	152	108	125
11	108	166	108	166	108	162	108	162	108	134
12	108	166	108	166	108	166	108	166	108	143
13	108	166	108	166	108	166	108	166	108	156
14	108	166	108	166	108	166	108	166	108	166

Table 9: STR – Dummy clock Cycles Required per Frequency (3.0V parts)

Number of Dummy Clock Cycles	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
1	90	94	80	79	50	60	43	44	30	39
2	100	112	90	97	70	77	60	61	40	48
3	108	129	100	106	80	86	75	78	50	58
4	108	133	105	115	90	97	90	97	60	69
5	108	133	108	125	100	106	100	106	70	78
6	108	133	108	133	105	115	105	115	80	86
7	108	133	108	133	108	125	108	125	86	97
8	108	133	108	133	108	133	108	133	95	106
9	108	133	108	133	108	133	108	133	105	115
10	108	133	108	133	108	133	108	133	108	125
11:14	108	133	108	133	108	133	108	133	108	133

Table 10: DTR – Dummy clock Cycles Required per Frequency (1.8V & 3.0V parts)

Number of Dummy Clock Cycles	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
1	45	59	40	45	25	40	30	26	15	20
2	50	73	45	59	35	49	38	40	20	30
3	54	82	50	68	40	59	45	59	25	39
4	54	90	53	76	45	65	47	65	30	49
5	54	90	54	83	50	75	50	75	35	58
6	54	90	54	90	53	83	53	83	40	68
7	54	90	54	90	54	90	54	90	43	78
8	54	90	54	90	54	90	54	90	48	85
9	54	90	54	90	54	90	54	90	53	90
10:14	54	90	54	90	54	90	54	90	54	90

Serial Flash Discovery Parameter Table Differences

Table 11: SFDP Table Differences

Description	Byte Address	Bits	N25Q	MT25Q
Parameter ID	08h:16h	7:0	FFh	Used
Sector type 3 size	50h	7:0	00h	0Fh
Sector type 3 opcode	51h	7:0	00h	52h
Flash Basic Properties	54h:6Ch		FFh	Used
4-Byte Address Command	80h:87h		FFh	Used

Note: 1. Only differences between device SFDP Table are included. See the N25Q datasheets and for MT25Q TN-25-06: Serial Flash Discovery Parameters for MT25Q Family for serial Flash discovery parameter data.

Electrical Characteristics

Table 12: DC Characteristics 1.8V

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Standby current 128Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	14	100	12	50	µA	
Standby current 128Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}		N/A	20	80	µA	
Standby current 256Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	100	15	75	µA	
Standby current 256Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	20	120	µA	
Standby current 512Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	150	55	100	µA	
Standby current 512Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	55	200	µA	
Standby current 1Gb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	200	60	160	µA	
Standby current 1Gb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	60	400	µA	
Deep power-down current 128Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	10	2	30	µA	1
Deep power-down current 128Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	2	50	µA	1
Deep power-down current 256Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	20	2	30	µA	1
Deep power-down current 256Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	2	80	µA	1
Deep power-down current 512Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	50	2	50	µA	1
Deep power-down current 512Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA	1
Deep power-down current 1Gb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	90	5	100	µA	1
Deep power-down current 1Gb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	140	µA	1

Table 12: DC Characteristics 1.8V (Continued)

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Operating current (fast-read extended I/O)	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 166 MHz, DQ1 = open	–	15	–	20	mA	2,3
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	6	–	8	mA	2,4
Operating current (fast-read dual I/O)	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 166 MHz, DQ1 = open	–	18	–	25	mA	2,5
Operating current (fast-read quad I/O)	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 166 MHz STR or 80Mhz DTR, DQ1 = open	–	20	–	28	mA	2,6
Operating current (fast-read quad I/O)	I_{CC3}	MT25Q: C = 0.1V_{CC}/0.9V_{CC} at 90Mhz DTR, DQ1 = open	–	-	–	31	mA	7
Operating current (page program)	I_{CC4}	S# = V_{CC}	–	20	–	35	mA	
Operating current (write status register)	I_{CC5}	S# = V_{CC}	–	20	–	35	mA	
Operating current (erase)	I_{CC6}	S# = V_{CC}	–	20	–	35	mA	

Notes: 1. N25Q supported deep power-down current only for 1.8V configuration instead MT25Q support 1.8V and 3.0V configuration.
2. Because of different frequencies in test conditions, the MT25Q device has a maximum operating current (I_{CC3}) slightly higher than the N25Q device.
3. For stacked device (1Gb MT25Q) Icc3=35mA
4. For stacked device (1Gb MT25Q) Icc3=15mA
5. For stacked device (1Gb MT25Q) Icc3=40mA
6. For stacked device (1Gb MT25Q) Icc3=50mA
7. For stacked device (1Gb MT25Q) Icc3=55mA

Table 13: DC Characteristics 3.0V

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Standby current 128Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	14	100	15	50	µA	
Standby current 128Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	14	150	30	80	µA	
Standby current 256Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	100	30	75	µA	
Standby current 256Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	250	30	120	µA	
Standby current 512Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	150	30	100	µA	
Standby current 512Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	500	30	200	µA	
Standby current 1Gb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	200	60	160	µA	
Standby current 1Gb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	60	400	µA	
Deep power-down current 128Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	30	µA	1
Deep power-down current 128Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	50	µA	1
Deep power-down current 256Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	35	µA	1
Deep power-down current 256Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	80	µA	1
Deep power-down current 512Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	50	µA	1
Deep power-down current 512Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA	1
Deep power-down current 1Gb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA	1
Deep power-down current 1Gb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	140	µA	1

Table 13: DC Characteristics 3.0V (Continued)

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units	Note
			Typ	Max	Typ	Max		
Operating current (fast-read extended I/O)	I_{CC3}	N25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 108 MHz, DQ1 = open MT25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 133 MHz, DQ1 = open	–	15	–	20	mA	2,3
		C = $0.1V_{CC}$/$0.9V_{CC}$ at 54 MHz, DQ1 = open	–	6	–	8	mA	2,4
Operating current (fast-read dual I/O)	I_{CC3}	N25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 108 MHz, DQ1 = open MT25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 133 MHz, DQ1 = open	–	18	–	25	mA	2,5
Operating current (fast-read quad I/O)	I_{CC3}	N25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 108 MHz, DQ1 = open MT25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 133 MHz STR DQ1 = open	–	20	–	22	mA	2,6
Operating current (fast-read quad I/O)	I_{CC3}	N25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 108 MHz, DQ1 = open MT25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 80Mhz DTR, DQ1 = open	–	20	–	28	mA	2,7
Operating current (fast-read quad I/O)	I_{CC3}	MT25Q: C = $0.1V_{CC}$/$0.9V_{CC}$ at 90Mhz DTR, DQ1 = open	–	20	–	28	mA	2,8
Operating current (page program)	I_{CC4}	S# = V_{CC}	–	20	–	35	mA	
Operating current (write status register)	I_{CC5}	S# = V_{CC}	–	20	–	35	mA	
Operating current (erase)	I_{CC6}	S# = V_{CC}	–	20	–	35	mA	

Notes:
1. N25Q supported deep power-down current only for 1.8V configuration instead MT25Q support 1.8V and 3.0V configuration.
2. Because of different frequencies in test conditions, the MT25Q device has a maximum operating current (I_{CC3}) slightly higher than the N25Q device.
3. For stacked device (1Gb MT25Q) Icc3=35mA
4. For stacked device (1Gb MT25Q) Icc3=20mA
5. For stacked device (1Gb MT25Q) Icc3=35mA
6. For stacked device (1Gb MT25Q) Icc3=45mA

7. For stacked device (1Gb MT25Q) Icc3=50mA
8. For stacked device (1Gb MT25Q) Icc3=55mA

Table 14: AC Specifications 1.8V

Parameter	Symbol	Trans rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Clock frequency for all commands other than READ (extended-SPI, DIO-SPI, and QIO-SPI protocols)	^fC	STR	DC	108	DC	166	MHz
		DTR	DC	54	DC	90	MHz
Clock frequency for READ commands	^fR	STR	DC	54	DC	54	MHz
		DTR	DC	27	DC	27	MHz
Clock HIGH time	^tCH	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
Clock LOW time	^tCL	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
S# active setup time	^tSLCH	STR/DTR	4	–	2.7	–	ns
S# not active hold time (relative to clock)	^tCHSL	STR/DTR	4	–	2.7	–	ns
Data in setup time	^tDVCH	STR/DTR	2	–	1.75	–	ns
	^tDVCL	DTR only	-	–	1.75	–	ns
Data in hold time	^tCHDX	STR/DTR	3	–	2	–	ns
	^tCLDX	DTR only	3	–	2.75	–	ns
S# active hold time (relative to clock)	^tCHSH	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
S# active hold time (relative to clock LOW) Only for writes in DTR	^tCLSH	DTR only	4	–	3.375	–	ns
S# not active setup time (relative to clock)	^tSHCH	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
Output disable time	^tSHQZ	STR/DTR	–	8	–	6	ns
Clock low to output valid (under 30pF)	^tCLQV	STR/DTR	–	7	–	6	ns
Clock low to output valid (under 30pF)	^tCHQV	DTR only	–	8	–	6	ns
Output hold time (clock LOW)	^tCLQX	STR/DTR	1	-	1	-	ns
Output hold time (clock HIGH)	^tCHQX	DTR only	1	-	1	-	ns
HOLD setup time (relative to clock)	^tHLCH	STR/DTR	4	–	2.7	–	ns
HOLD hold time (relative to clock)	^tCHHH	STR/DTR	4	–	2.7	–	ns
HOLD setup time (relative to clock)	^tHHCH	STR/DTR	4	–	2.7	–	ns
HOLD hold time (relative to clock)	^tCHHL	STR/DTR	4	–	2.7	–	ns
HOLD to output Low-Z	^tHHQX	STR/DTR	-	8	-	5	ns
HOLD to output High-Z	^tHLQZ	STR/DTR	-	8	-	5	ns
Write protect setup time	^tWHSL	STR/DTR	20	–	20	–	ns
Write protect hold time	^tSHWL	STR/DTR	100	–	100	–	ns

Table 14: AC Specifications 1.8V (Continued)

Parameter	Symbol	Trans rate	N25Q		MT25Q		Units
			Min	**Max**	**Min**	**Max**	
Enhanced V$_{PPH}$ HIGH to S# LOW for extended and dual I/O page program	^{t}VPPHS		200	–	–	–	ns
S# HIGH to deep power-down	^{t}DP		–	–	3	–	µs
S# HIGH to standby mode (DPD exit time)	^{t}RDP		–	–	30	–	µs

Table 15: AC Specifications 3.0V

Parameter	Symbol	Trans rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Clock frequency for all commands other than READ (extended-SPI, DIO-SPI, and QIO-SPI protocols)	^{f}C	STR	DC	108	DC	133	MHz
		DTR	DC	54	DC	90	MHz
Clock frequency for READ commands	^{f}R	STR	DC	54	DC	54	MHz
		DTR	DC	27	DC	27	MHz
Clock HIGH time	^{t}CH	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
Clock LOW time	^{t}CL	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
S# active setup time	^{t}SLCH	STR/DTR	4	–	3.375	–	ns
S# not active hold time (relative to clock)	^{t}CHSL	STR/DTR	4	–	3.375	–	ns
Data in setup time	^{t}DVCH	STR	2	–	1.75	–	ns
		DTR	2	–	1.5	–	ns
	^{t}DVCL	DTR only	-	–	1.5	–	ns
Data in hold time	^{t}CHDX	STR/DTR	3	–	2.3	–	ns
	^{t}CLDX	DTR only	3	–	2.3	–	ns
S# active hold time (relative to clock)	^{t}CHSH	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
S# active hold time (relative to clock LOW) Only for writes in DTR	^{t}CLSH	DTR only	4	–	3.375	–	ns
S# not active setup time (relative to clock)	^{t}SHCH	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
Output disable time	^{t}SHQZ	STR/DTR	–	8	–	7	ns
Clock low to output valid (under 30pF)	^{t}CLQV	STR/DTR	–	7	–	6	ns
Clock low to output valid (under 30pF)	^{t}CHQV	DTR only	–	8	–	6	ns
Output hold time (clock LOW)	^{t}CLQX	STR/DTR	1	-	1.5	-	ns
Output hold time (clock HIGH)	^{t}CHQX	DTR only	1	-	1.5	-	ns
HOLD setup time (relative to clock)	^{t}HLCH	STR/DTR	4	–	3.375	–	ns
HOLD hold time (relative to clock)	^{t}CHHH	STR/DTR	4	–	3.375	–	ns
HOLD setup time (relative to clock)	^{t}HHCH	STR/DTR	4	–	3.375	–	ns
HOLD hold time (relative to clock)	^{t}CHHL	STR/DTR	4	–	3.375	–	ns
HOLD to output Low-Z	^{t}HHQX	STR/DTR	-	8	-	8	ns
HOLD to output High-Z	^{t}HLQZ	STR/DTR	-	8	-	8	ns
Write protect setup time	^{t}WHSL	STR/DTR	20	–	20	–	ns
Write protect hold time	^{t}SHWL	STR/DTR	100	–	100	–	ns

Table 15: AC Specifications 3.0V (Continued)

Parameter	Symbol	Trans rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Enhanced V_{PPH} HIGH to S# LOW for extended and dual I/O page program	^tVPPHS		200	–	–	–	ns
S# HIGH to deep power-down	^tDP		–	–	3	–	µs
S# HIGH to standby mode (DPD exit time)	^tRDP		–	–	30	–	µs

Table 16: WRITE Cycle, PROGRAM, ERASE Times

Parameter	Symbol	N25Q		MT25Q		Units	Note
		Typ	Max	Typ	Max		
WRITE STATUS REGISTER cycle time	^tW	1.3	8	1.3	8	ms	
WRITE NONVOLATILE CONFIGURA-TION REGISTER cycle time	^tWNVCR	0.2	3	0.2	1	s	
CLEAR FLAG STATUS REGISTER cy-cle time	^tCFSR	40	–	–	–	ns	
WRITE VOLATILE CONFIGURATION REGISTER cycle time	^tWVCR	40	–	–	–	ns	
WRITE VOLATILE ENHANCED CON-FIGURATION REGISTER cycle time	^tWRVECR	40	–	–	–	ns	
WRITE EXTENDED ADDRESS REGIS-TER cycle time	^tWREAR	40	–	–	–	ns	
NONVOLATILE SECTOR LOCK	^tPPBP	–	–	0.1	2.8	ms	
PROGRAM ASP REGISTER	^tASPP	–	–	0.1	0.5	ms	
PROGRAM PASSWORD	^tPASSP	–	–	0.2	0.8	ms	
ERASE NONVOLATILE SECTOR LOCK ARRAY	^tPPBE	–	–	0.2	1	s	
PAGE PROGRAM (256 bytes)	^tPP	0.4	5	0.2	2.8	ms	
PROGRAM OTP (64 bytes)	^tPOTP	0.2	–	0.12	0.8	ms	
64KB SECTOR ERASE	^tSE	0.6	3	0.15	1	s	
4KB SECTOR ERASE	^tSSE	0.25	0.8	0.05	0.4	s	
32KB SUBSECTOR ERASE	^tSSE	–	–	0.1	1	s	
128Mb BULK ERASE	^tBE	120	240	38	114	s	
256Mb BULK ERASE	^tBE	240	480	77	231	s	
512Mb BULK ERASE	^tBE	240	480	153	460	s	1

Note: 1. N25Q is die erase (two stack device)

Part Numbers

Table 17: Cross-Reference Part Numbers 128Mb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Note
N/A	MT25QL128ABA1ESE-MSIT	SO8 Wide	2.7V–3.6V	No	1
N25Q128A13ESE40x	MT25QL128ABA1ESE-0SIT	SO8 Wide	2.7V–3.6V	No	
N25Q128A13ESEH0E	N/A	SO8 Wide	2.7V–3.6V	Yes	
N25Q128A13ESEA0E	N/A	SO8 Wide	2.7V–3.6V	Yes	
N25Q128A11ESE40x	MT25QU128ABA1ESE-0SIT	SO8 Wide	1.7V–2.0V	No	
N/A	MT25QU128ABA1ESE-MSIT	SO8 Wide	1.7V–2.0V	No	1
N25Q128A13ESF40x	MT25QL128ABA8ESF-0SIT	SO16 Wide	2.7V–3.6V	No	2
N25Q128A13ESFH0x	MT25QL128ABA8ESF-0AAT	SO16 Wide	2.7V–3.6V	Yes	2
N25Q128A13ESFA0F		SO16 Wide	2.7V–3.6V	Yes	2
N25Q128A11ESF40x	MT25QU128ABA8ESF-0SIT	SO16 Wide	1.7V–2.0V	No	2
N/A	MT25QU128ABA8ESF-0AAT	SO16 Wide	1.7V–2.0V	Yes	
N25Q128A13E1240x	MT25QL128ABA8E12-0SIT	T-PBGA	2.7V–3.6V	No	2
N25Q128A13E1241x	MT25QL128ABA8E12-1SIT	T-PBGA	2.7V–3.6V	No	2,3
N25Q128A13E12A0F	MT25QL128ABA8E12-0AAT	T-PBGA	2.7V–3.6V	Yes	2
N/A	MT25QL128ABA8E14-0SIT	T-PBGA	2.7V–3.6V	No	
N/A	MT25QL128ABA8E14-1SIT	T-PBGA	2.7V–3.6V	No	3
N25Q128A11E1240x	MT25QU128ABA8E12-0SIT	T-PBGA	1.7V–2.0V	No	2
N25Q128A11E1241E	MT25QU128ABA8E12-1SIT	T-PBGA	1.7V–2.0V	No	2,3
N/A	MT25QU128ABA8E12-0AAT	T-PBGA	1.7V–2.0V	Yes	
N/A	MT25QU128ABA8E14-0SIT	T-PBGA	1.7V–2.0V	No	
N/A	MT25QU128ABA8E14-1SIT	T-PBGA	1.7V–2.0V	No	3
N25Q128A13EF740x	MT25QL128ABA1EW7-0SIT	DFN-8	2.7V–3.6V	No	4
N25Q128A13EF840x	MT25QL128ABA1EW9-0SIT	DFN-8	2.7V–3.6V	No	
N25Q128A13EF8A0F	N/A	DFN-8	2.7V–3.6V	Yes	
N/A	MT25QL128ABA1EW7-MSIT	DFN-8	2.7V–3.6V	No	1
N/A	MT25QU128ABA1EW7-MSIT	DFN-8	1.7V–2.0V	No	1
N25Q128A11EF740x	MT25QU128ABA1EW7-0SIT	DFN-8	1.7V–2.0V	No	4
N25Q128A11EF840x	MT25QU128ABA1EW9-0SIT	DFN-8	1.7V–2.0V	No	
N/A	MT25QU128ABA8E54-0SIT	XFWLBGA 0.5P	1.7V–2.0V	No	

Notes:
1. Monotonic Counter
2. MT25Q has a dedicated #RESET pin with internal pull up
3. Advanced security version
4. N25Q DFN/6x5 Sawn

Table 18: Cross-Reference Part Numbers 256Mb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Note
N25Q256A13ESF40x	MT25QL256ABA8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	2
N25Q256A83ESF40x		SO16 Wide	2.7V-3.6V	No	
N25Q256A73ESF40x	N/A	SO16 Wide	2.7V-3.6V	No	
N/A	MT25QL256ABA8ESF-MSIT	SO16 Wide	2.7V-3.6V	No	1
N25Q256A83ESFH0F	MT25QL256ABA8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	
N25Q256A83ESFA0F		SO16 Wide	2.7V-3.6V	Yes	
N25Q256A11ESF40x	MT25QU256ABA8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	2
N25Q256A81ESF40x		SO16 Wide	1.7V-2.0V	No	
N/A	MT25QU256ABA8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	
N/A	MT25QU256ABA8ESF-MSIT	SO16 Wide	1.7V-2.0V	No	1
N25Q256A13E1240x	MT25QL256ABA8E12-1SIT	T-PBGA	2.7V-3.6V	No	2,3
N25Q256A83E1240x		T-PBGA	2.7V-3.6V	No	3
N25Q256A13E1241x		T-PBGA	2.7V-3.6V	No	2,3
N/A	MT25QL256ABA8E14-1SIT	T-PBGA	2.7V-3.6V	No	3
N25Q256A13E12A0F	MT25QL256ABA8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	3
N25Q256A11E1240x	MT25QU256ABA8E12-1SIT	T-PBGA	1.7V-2.0V	No	3
N/A	MT25QU256ABA8E14-1SIT	T-PBGA	1.7V-2.0V	No	3
N/A	MT25QU256ABA8E12-0AAT	T-PBGA	1.7V-2.0V	Yes	
N25Q256A13EF840x	MT25QL256ABA1EW9-0SIT	DFN-8	2.7V-3.6V	No	
N/A	MT25QL256ABA1EW7-0SIT	DFN-8	2.7V-3.6V	No	
N25Q256A13EF8A0F	MT25QL256ABA1EW9-0AAT	DFN-8	2.7V-3.6V	Yes	
N25Q256A11EF840x	MT25QU256ABA1EW9-0SIT	DFN-8	1.7V-2.0V	No	
N/A	MT25QU256ABA1EW7-0SIT	DFN-8	1.7V-2.0V	No	
N/A	MT25QU256ABA8E55-0SIT	XFWLBGA 0.5P	1.7V-2.0V	No	

Notes:
1. Monotonic Counter
2. MT25Q has a dedicated #RESET pin with internal pull up
3. Advanced security version

Table 19: Cross-Reference Part Numbers 512Mb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Note
N25Q512A13GSF40x	MT25QL512ABB8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	1
N25Q512A83GSF40x		SO16 Wide	2.7V-3.6V	No	
N25Q512A13GSFA0F	MT25QL512ABB8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	1
N25Q512A13GSFH0E		SO16 Wide	2.7V-3.6V	Yes	1
N25Q512A83GSFA0F		SO16 Wide	2.7V-3.6V	Yes	
N25Q512A11GSF40x	MT25QU512ABB8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	1
N25Q512A81GSF40x		SO16 Wide	1.7V-2.0V	No	
N/A	MT25QU512ABB8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	

Table 19: Cross-Reference Part Numbers 512Mb (Continued)

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Note
N25Q512A13G1240x	MT25QL512ABB8E12-0SIT	T-PBGA	2.7V-3.6V	No	1
N25Q512A83G1240x		T-PBGA	2.7V-3.6V	No	
N25Q512A13G12A0F	MT25QL512ABB8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	1
N25Q512A13G12H0F		T-PBGA	2.7V-3.6V	Yes	1
N25Q512A11G1240x	MT25QU512ABB8E12-0SIT	T-PBGA	1.7V-2.0V	No	1
N/A	MT25QU512ABB8E12-0AAT	T-PBGA	1.7V-2.0V	Yes	
N25Q512A13GF840x	MT25QL512ABB1EW9-0SIT	DFN-8	2.7V-3.6V	No	
N/A	MT25QU512ABB1EW9-0SIT	DFN-8	1.7V-2.0V	No	
N/A	MT25QU512ABB8E56-0SIT	XFWLBGA 0.5P	1.7V-2.0V	No	

Notes: 1. MT25Q has a dedicated #RESET pin with internal pull up
2. Advanced security version

Table 20: Cross-Reference Part Numbers 1Gb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Note
N25Q00AA13GSF40x	MT25QL01GBBB8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	1
N/A	MT25QL01GBBB8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	
N25Q00AA11GSF40x	MT25QU01GBBB8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	1
N/A	MT25QU01GBBB8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	
N25Q00AA13G1240x	MT25QL01GBBB8E12-0SIT	T-PBGA	2.7V-3.6V	No	1
N/A	MT25QL01GBBB8E12-1SIT	T-PBGA	2.7V-3.6V	No	2
N/A	MT25QL01GBBB8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	
N25Q00AA11G1240x	MT25QU01GBBB8E12-0SIT	T-PBGA	1.7V-2.0V	No	1
N/A	MT25QL01GBBB1EW9-0SIT	DFN-8	2.7V-3.6V	No	
N/A	MT25QU01GBBB1EW9-0SIT	DFN-8	1.7V-2.0V	No	

Notes: 1. MT25Q has a dedicated #RESET pin with internal pull up
2. Advanced security version

Revision History

Rev. D – 05/17

- Review command table
- Adjust table Write Cycle, PROGRAM, ERASE Times

Rev. C – 09/16

- Fixed a table column spacing inconsistency

Rev. B – 08/16

- Correct tables: STR: Minimum Number of Dummy Cycles Required per Each Frequency, DTR: Minimum Number of Dummy Cycles Required per Each Frequency, and DC Characteristics
- Review registers consideration
- Review command and SFDP table (only differences)
- Updated Max DTR frequency to 90MHz for MT25Q
- Updated Part Numbers tables

Rev. A – 06/13

- Initial release

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