PUSB3AB2DF

Extremely low clamping low capacitance ESD protection

22 November 2019 Product data sheet

1. General description

Symmetrical bidirectional ElectroStatic Discharge (ESD) protection diode array, part of the TrEOS protection family. This device is housed in a DFN0603-3 (SOT8013) leadless ultra small Surface-Mounted Device (SMD) package designed to protect two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of two lines
- Very low diode capacitance C_d = 0.26 pF
- Extremely low clamping to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to ±20 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

4. Quick reference data

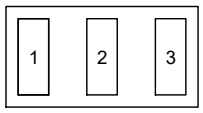
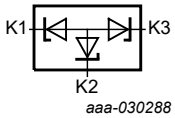
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-4	-	4	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.26	-	pF

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DFN0603-3 (SOT8013)**	
2	K2	cathode (diode 2)[1]		
3	K3	cathode (diode 3)		

[1] recommended for GND connection.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3AB2DF	DFN0603-3	DFN0603-3; plastic, ultra small and leadless full encapsulated package; 3 terminals; 0.225 mm pitch; 0.63 mm x 0.33 mm x 0.25 mm body	SOT8013

7. Marking

Table 4. Marking codes

Type number	Marking code
PUSB3AB2DF	A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-4	4	V
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[1]	-20	20	kV
		IEC 61000-4-2; air discharge	[1]	-20	20	kV

[1] Device stressed with ten non-repetitive ESD pulses.

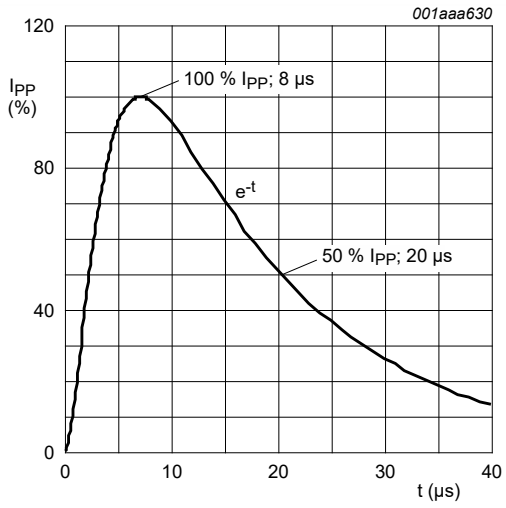


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

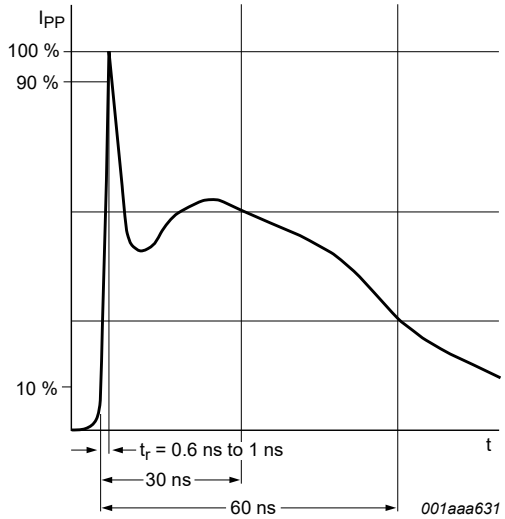


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25 °C		-	6.6	-	V
I_{RM}	reverse leakage current	V_{RWM} = 4 V; T_{amb} = 25 °C		-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.26	-	pF
		f = 1 MHz; V_R = 1.5 V; T_{amb} = 25 °C		-	0.23	-	pF
V_{CL}	clamping voltage	I_{TLP} = 4 A; T_{amb} = 25 °C	[1]	-	3.7	-	V
R_{dyn}	dynamic resistance	I_R = 5 A; T_{amb} = 25 °C	[1]	-	0.3	-	Ω
		I_R = -5 A; T_{amb} = 25 °C	[1]	-	0.3	-	Ω
f_{-3dB}	-3 dB cut-off frequency	T_{amb} = 25 °C; normalized to attenuation at 1 MHz		-	11.8	-	GHz

[1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

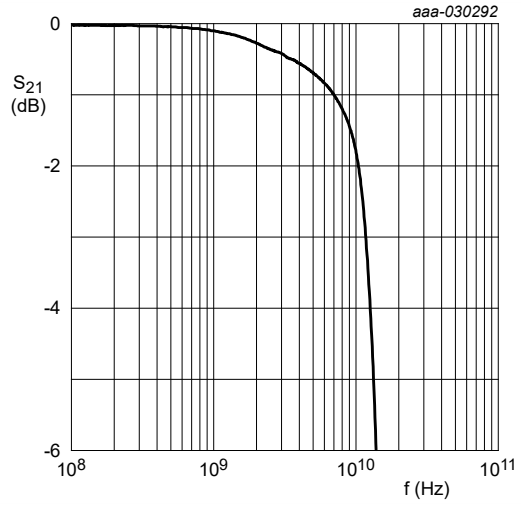
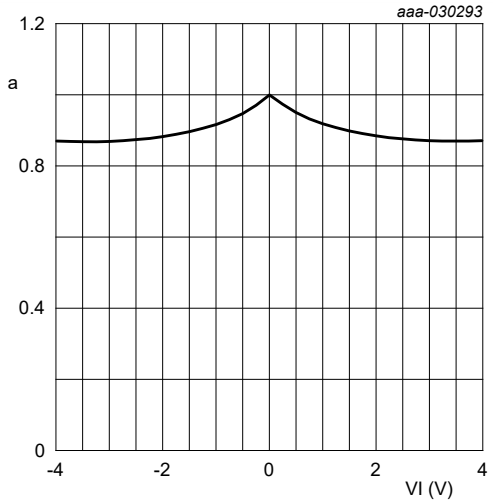
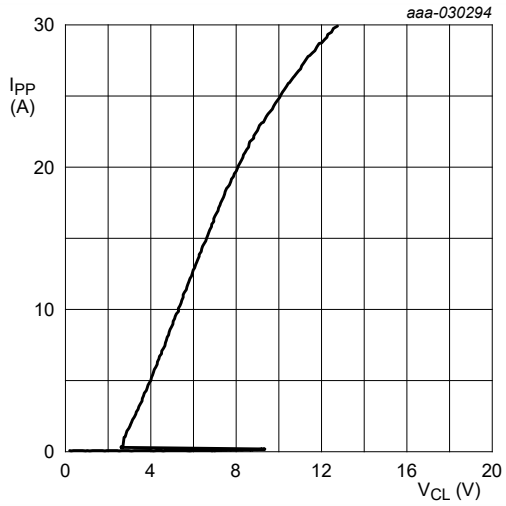


Fig. 3. Insertion loss; typical values



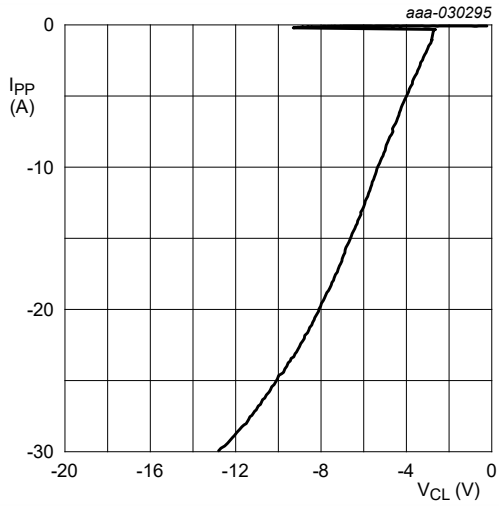
$$a = \frac{C_{line}}{C_{line(V_I=0\ V)}}$$

Fig. 4. Relative capacitance as a function of input voltage; typical values



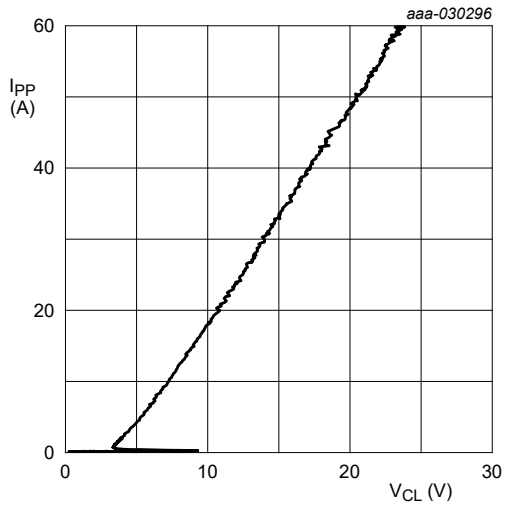
t_r = 1 ns
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 5. Dynamic resistance with positive clamping; typical values



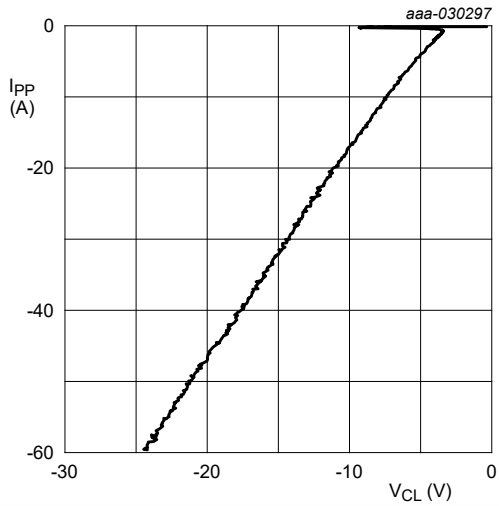
t_r = 1 ns
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 6. Dynamic resistance with negative clamping; typical values



t_r = 600 ps
t_p = 5 ns; Very-Fast Transmission Line Pulse (VF-TLP)

Fig. 7. Dynamic resistance with positive clamping; typical values



t_r = 600 ps
t_p = 5 ns; Very-Fast Transmission Line Pulse (VF-TLP)

Fig. 8. Dynamic resistance with negative clamping; typical values

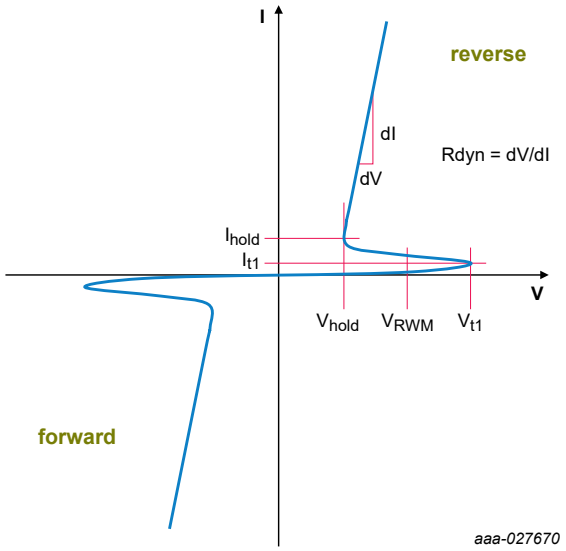


Fig. 9. V-I characteristics for a bidirectional ESD protection diode

10. Application information

The device is designed for the protection of two signal lines from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

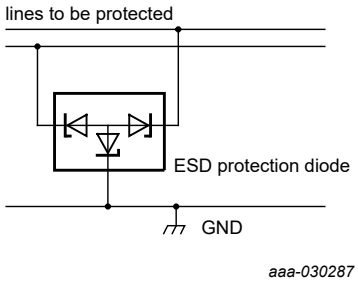


Fig. 10. Application diagram

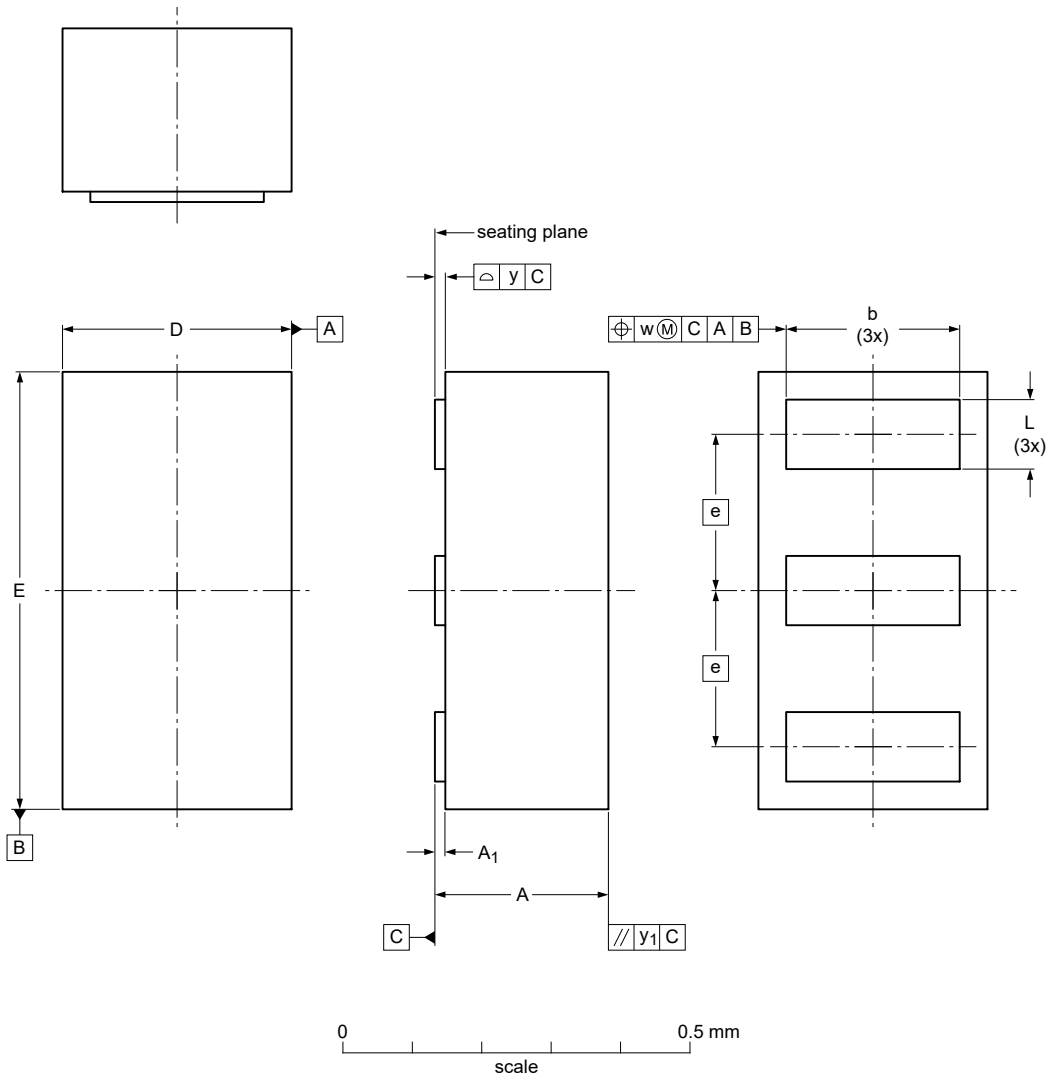
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

DFN0603-3; plastic, ultra small and leadless full encapsulated package; 3 terminals; 0.225 mm pitch; 0.63 mm x 0.33 mm x 0.25 mm body **SOT8013**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	D	E	e	L	w	y	y_1
mm	max	0.275	0.03	0.27	0.350	0.650		0.12			
	nom						0.225		0.04	0.03	0.05
	min	0.225		0.23	0.305	0.605		0.08			

Note
1. Device is electrically symmetrical

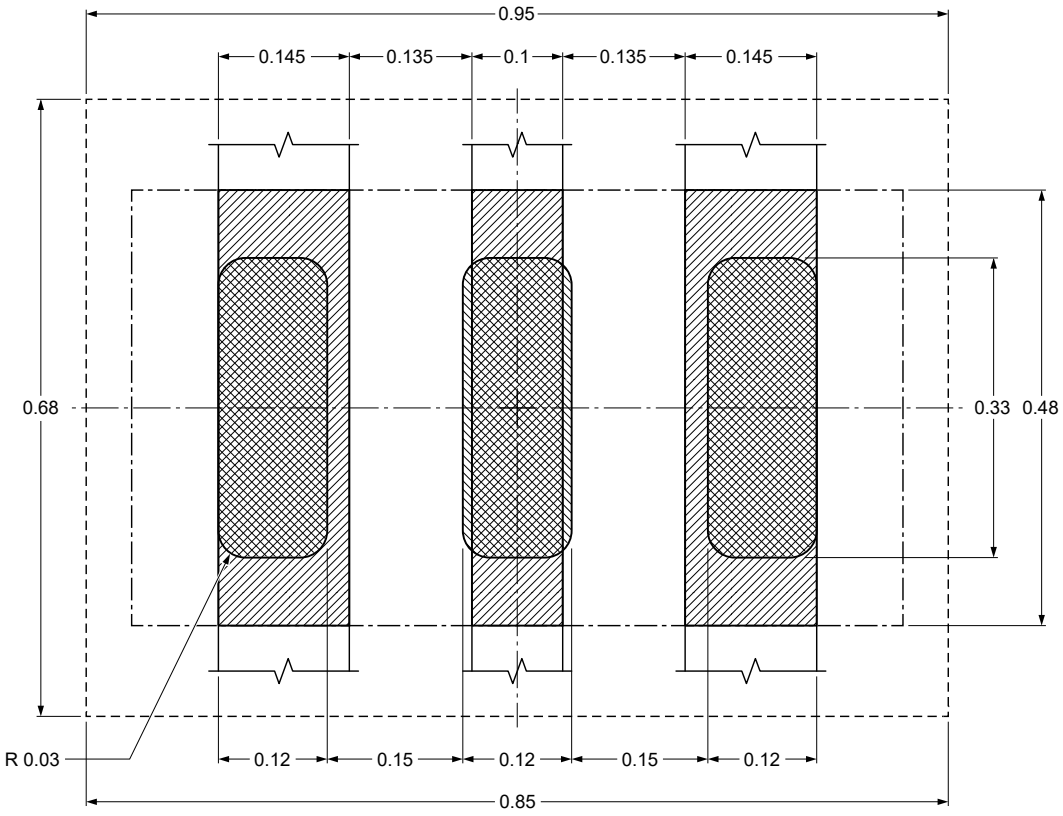
sot8013_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8013		---				~~19-08-06~~ 19-08-29

Fig. 11. Package outline DFN0603-3 (SOT8013)

12. Soldering

Footprint information for reflow soldering of ultra small and leadless encapsulated package; 3 terminals **SOT8013**



recommended stencil thickness: 0.08 mm

occupied area

solder resist

solder land
(Cu extends under
solder resist)

stencil opening

Dimensions in mm

Issue date 19-10-29

sot8013_fr

Fig. 12. Reflow soldering footprint for DFN0603-3 (SOT8013)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3AB2DF v.1	20191122	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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