# HEF4511B

## BCD to 7-segment latch/decoder/driver

Rev. 7 — 11 November 2011 Product data sheet

## 1. General description

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D0 to D3), an active HIGH latch enable input (LE), an active LOW ripple blanking input ($\overline{BL}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH NPN bipolar transistor segment outputs (Qa to Qg).

When LE is LOW and $\overline{BL}$ is HIGH, the state of the segment outputs (Qa to Qg) is determined by the data on D0 to D3. When LE goes HIGH, the last data present on D0 to D3 is stored in the latches and the segment outputs remain unchanged. When $\overline{LT}$ is LOW, all of the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BL}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BL}$ do not affect the latch circuit.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C and −40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

## 3. Ordering information

**Table 1. Ordering information**

*All types operate from −40 °C to +125 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| HEF4511BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4511BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## 4. Functional diagram

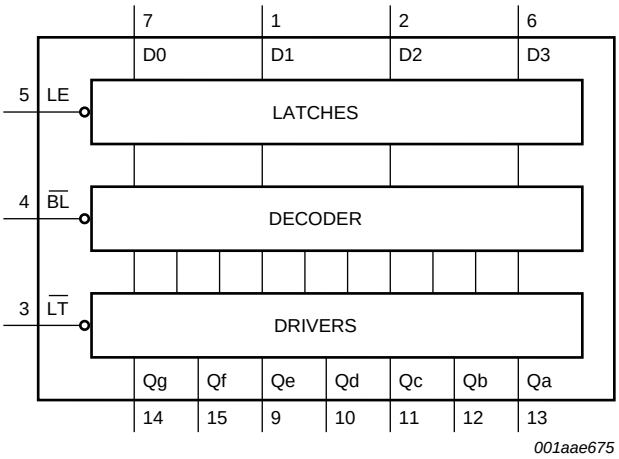



**Fig 1. Functional diagram**

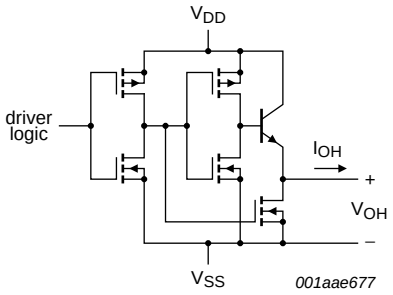



**Fig 2. Schematic diagram of output stage**

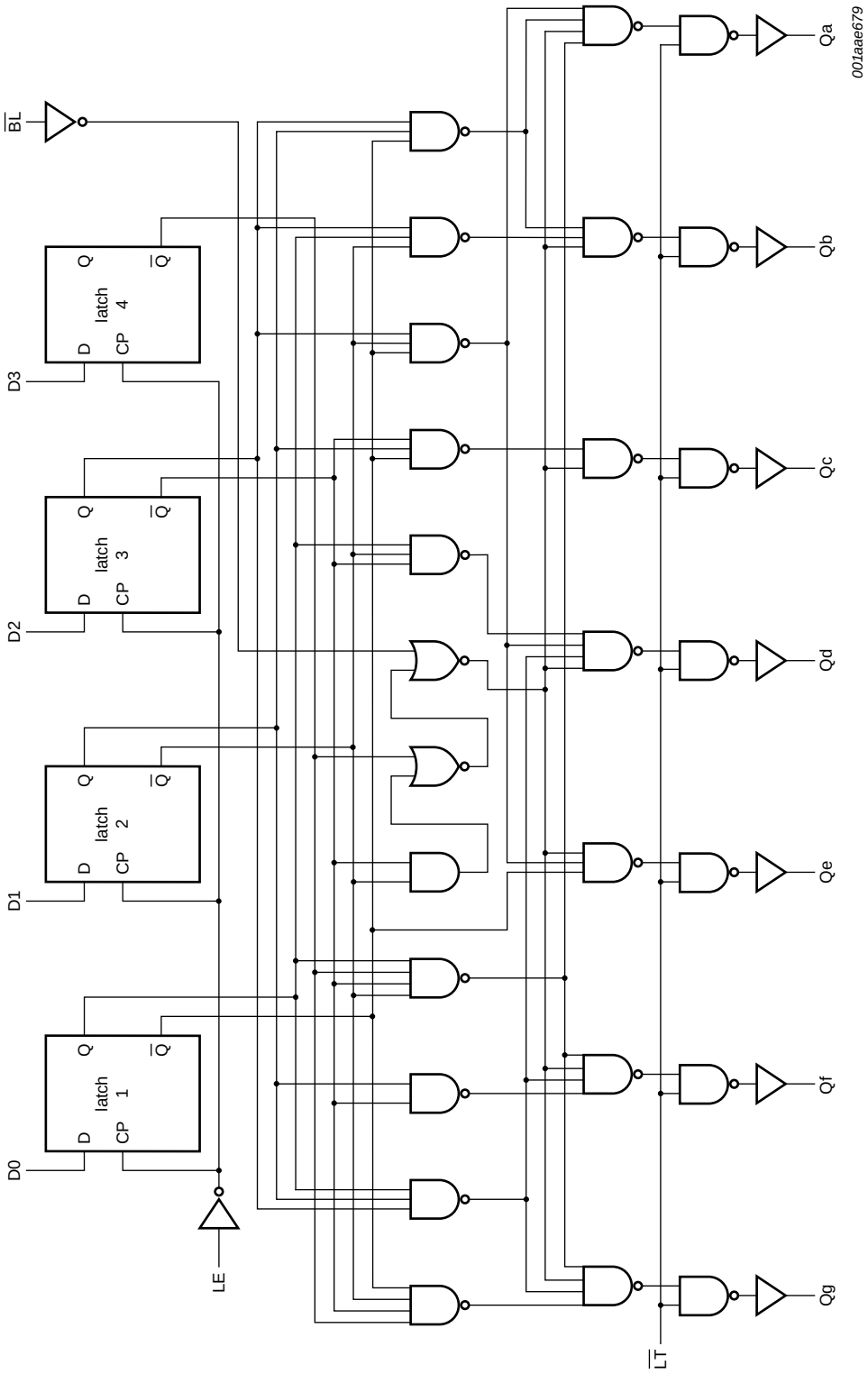



Fig 3. Logic diagram

# 5. Pinning information

## 5.1 Pinning

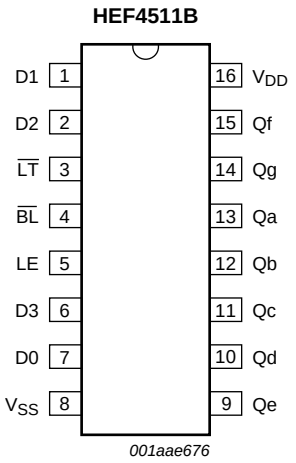



**Fig 4. Pin configuration DIP16 and SO16**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{LT}$ | 3 | lamp test input (active LOW) |
| $\overline{BL}$ | 4 | ripple blanking input (active LOW) |
| LE | 5 | latch enable input (active HIGH) |
| D0 to D3 | 7, 1, 2, 6 | address (data) input |
| $V_{SS}$ | 8 | ground supply voltage |
| Qa to Qg | 13, 12, 11, 10, 9, 15, 14 | segment output |
| $V_{DD}$ | 16 | supply voltage |

## 6. Functional description

**Table 3. Function table[1]**

| Inputs | | | | | | | Outputs | | | | | | | Display |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LE | $\overline{BL}$ | $\overline{LT}$ | D3 | D2 | D1 | D0 | Qa | Qb | Qc | Qd | Qe | Qf | Qg | |
| X | X | L | X | X | X | X | H | H | H | H | H | H | H | 8 |
| X | L | H | X | X | X | X | L | L | L | L | L | L | L | blank |
| L | H | H | L | L | L | L | H | H | H | H | H | H | L | 0 |
| L | H | H | L | L | L | H | L | H | H | L | L | L | L | 1 |
| L | H | H | L | L | H | L | H | H | L | H | H | L | H | 2 |
| L | H | H | L | L | H | H | H | H | H | H | L | L | H | 3 |
| L | H | H | L | H | L | L | L | H | H | L | L | H | H | 4 |
| L | H | H | L | H | L | H | H | L | H | H | L | H | H | 5 |
| L | H | H | L | H | H | L | L | L | H | H | H | H | H | 6 |
| L | H | H | L | H | H | H | H | H | H | L | L | L | L | 7 |
| L | H | H | H | L | L | L | H | H | H | H | H | H | H | 8 |
| L | H | H | H | L | L | H | H | H | H | L | L | H | H | 9 |
| L | H | H | H | L | H | X | L | L | L | L | L | L | L | blank |
| L | H | H | H | H | X | X | L | L | L | L | L | L | L | blank |
| H | H | H | X | X | X | X | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; N.C. = no change.

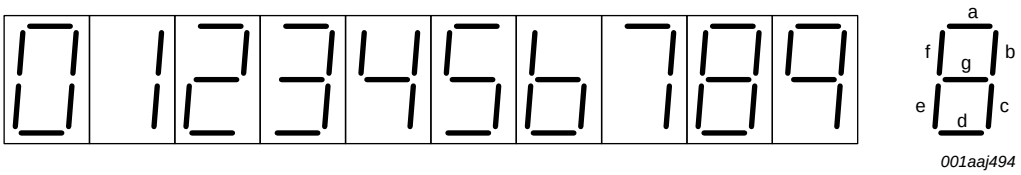



**Fig 5. Seven segment digital display with segment designation**

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | –0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | –0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{OH}$ | HIGH-level output current | | [1] | –25 | - | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | –40 | +125 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = 125 °C | | | | |
| | | DIP16 package | [2] | - | 750 | mW |
| | | SO16 package | [3] | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1] A destructive high current mode may occur if $V_I$ and $V_O$ are not constrained to the range $V_{SS} \leq V_I$ or $V_O \leq V_{DD}$.

[2] For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[3] For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | µs/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | µs/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | µs/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$; unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = +25 °C | | $T_{amb}$ = +85 °C | | $T_{amb}$ = +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 µA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 µA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | see Table 7 | - | - | - | - | - | - | - | - | - | - |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 µA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | –1.7 | - | –1.4 | - | –1.1 | - | –1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | –0.64 | - | –0.5 | - | –0.36 | - | –0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | –1.6 | - | –1.3 | - | –0.9 | - | –0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | –4.2 | - | –3.4 | - | –2.4 | - | –2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.64 | - | 0.5 | - | 0.36 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.6 | - | 1.3 | - | 0.9 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 4.2 | - | 3.4 | - | 2.4 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | ±0.1 | - | ±0.1 | - | ±1.0 | - | ±1.0 | µA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 5 | - | 5 | - | 150 | - | 150 | µA |
| | | | 10 V | - | 10 | - | 10 | - | 300 | - | 300 | µA |
| | | | 15 V | - | 20 | - | 20 | - | 600 | - | 600 | µA |
| $C_I$ | input capacitance | | - | - | - | - | 7.5 | - | - | - | - | pF |

**Table 7. Static characteristics for $V_{OH}$**

*$V_{SS}$ = 0 V.*

| Symbol | Parameter | $I_{OH}$ | $V_{DD}$ | $T_{amb}$ = –40 °C | $T_{amb}$ = +25 °C | | $T_{amb}$ = +85 °C | $T_{amb}$ = +125 °C | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | mA | V | Min | Min | Typ | Min | Min | |
| $V_{OH}$ | HIGH-level output voltage | 0 | 5 V | 4.10 | 4.10 | 4.40 | 4.10 | 4.10 | V |
| | | | 10 V | 9.10 | 9.10 | 9.90 | 9.10 | 9.10 | V |
| | | | 15 V | 14.10 | 14.10 | 14.40 | 14.10 | 14.10 | V |
| | | 5 | 5 V | - | - | 4.30 | - | - | V |
| | | | 10 V | - | - | 9.30 | - | - | V |
| | | | 15 V | - | - | 14.30 | - | - | V |
| | | 10 | 5 V | 3.60 | 3.60 | 4.25 | 3.30 | 3.20 | V |
| | | | 10 V | 8.75 | 8.75 | 9.25 | 8.45 | 8.35 | V |
| | | | 15 V | 13.75 | 13.75 | 14.30 | 13.45 | 13.35 | V |
| | | 15 | 5 V | - | - | 4.20 | - | - | V |
| | | | 10 V | - | - | 9.20 | - | - | V |
| | | | 15 V | - | - | 14.20 | - | - | V |
| | | 20 | 5 V | 2.80 | 2.80 | 4.20 | 2.50 | 2.30 | V |
| | | | 10 V | 8.10 | 8.10 | 9.20 | 7.80 | 7.60 | V |
| | | | 15 V | 13.10 | 13.10 | 14.20 | 12.80 | 12.60 | V |
| | | 25 | 5 V | - | - | 4.15 | - | - | V |
| | | | 10 V | - | - | 9.20 | - | - | V |
| | | | 15 V | - | - | 14.20 | - | - | V |

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

*$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | $V_{DD}$ | Extrapolation formula[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | Dn → Qn; see Figure 6 | 5 V | 128 ns + (0.55 ns/pF)$C_L$ | - | 155 | 310 | ns |
| | | | 10 V | 49 ns + (0.23 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)$C_L$ | - | 40 | 80 | ns |
| | | LE → Qn; see Figure 6 | 5 V | 133 ns + (0.55 ns/pF)$C_L$ | - | 160 | 320 | ns |
| | | | 10 V | 49 ns + (0.23 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 15 V | 37 ns + (0.16 ns/pF)$C_L$ | - | 45 | 90 | ns |
| | | $\overline{BL}$ → Qn; see Figure 6 | 5 V | 93 ns + (0.55 ns/pF)$C_L$ | - | 120 | 240 | ns |
| | | | 10 V | 39 ns + (0.23 ns/pF)$C_L$ | - | 50 | 100 | ns |
| | | | 15 V | 27 ns + (0.16 ns/pF)$C_L$ | - | 35 | 70 | ns |
| | | $\overline{LT}$ → Qn; see Figure 6 | 5 V | 52 ns + (0.55 ns/pF)$C_L$ | - | 80 | 160 | ns |
| | | | 10 V | 19 ns + (0.23 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | 12 ns + (0.16 ns/pF)$C_L$ | - | 20 | 40 | ns |

**Table 8. Dynamic characteristics** *...continued*

*$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | $V_{DD}$ | Extrapolation formula[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | LOW to HIGH propagation delay | Dn → Qn; see Figure 6 | 5 V | 108 ns + (0.55 ns/pF)$C_L$ | - | 135 | 270 | ns |
| | | | 10 V | 44 ns + (0.23 ns/pF)$C_L$ | - | 55 | 110 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)$C_L$ | - | 40 | 80 | ns |
| | | LE → Qn; see Figure 6 | 5 V | 133 ns + (0.55 ns/pF)$C_L$ | - | 160 | 320 | ns |
| | | | 10 V | 59 ns + (0.23 ns/pF)$C_L$ | - | 70 | 140 | ns |
| | | | 15 V | 42 ns + (0.16 ns/pF)$C_L$ | - | 50 | 100 | ns |
| | | $\overline{BL}$ → Qn; see Figure 6 | 5 V | 78 ns + (0.55 ns/pF)$C_L$ | - | 105 | 210 | ns |
| | | | 10 V | 29 ns + (0.23 ns/pF)$C_L$ | - | 40 | 80 | ns |
| | | | 15 V | 22 ns + (0.16 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | $\overline{LT}$ → Qn; see Figure 6 | 5 V | 33 ns + (0.55 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | 19 ns + (0.23 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | 17 ns + (0.16 ns/pF)$C_L$ | - | 25 | 50 | ns |
| $t_{THL}$ | HIGH to LOW output transition time | see Figure 6 | 5 V | 10 ns + (1.00 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | 9 ns + (0.42 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | 6 ns + (0.28 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_{TLH}$ | LOW to HIGH output transition time | see Figure 6 | 5 V | 20 ns + (1.00 ns/pF)$C_L$ | - | 25 | 50 | ns |
| | | | 10 V | 13 ns + (0.06 ns/pF)$C_L$ | - | 16 | 32 | ns |
| | | | 15 V | 10 ns + (0.06 ns/pF)$C_L$ | - | 13 | 26 | ns |
| $t_{su}$ | set-up time | Dn → LE; see Figure 7 | 5 V | | 50 | 25 | - | ns |
| | | | 10 V | | 25 | 12 | - | ns |
| | | | 15 V | | 20 | 9 | - | ns |
| $t_h$ | hold time | Dn → LE; see Figure 7 | 5 V | | 60 | 30 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 25 | 12 | - | ns |
| $t_W$ | pulse width | LE input LOW; minimum width; see Figure 7 | 5 V | | 80 | 40 | - | ns |
| | | | 10 V | | 40 | 20 | - | ns |
| | | | 15 V | | 35 | 17 | - | ns |

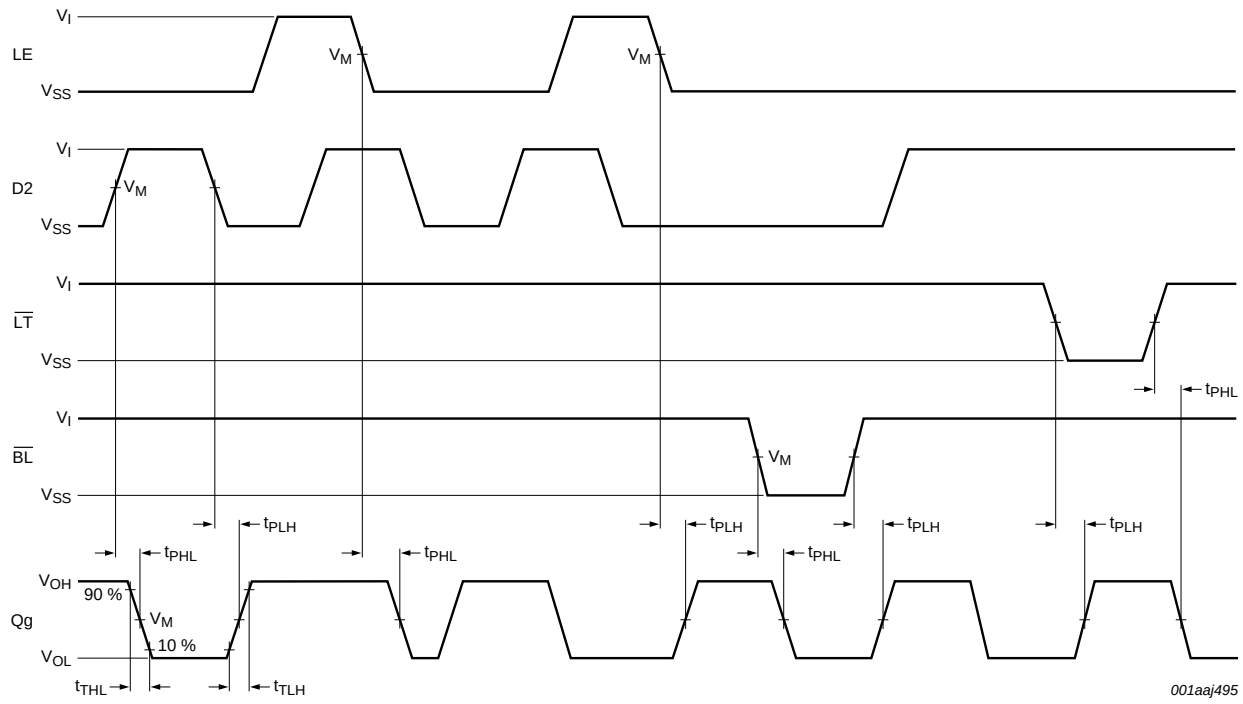
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).

**Table 9. Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown. $V_{SS}$ = 0 V; $t_r = t_f \leq 20$ ns; $T_{amb}$ = 25 °C.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (µW) | where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs. |
| | | 10 V | $P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 10000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

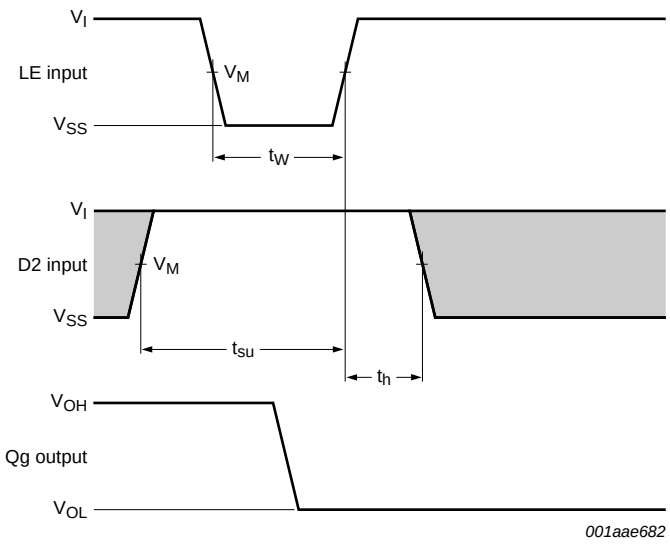
## 11. Waveforms




Conditions: D3 = LOW and D0 = D1 = HIGH.

Measurement points are given in Table 10.

**Fig 6. Propagation delays and output transition times**

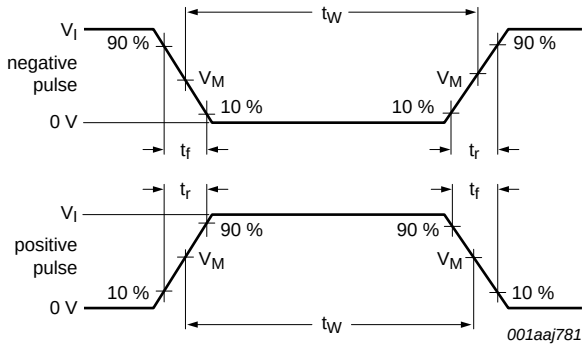



The shaded area indicates where the input is permitted to change for predictable output performance.

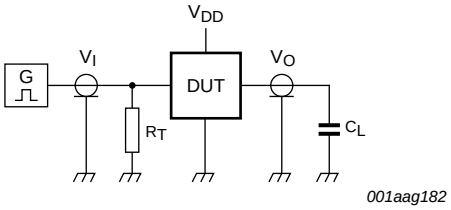
Conditions: D3 = LOW and D0 = D1 = $\overline{BL}$ = $\overline{LT}$ = HIGH.

Measurement points are given in Table 10.

**Fig 7. Waveforms showing minimum LE pulse width, set-up, and hold time for Dn to LE**




a. Input waveforms




b. Test circuit

Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

**Fig 8. Test circuit for measuring switching times**

**Table 10. Measurement points and test data**

| Supply voltage | Input | | | Load |
|---|---|---|---|---|
| | $V_I$ | $V_M$ | $t_r$, $t_f$ | $C_L$ |
| 5 V to 15 V | $V_{DD}$ | $0.5V_I$ | ≤ 20 ns | 50 pF |

## 12. Application information

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

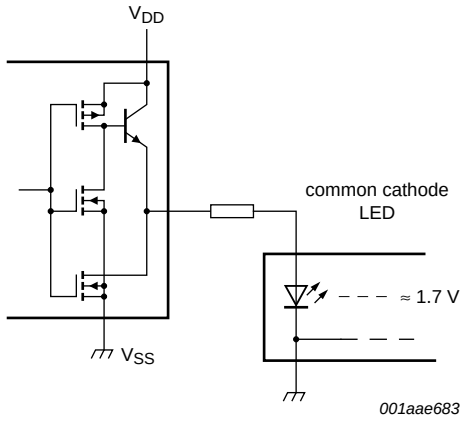



**Fig 9. Connection to common cathode LED display readout**

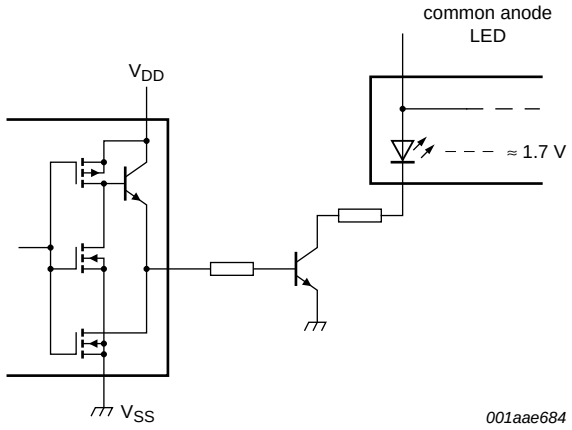
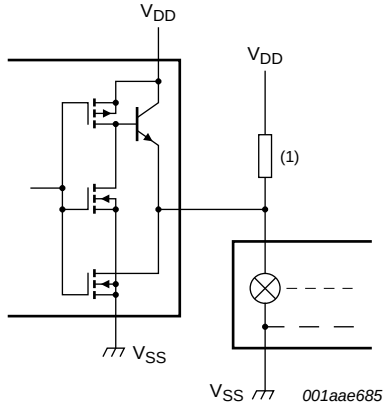



**Fig 10. Connection to common anode LED display readout**




(1) A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

**Fig 11. Connection to incandescent display readout**

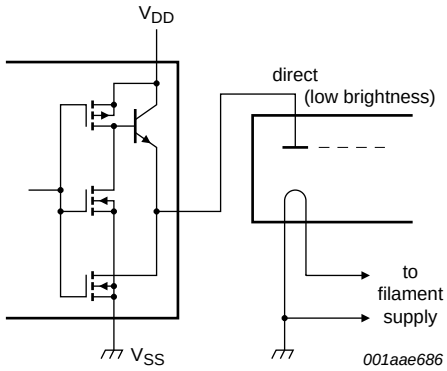



**Fig 12. Connection to fluorescent display readout**

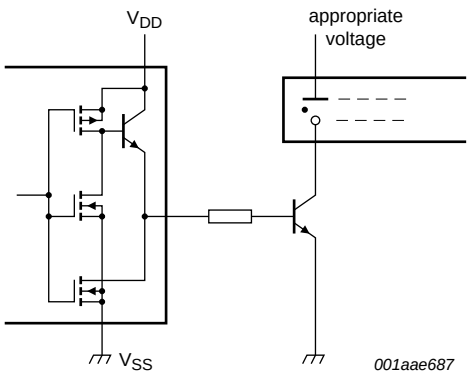
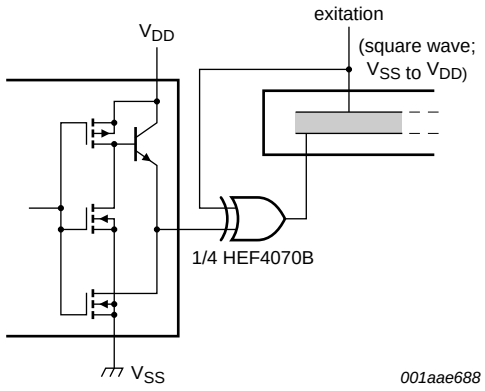



Fig 13. Connection to gas discharge display readout

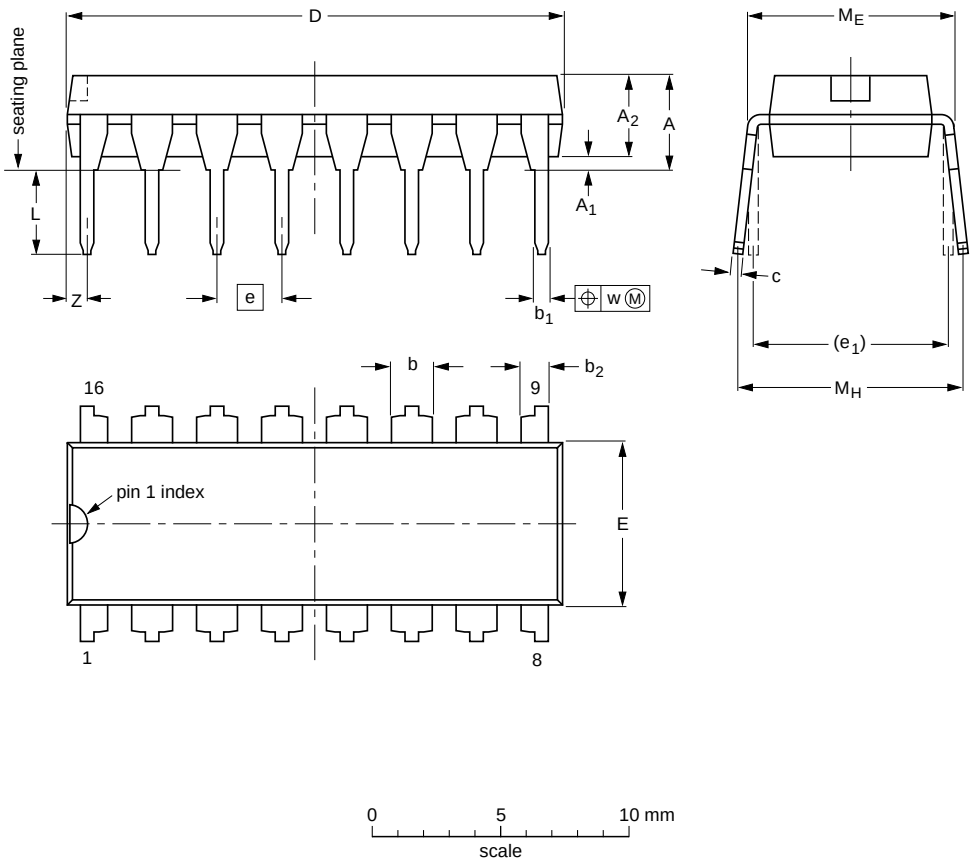



Direct DC drive of LCDs not recommended for life of LCD readouts.

Fig 14. Connection to LCD readout

## 13. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

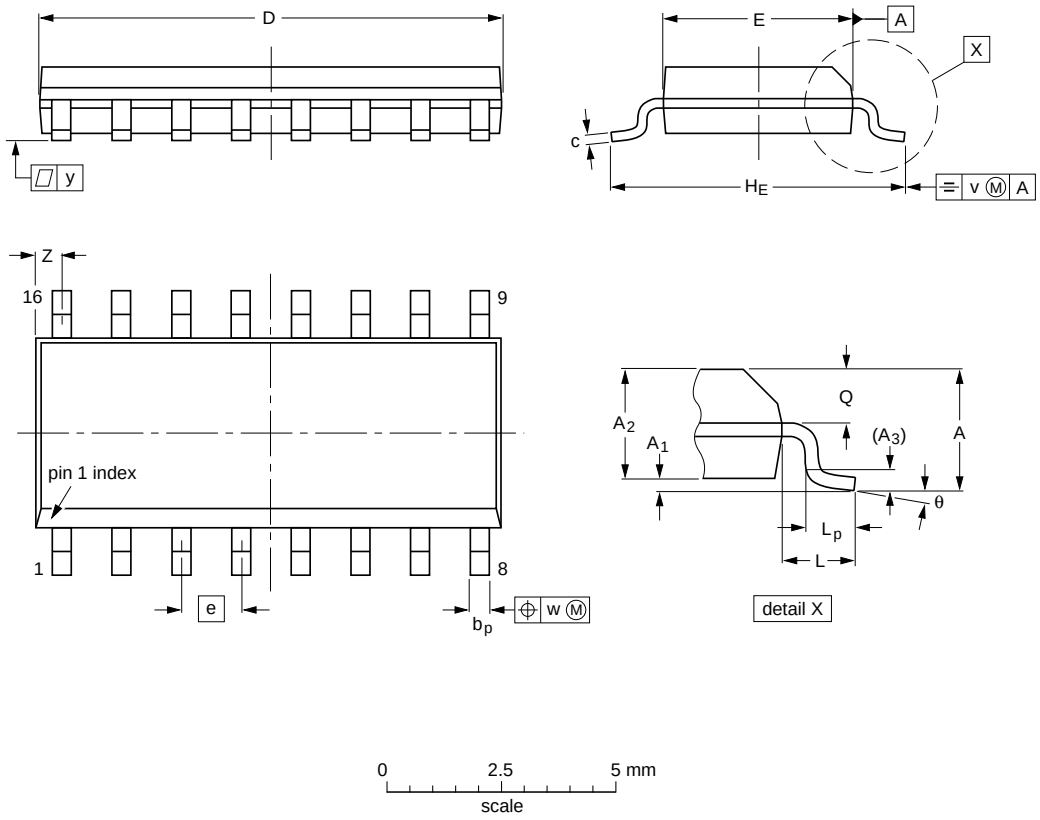
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 15. Package outline SOT38-4 (DIP16)**

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 16. Package outline SOT109-1 (SO16)**

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4511B v.7 | 20111111 | Product data sheet | - | HEF4511B v.6 |
| Modifications: | • Section Applications removed<br>• Table 6: $I_{OH}$ minimum values changed to maximum | | | |
| HEF4511B v.6 | 20091207 | Product data sheet | - | HEF4511B v.5 |
| HEF4511B v.5 | 20090813 | Product data sheet | - | HEF4511B v.4 |
| HEF4511B v.4 | 20090305 | Product data sheet | - | HEF4511B_CNV v.3 |
| HEF4511B_CNV v.3 | 19950101 | Product specification | - | HEF4511B_CNV v.2 |
| HEF4511B_CNV v.2 | 19950101 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 15.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 15.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 17. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 11 November 2011**
**Document identifier: HEF4511B**